Digitally Controlled Distributed Multiphase DC-DC Converters

Xu Zhang, Luca Corradini and Dragan Maksimovic
Colorado Power Electronics Center
ECEE Department
University of Colorado at Boulder
{xzhang, corradin, maksimov}@colorado.edu

Abstract — This paper describes a distributed master-slave multiphase DC-DC converter architecture and related digital control and communication techniques. In the distributed master-slave architecture, all converter modules are identical, but one module operates as the master. The master module communicates its voltage error and current data over a single-wire serial bus to remove the voltage sensing mismatch and to accomplish active current sharing among the modules. Experimental results are shown for a 5 V-to-12 V input, 1.3 V, 20 A output two-phase synchronous buck converter.

Index Terms — Multiphase DC-DC converter, current sharing, digital control, single-wire serial bus.

I. INTRODUCTION

In low voltage high current applications, interleaved multiphase converters are frequently used due to the advantages of power sharing among the phases, ripple cancellation, fast transient response, and small output capacitance. Control objectives in multiphase converters include output voltage regulation and current sharing among the phases. Many approaches have been presented to control multiphase converters [1, 4, 6, 10-12], with increasing attention given to digital control techniques [1-3, 5-8, 12-13]. The controller structure for multiphase converters can be classified into two basic categories: centralized or distributed. With a centralized controller, all phases are controlled by a common controller which generates the gate drive signals to the high side and low side power MOSFETs for all phases [1, 12]. The centralized controller is highly integrated and requires no additional pins for communication among phases. However, the number of phases is fixed and limited. On the other hand, a distributed controller architecture allows a greater degree of system modularity, flexibility and redundancy, but requires communication among the phases to facilitate appropriate phase shifts among the phases, as well as output voltage regulation and current sharing [10, 13, 14-15]. Problems related to voltage regulation and current sharing in a masterless distributed control architecture have been addressed in [10].

This paper presents an approach to digital control of a distributed master-slave architecture shown in Fig. 1, which has the following features:

• Flexibility: all modules are identical, so that each module could be operated either as a stand-alone (single phase) buck converter or paralleled with other modules to form a multi-phase converter. In this case, one module operates as the master and other modules operate as slave to supply higher current to the load.

• Simple communication: the digital voltage error and current data sampled in the master module are transmitted to the slave modules over a single-wire serial digital bus for output voltage regulation and current sharing purposes.

• One-wire connection among modules: a single wire digital bus communication is employed for active current sharing, interleaving phase shift and synchronization among modules. Other approaches normally required three or more wires for a similar parallel operation [14, 15].

Throughout the paper, experimental results are presented for a two-phase prototype operating from a 5 V-to-12 V input voltage source, regulating at 1.3 V output voltage over a 0-20 A load current range. The per-phase switching frequency is 400 kHz. The system and digital controller architectures are described in Section II. Digital bus and
serial communication are discussed in Section III. The analog-to-digital (A/D) sensing circuit is described in Section IV. Experimental results are shown in Section V and conclusions are presented in Section VI.

II. DIGITALLY CONTROLLED DISTRIBUTED MULTIPHASE CONVERTER

Fig. 1 shows the proposed distributed multiphase converter architecture. All modules are identical: each module, consisting of a synchronous buck converter and a controller, includes its own A/D sensing circuit, digital compensators and a digital pulse-width modulator (DPWM) [16]. When a module is operated as a stand-alone (single phase) converter, it regulates the output by sensing the local output voltage through its own A/D sensing circuitry and processes the voltage error through its voltage loop compensator; the current sharing functionality is disabled.

When operating in the distributed multi-phase configuration shown in Fig. 1, one of the modules (module 1 in Fig. 1) assumes the role of the master. The master designation can be decided by pin-strapping or at random by bus arbitration during start-up.

In the distributed multiphase mode the master module transmits both the current and voltage error information to the slave modules through the communication bus. The slave modules process the received current and voltage data for two distinct purposes:

1) The current information of the master module is compared with the local module current in order to adjust the duty cycle and achieve current sharing. This approach is similar to the traditional inner current loop method [9], except that in Fig. 1 each controller has its own voltage loop instead of sharing a common voltage compensator. This choice increases modularity while still keeping the advantages of the inner loop structure, including stable current sharing and precise output voltage regulation.

2) The voltage error received from the master unit is fed to the local (slave) digital compensator. This guarantees that all the voltage loops process exactly the same voltage error information, and therefore produce the very same control command. This eliminates problems associated with mismatches in the voltage sensing circuitries of the different modules, which would produce slightly different control commands. Competition between the various voltage loops could result in stability problems and possibly phase current saturation [10, 11]. In contrast, with shared voltage error information all digital loops behave exactly in the same way, which is equivalent to one common voltage loop but with increased modularity of the system.

A block diagram of the controller in each module is shown in Fig. 2. Each module uses the voltage error signal from its local A/D sensing circuit and disables the current sharing when it is programmed as a master module or when it operates as a stand-alone unit. When operating in the distributed multiphase structure, all slave modules use the voltage error from the master and compare their local current with the current from the master module to achieve current sharing.

An advantage of the distributed master-slave architecture is that the number of paralleled modules is flexible and that no separate master controller hardware is necessary, although the configuration still takes advantage of the master-slave control approaches.

Since the voltage error signal is sensed and communicated from the master module to the slave modules, the slave modules will respond to output voltage transients only when they receive the voltage error signal from the digital bus. In order to minimize delays in the voltage control loop, it is advantageous to transmit the voltage error within one switching period. A single-wire serial digital bus and a communication method are described in the next section to accomplish fast serial communication without the need for a very high frequency clock distribution or additional controller pins. In what follows, the current and voltage information are assumed to be 4 bit wide, which is consistent with the experimental prototype implementation.

III. DIGITAL BUS AND SERIAL COMMUNICATION

In digitally controlled converters, a two-wire I²C based PMbus (Power Management Bus) is often used to accomplish programmability, power management and diagnostics functions. It requires two bidirectional open-drain pins, Serial Data (SDA) and Serial Clock (SCL). Both master and slave send or receive data on the Serial Data bus based on a Serial Clock frequency. If each data is a 4 bit signal and the address is 7 bits, it would take more than ten Serial Clock cycles to transfer the data. So, this approach may not be sufficiently fast to accomplish communication of voltage error and current in the distributed architecture of Fig. 1 assuming a relatively low frequency Serial Clock. On the other hand, for a sufficiently high frequency Serial Clock, it is more difficult to respect rising and falling time requirements on the bus. A high frequency Serial Clock signal distributed among all modules would further result in increased power consumption and noise.

A single-wire bus has recently been proposed in [13] as an open-industry standard for current sharing in multiphase
converters in which an 8-bits current information is transmitted in the form of pulses with 2 different pulse widths, updated at a relatively low rate (about 10 kHz). The low speed communication limits the bandwidth of current sharing loop design and is not suitable for sharing the voltage error on the digital bus within one switching period. This approach is extended here to introduce a method suitable for fast voltage error and current data communication over a single-wire serial digital bus as shown in Fig. 3. Normally, each digital controller has an internal system clock whose frequency is significantly higher than the converter switching frequency. For example, in the experimental prototype described in this paper, the per-phase switching frequency is 400kHz and the internal system clock of each digital controller is 25 MHz. Using this system clock, the master module modulates the voltage error information into a pulse-width modulated signal switched at per-phase switching frequency. The relation between the pulse width and the voltage error signal can be freely set up in the “Encoder” block. All the slave modules receive the pulse-width modulated signal from the digital bus with a constant delay shorter than one switching period. Then, the pulse width information is demodulated to corresponding voltage information in the slave modules to achieve output voltage regulation. In each slave, demodulation is accomplished by measuring the pulse width using the module’s internal system clock.

In the application where no common Serial Clock signal is shared between the master and the slave modules, the internal system clocks among modules are asynchronous, and have clock frequency mismatches. The clock frequency mismatches are assumed to be such that the pulse width measurements on a slave module may have a ±1 LSB error as shown in Fig. 4. To account for this, a simple error correction provision is implemented based on encoding the voltage error signal before the pulse-width modulation operated by the master module. Since each code is assumed to be received with a maximum of ±1 LSB uncertainty, an encoding function is provided on the transmission side which ensures that two consecutive transmitted pulse-widths differ by at least 3 LSBs.

After measuring the received pulse width, the slave decoder simply rounds it to the closest nominal value; as exemplified in Table I for two consecutive values of $V_{\text{error}_m}$, this decision rule corrects any transmission errors and ensures that the transmitted pulse-widths always represent the same voltage error information in both master and slave modules.

<table>
<thead>
<tr>
<th>Voltage error on the master $V_{\text{error}_m}$</th>
<th>Encoded pulse width on the digital bus $E_{\text{codem}}$</th>
<th>Measured pulse width on slave $E_{\text{code}}$</th>
<th>Decoded voltage error $V_{\text{error}_s}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>23</td>
<td>22</td>
<td>0000</td>
</tr>
<tr>
<td>0001</td>
<td>26</td>
<td>25</td>
<td>0001</td>
</tr>
</tbody>
</table>

The system clock must be chosen to accommodate for the redundancy required by the foregoing error correction scheme. As an example, encoding of a 4-bit signal involves a minimum of 48 different codes. With a switching frequency of about 400 kHz, this sets a minimum clock frequency at 19.2 MHz, which is easily achievable in a digital controller. In the experimental prototype, a 25MHz clock is available in each module which allows accommodating all the encoded voltage information within three quarters of a switching period.

The maximum clock frequency mismatch that can be tolerated between the modules in order to maintain the assumed ±1 LSB maximum uncertainty in the measuring process is found as:
\[
\frac{\Delta f_{\Delta \Sigma}}{f_{clk}} \leq \frac{1}{\max(E_{\text{code}})}
\]  

A 48 values coding scheme can accommodate a ±2% frequency mismatch, which can be met by standard digital system clock oscillators.

Different pulse width coding methods could be designed to realize additional functions. In the design described above, the pulse width on the digital bus is between a minimum value greater than zero and a maximum value less than 100%. If the digital bus is always low or always high, the slave modules can take these cases as different fault conditions and select to use their local voltage error, disable current sharing loop or shut down the system. Furthermore, since the transmitted data is updated at the master phase switching frequency, the rising edge of the digital pulse on the bus can be used by the slave modules for synchronization and to generate the corresponding phase shift with respect to the master.

In addition to the voltage error transmission, the current data can also be transmitted in the same manner on the same wire by time multiplexing another pulse the width of which corresponds to the measured current value. As previously mentioned, the voltage error transmission can be accommodated in three quarters of the switching period, leaving the remaining quarter available for the current information.

Two pulses are therefore transmitted on the share bus wire per switching period, one pulse for the voltage error, and another pulse for the current data. Given the redundancy requirements of the proposed error correction scheme, one quarter of the switching cycle is not sufficient to host the 4-bit current information. However, the speed of the current sharing loop can typically be slower compared with the output voltage regulation loop. Therefore, the current data transmission can be spread over several switching cycles to improve the range and resolution of the transmitted data at the expense of increased delay in sharing the current information.

The master module current signal is split into 4 parts and transmitted in four consecutive switching periods. There are two ways to split the 4 bit current data:

1) The master could transmit one data bit per switching cycle from MSB to LSB, and the slaves could combine every 4 cycle data bits together in a 4-bit word, similar to what is done in standard serial communication protocols. A drawback of this approach is the need to identify a start bit and an ending bit in order to separate each data word.

2) As a second approach, which is adopted here, the 4 bit current data is transmitted as a 2 bit, \(\Delta \Sigma\)–modulated signal using a first order \(\Delta \Sigma\) modulator. Slave units perform a 4 cycle moving average filtering to decode the 4-bit current data. For example, transmission of the word \(I_{\text{master}} = 0001\) with a first order, 2-bit \(\Delta \Sigma\) modulation would produce the periodic sequence “00”, “00”, “00”, “01”. A slave module performs a 4 cycles moving average and obtains \(I_{\text{bus}} = (0000+0000+0000+0100)/4 = 0001 = I_{\text{master}}\). The system structure of the current signal communication on the digital bus is shown in Fig. 5.

![Fig. 5. Current data communication through the single-wire digital bus using \(\Delta \Sigma\) modulation](image)

With a 4 cycle moving average in the slave modules the transmitted signal passes through a low-pass filter and reaches the steady state value with a delay of 4 cycles. In steady state, the signal received by the slaves is exactly the same as the master module signal. However, during a transient, such as a step load transient, when the current signal measured by the master changes quickly, the decoding process using the moving average filter may result in more significant differences between the current \(I_{\text{master}}\) measured by the master and the current data \(I_{\text{bus}}\) received by the slaves. As an example, Fig. 6 shows the master module current \(I_{\text{master}}\) and current \(I_{\text{bus}}\) received by the slaves during a 2-4.5A load step transient. The decoded current signal \(I_{\text{bus}}\) in the slaves includes a non-monotonic behavior during the transient. Furthermore, due to the quantizer saturation in the sigma-delta modulator, without further complications in the implementation, the valid transmit range for a 4-bit current data is 0-12 instead of 0-15. For example, \(I_{\text{master}} = 1001\) and \(I_{\text{master}} = 1101\) would result in two different periodic

![Fig. 6. Current in the master module \(I_{\text{master}}\) and current \(I_{\text{bus}}\) received by the slave modules from the digital bus during a step load transient](image)
Fig. 7. Experimental waveforms with the voltage and current information shared on the single-wire digital bus in steady state (left) and during a 2-8A load transient (right).

Output voltage (AC coupled) [100mV/div]

Gate drive signal (master)

Gate drive signal (slave)

Digital share bus

High frequency internal system clock (master)

sequences, “10”, “10”, “10”, “11”, “11”, “11”, “00”, respectively, using a first order ΔΣ modulator, while the same current data \( I_{bus} = 1001 \) would be received by the slave modules after the moving average filter.

Fig. 7 shows steady state timing logic of a two phase buck showing interleaved operation and digital share bus waveform transmitting the voltage error and current data through the single wire digital bus.

The main disadvantage of the described single wire digital communication is that the resolutions of the transmitted signals are relatively low and limited by the length of the switching period and the frequency of the system clock. A low resolution window A/D for sensing both the output voltage and the inductor current is described in the next section.

IV. VOLTAGE ERROR AND CURRENT SENSING A/D CONVERTER

Per-phase voltage and current sensing (or estimation) can be implemented in a number of ways. In the experimental prototype, in order to minimize A/D converter hardware resources as well as the number of bits for the voltage error and current signals, both current and voltage are sensed through a single 4-bit window-flash A/D converter as shown in Fig. 8. The input of the window-flash A/D converter is connected to two sensing points \( V_{out} \) and \( V_{rsense} \) by an analog switch controlled by a digital control signal \( CLK \) switching 2 times per switching period. During the first half cycle of a switching period, the switch is connected to \( V_{rsense} \). During the second half cycle of the switching period, the switch is connected to \( V_{out} \) and the output voltage is sensed by the A/D converter. The output voltage error signal is obtained directly from the quantized \( V_{out} \) while the current information is calculated by subtracting the two ADC outputs, which gives a digital value proportional to the voltage drop on the sensing resistor \( R_{sense}i_{L} \). In the experimental prototype, the sensing resistance is 10 mΩ, and the A/D LSB resolution is 10 mV. As a result, the current sensing LSB resolution is 1 A.

Since the A/D converter is a 4-bit converter with 10 mV resolution, it can only sense the voltage within ±80 mV range around the reference voltage. The voltage on \( R_{sense} \) is always higher than the output voltage, and is proportional to the load current. With 80 mV A/D sensing range, the maximum sensed current is 8 A. The voltage control includes Adaptive Voltage Positioning (AVP) which, as shown in Fig. 9, further increases the current sensing range since the output voltage is regulated to a lower voltage in the A/D sensing range as the load current increases, leaving more headroom for the voltage sensing at \( V_{rsense} \). With digital implementation, the output voltage positioning can be achieved by adding the current signal on the voltage error as shown in Fig. 9. To eliminate the voltage sensing mismatch, the voltage error signal is transmitted and shared between the master module and slave modules as described in Section III. When AVP is implemented to increase the current sensing range, the voltage error signal including AVP in the master module is transmitted on the digital bus instead of using voltage error on the bus and local current signal to generate the voltage droop. This guarantees that the voltage loops in all modules are identical.
Fig. 10. 2-10 A step load transient in the experimental two-phase converter: (a) no current sharing and no AVP, and (b) active current sharing with AVP.

VI. CONCLUSIONS

This paper describes a distributed master-slave multiphase DC-DC converter architecture and related digital control and communication techniques. In the distributed master-slave multiphase architecture, all converter modules are identical, but one module operates as the master. The master module communicates its voltage error and current data over a single-wire serial bus to remove the voltage sensing mismatches and to accomplish active equal current sharing among the modules. Experimental results are shown for a 5 V-to-12 V input, 1.3 V, 0-20A output two-phase buck converter.

REFERENCES


