Abstract—Several designs for test techniques for fully differential circuits have recently been proposed. These techniques are based on the inherent data encoding, the fully differential analog code (FDAC), present in differential circuits. These techniques have not previously been verified experimentally. In this paper, we report results from a fabricated test chip which incorporates design for test structures. The test chip is a fully differential fifth-order filter, and was fabricated on a 2-μm CMOS process. The test techniques implemented are derived from a system-level technique developed earlier. The test chip contains fault injection circuitry to emulate faults. Our results demonstrate that the FDAC is a viable design for test technique for analog circuits.

I. INTRODUCTION

In analog IC's, high precision in signal measurement is a necessary prerequisite for test accuracy. Design for test techniques can be used to reduce the need for precision during test. Several such schemes have been developed for differential circuits. These schemes were first developed at the circuit level [1], [2] and later extended to the system level [3], [4]. The main contribution of this paper is the implementation of a low-overhead system-level design for test (DFT) technique for fully differential IC's. The methodology developed is applied to a fifth-order Butterworth filter. Our approach is based on a DFT technique developed by us [4]. Since our main goal was verifying the technique, our actual implementation differs in some respects from the methodology described in [4]. A test chip has been fabricated on a 2.0-μm, double-metal CMOS N-well process in order to experimentally verify the capabilities of this technique. Our results suggest that this technique is viable for practical use. A second benefit of fabrication is that the test chip can be used to validate the accuracy of simulation. This validation will give credence to fault coverages generated based exclusively on simulation.

This paper is organized as follows. Previous work on this topic is discussed in Section II. Section III discusses key issues in the development of checker circuits at the system level. In Section IV, we demonstrate the application of our technique through a design example. Section V provides a summary of the results obtained from the test chip. Section VI concludes this paper with an overview of the performance of our system-level scheme.
III. SYSTEM-LEVEL DESIGN FOR TEST

Consider a large fully differential switched capacitor circuit such as a multistage filter. It can be shown that placing a checker only at the filter's outputs is not sufficient to detect all target faults. Given a large circuit, we will present techniques to identify the number, location, and type of checkers required. We also discuss how the number of false flags, that is faulty units identified as good and vice-versa, can be reduced. Compared to previous checker designs, ours offer lower cost, an insignificant impact on performance, improved fault coverage, and can be used with both discrete and continuous time circuits.

A. Checker Location

Each stage in a filter consists of an op-amp and associated passive circuitry. Faults may occur in either the active or passive components. At a stage, single faults in the passive components will cause them to be asymmetric. This asymmetry will cause the common-mode (CM) signal at the input of the amplifier fed by the passive components to shift due to the action of the common-mode feedback circuit within the op-amp. Therefore, such faults can be detected by placing a checker at the input terminals of the op-amp. A number of faults within the amplifier can cause the CM circuitry to malfunction, producing FDAC errors at the op-amp outputs. It may not be necessary, however, to detect these faults using output checkers since the outputs of one filter stage are passed directly to the inputs of another stage. Input checkers in the following stage can detect the corruption. Therefore, it is possible to obtain adequate fault coverage for the entire filter circuit using checkers at op-amp inputs. However, nominal variations in the CM signal at the inputs are substantially larger than the nominal CM variations seen at the outputs. To avoid frequent false triggers, the threshold voltages of checkers at the inputs need to be larger than for those placed at the outputs of op-amps.

B. Parametric Variations

Large component variations and catastrophic faults are easier to detect because of the large resultant change in common-mode voltages. However, the probability of small component variations is substantially greater than catastrophic defects. Therefore, it is important to check for these smaller parametric faults as well. The smallest parametric fault detectable is constrained by the checker threshold voltage. However, the checker threshold voltage is limited by nominal variations in the common-mode voltage to prevent too many false triggers. The choice of checker threshold voltages will of necessity be circuit specific. Our checkers are designed to have variable thresholds that can be set for each application.

C. Matching and Phase

FDAC's rely heavily on well matched device pairs. Any mismatch results in the signals in a conjugate pair not being exact complements of each other. Component matching affects both the ac and dc characteristics of the circuit. Therefore, both the design and location of the checker need to consider device matching issues. Checkers that are placed away from the CUT are not likely to track due to normal process and temperature variations. Our checkers are designed to track the common-mode voltage over temperature and process by maintaining close proximity and a structure similar to the common-mode feedback circuitry of the op-amp. Additionally, the signal delay from the CUT to the checker should be minimized. Or else, the signal seen by the CUT and the checker may be out of phase. In [6] the authors use a roving programmable stage to provide data redundancy. The data output from the programmable filter and CUT are able to match to a large extent only because the components that set up the pole/zero frequencies use a common (common centroid) capacitor bank. This matching is also good only for low to medium frequencies when the parasitic layout capacitances are much smaller than the unit capacitors used to set the filter frequencies. This may render the technique unviable at higher frequencies.

D. Overhead

It is essential that any checker design minimize the overhead on area and performance. The naive placement and design of checkers can adversely impact performance. Any degradation of performance may be impossible to recuperate from. For example, in [9] and [3] the checker design uses an extra clock phase to measure the voltage difference between the two differential signals. To maintain the performance obtained before the introduction of DFT, the clock speed needs to be increased by 33%. Since the transconductance is only proportional to the square root of the current, it implies that regaining the 33% loss in speed requires a 150% increase in power. Consequently, the performance impact should be minimized by careful design and appropriate placement of the checker circuits. It has been shown that our FDAC checkers have less than 1% impact on all performance specifications other than area and power. Readers are referred to [11], [2], and [10] for more details on the impact of checkers.

The method used to sense the signal is also of interest. In a fully differential switched capacitor circuit, the change in the nominal common mode voltage can be sensed by using either transistors or capacitors. Generally, passive devices, which set circuit performance characteristics, are made large to minimize the effects of local variations. Due to the smaller size of active integrated components, active component-based checkers result in significantly lower area overhead than passive component-based checkers. Our checker designs use only active components.

The impact of a design for test technique on a circuit designer should also be considered in detail. Since the design of analog circuits is still largely manual, it is necessary to minimize the extra design effort needed to use checkers. As far as possible, checker designs should be invisible to the circuit designer. We have designed the checkers such that an original design without DFT capability can easily be converted by replacing all the regular op-amps with op-amps with checkers. Additionally, the same op-amps with checkers can be used for both continuous-time and sampled-data analog circuits.
IV. DESIGN EXAMPLE

We apply the techniques developed in Section III to a fully differential fifth-order “leapfrog” switched capacitor topology [11]. The circuit was designed as a Butterworth lowpass filter with a cutoff frequency of 3.4 kHz and a clock frequency of 256 kHz. The circuit operates from a ±2.5 V supply with $V_D$ set to 0 V. Fig. 1 shows the circuit diagram for the filter. For our analysis, we partition the faults in the circuit into two categories: faults within the operational amplifiers and faults in the remaining functional circuitry. It has been shown previously that faults internal to the op-amp can be detected [2]. Additionally, at the system level, chip area is dominated by passive components. Hence, we concentrate primarily on detecting faults external to the op-amps. We focus on faults in the switches and the capacitors between the op-amps. Before discussing our results, we develop some of the design constraints for the checker circuits. We start by introducing a fully differential switched capacitor integrator.

A. Switched-Capacitor Integrator

Each stage in a multistage filter can be modeled as a lossy integrator. We use an integrator stage to develop the design constraints for its simplicity. In the integrator in Fig. 2, capacitors $C_{F_1}$ and $C_{F_2}$ form the integrating capacitors and capacitors $C_1$ and $C_2$ form the sampling capacitors. The latter sample the differential input voltage during $\phi_2$ and transfer this charge onto the integrating capacitors during $\phi_1$. Fig. 2 also shows a simplified schematic for a fully differential amplifier. As with other fully differential amplifiers, a common-mode feedback circuit (CMF) sets the common-mode voltage at the inputs to the desired value. We focus on faults that occur in the capacitors and the associated switches. As an example, assume that one of the integrating capacitors $C_{F_1}$ is shorted. Assume that the input signal is completely differential, i.e., $(V_{in_+} + V_{in_-})/2 = V_B$, where $V_B$ is a constant bias voltage. Because of the fault, the two forward paths are not symmetrical. Therefore, for every input signal there is a momentary shift in the output common-mode voltage (OCMV). However, the common-mode feedback circuit quickly reacts to set the output common-mode voltage back to its desired value. To maintain a constant OCMV, it is forced to alter the common-mode voltage at the inputs, (ICMV), of the op-amp. Therefore, any fault that has asymmetrical impact on the two differential paths external to the op-amp causes a shift in the common mode voltage at the inputs to the op-amp. In [1] and [2] checkers were introduced only at the outputs of the op-amp to detect faults internal to the op-amp. However, to detect faults external to the op-amp, a checker, similar to those developed in [1] and [2], needs to be added to the inputs of the op-amp. Compared to the outputs, the nominal variations in the common mode voltage at the inputs is substantially larger. These variations in the ICMV result from clock feedthrough, nonlinearity in the common-mode feedback circuit, finite common-mode feedback gain, and offset voltages. To balance fault coverage and false flag requirements, the minimum trip voltages for the checkers at the op-amp inputs need to be larger than those placed at the outputs of an op-amp.

B. Modeling Filter Stages

Each stage of a switched capacitor filter can be modeled using the circuit shown in Fig. 3. In this figure, $F_{2_a}$ and $F_{2_b}$ model all the feedback paths around the op-amp and $F_{1_a}$ and $F_{1_b}$ model all the paths entering the stage. The change in the ICMV due to the external circuit is given by (1), $V_{DF} = V_{in_+} - V_{in_-}$ is the differential-mode input signal. In an ideal circuit the variation in the ICMV is zero. It is
clear from this equation that the variation in the ICMV is a function of the differential-mode input signal. To maximize the ICMV variation for a given filter stage, the differential-mode input signal should be maximized. However, the magnitude of the ICMV for a particular filter stage is a function of frequency. Furthermore, the signal appearing at the input to a filter stage depends on the internal transfer characteristics of the filter itself. For a specific filter stage, to maximize the ICMV variation, one must determine the frequency response of the ICMV signal (with respect to the input signal). In most cases, this can easily be accomplished through ac analysis of a continuous-time model or with the help of switched-capacitor simulator such as SWITCAP.

\[
\Delta V_{ICMV} = \frac{V_{1D}}{2} \left( \frac{F_{1a}F_{2b} - F_{1b}F_{2a}}{F_{1a}F_{2b} + 2F_{1a}F_{1b} + F_{1b}F_{2a}} \right). \tag{1}
\]

In general, the path blocks may actually consist of one or more capacitors in parallel, or one or more capacitive units in series. If a functional block consists of a single capacitor, a single short or open is a catastrophic fault for the block. If a functional block contains several parallel paths, an open in one of the paths is equivalent to a parametric variation in the path block characteristics. A short in any one of the parallel paths is a catastrophic fault. Conversely, in series paths a single short is equivalent to a parametric variation. An open in any capacitor is a catastrophic fault. As an example, in (2) we derive the maximum deviation in the ICMV due to a parametric variation in \(F_{2b}\). Here, \(\delta\) is the percentage variation in the path block impedance at a fixed frequency

\[
\Delta V_{ICMV} = \frac{V_{1D}}{2} \left[ \frac{F_{1}F_{2}(1 + \delta) - F_{1}F_{2}}{F_{1}F_{2}(1 + \delta) + 2F_{1}F_{2} + F_{1}F_{2}} + \frac{F_{2}}{F_{1} + F_{2}} \right]. \tag{2}
\]

Most switched-capacitor filters are designed such that the passband transfer function has a magnitude of one. Using this assumption, the maximum deviation in the ICMV is equal to \(V_{1D}/2 \times \delta/4 + \delta\). The magnitude of the error is dependent on the magnitude of the fault. Clearly, the minimum detectable deviation in the path block impedance depends on the trip voltage selected for the checker. The minimum trip voltage selected has to be larger than the nominal variation in the ICMV. The nominal variation in the ICMV is equal to

\[
\Delta V_{ICMV}^{\text{nominal}} = \Delta V_{CF} + \Delta V_{NL} + \Delta V_{OFF}.
\]

Here, \(\Delta V_{CF}\), and \(\Delta V_{NL}\) are the nominal variations in the common-mode voltage caused by clock feedthrough and the nonlinearity of the differential pair of the CMF circuit. \(\Delta V_{OFF}\) is the sum of the systematic and random offset voltages. For the fifth-order filter shown in Fig. 1, \(\Delta V_{ICMV}^{\text{nominal}}\) was estimated to be at most 15 mVp-p for a 2 Vp-p input signal. Setting the checker trip voltages to ±10 mV and using a 5 V supply we can detect a 10% deviation in the path block impedance at a fixed frequency. This constraint bounds the minimum parametric deviations that are detectable. In addition to the passive components, faults can also occur in the active components of the filter. A fault in an op-amp will corrupt the FDAC at the output of the op-amp. It would appear that each stage requires an input checker to detect faults in passive components, and an output checker to detect faults in its op-amp. However, the code corruptions caused by a fault inside an op-amp are also propagated to the inputs of an adjoining filter stage. Equation (3) describes the ICMV variation at the op-amp inputs in response to a common-mode variation at the inputs to a filter stage. \(\Delta V_{ICMV}\), is the common-mode voltage appearing at the inputs to the filter stage

\[
\Delta V_{ICMV} = V_{CM} \left[ \frac{F_{2}}{F_{1} + F_{2}} \right]. \tag{3}
\]

C. Input Checker Design

At each stage, input checkers are needed to monitor the ICMV, and detect significant variations in it. Our technique works as follows. At each op-amp, a measurement of the ICMV is generated locally. A pair of comparators is used to determine if the magnitude of the variation in the ICMV has exceeded a predetermined threshold. This scheme allows a pair of comparators to be shared among multiple op-amps through an analog multiplexer. This reduces the area and power overhead for the checker circuitry. For our test chip, threshold voltages for each comparator were set using off-chip reference voltages for easier evaluation. Alternatively, they can also be set internally using asymmetrical device sizes [2].

At each stage, the ICMV generator can be incorporated into the input differential pair of the op-amp. Fig. 4 shows how this can be accomplished. In a differential pair, the common source node \(V_{s}\) tracks the ICMV linearly, but is offset by the quiescent gate-to-source voltage drop across the input devices \(Q_{1}\) and \(Q_{2}\). To eliminate this offset, a third diode-connected NMOS transistor, \(Q_{3}\), is added to the differential pair and is biased with one-third of the tail current \(I_{t}\). A measurement of the ICMV is then available at the drain of transistor \(Q_{3}\). Since the differential pair transistors are typically made large for maximum gain and noise performance, this scheme can exact significant area and power penalties. This overhead can be reduced by decreasing the size of \(Q_{3}\) and scaling down its bias current by the same amount. In our checker, the width of \(Q_{3}\) is reduced by a factor of five as is its bias current with respect to each of the differential pair transistors. The resulting bias current for \(Q_{3}\) is \(I/11\). However, channel-length modulation has some detrimental effects on this design. The effects of channel-length modulation on the accuracy of the input checker shall be discussed further in the next section.
A. Fault List Generation

Typically, a fault list is generated from a circuit layout using a yield simulator [1], [2]. VLASIC, the yield simulator available to us, was written primarily for digital designs. This simulator did not recognize several layers used in analog designs. For this reason, we were forced to develop a fault list manually. Finite chip area places a restriction on the number of faults that can be injected. Faults can be injected into capacitors, interconnect, op-amps, and checkers. We have decided to make the number of faults injected in the various components proportional to the fraction of chip area occupied by them. The checker circuits occupy the smallest fraction of chip area. Additionally, because of its small size, injecting even a limited number of faults into the checker would have resulted in a significant increase in checker area. Therefore, we have decided to focus on injecting faults in the remaining three components. For details on coverage for checker faults estimated using simulation, readers are referred to [1], [2], and [10]. The coverage of checker faults, while high, is lower than the coverage for op-amp faults.

The fault list formation for the rest of the chip was guided by inspection of various circuit layouts. For example, in our design, approximately 75% of the area in the layout is consumed by capacitors. It is reasonable to assume that a large percentage of defects will occur in the capacitors. Faults produced by capacitor defects can be grouped into three categories: shorts, opens, and parametric variations. A short is often caused by an oxide pinhole between the two poly plates of a capacitor or by shorts between interconnect lines. Opens may occur due to mask errors resulting in missing contacts to the top or bottom plates. Parametric variations in capacitance values can result from changes in oxide thickness, etching errors, and broken interconnections between unit-size capacitors.

While the number of shorts and opens, i.e., catastrophic faults, is finite, the number of parametric faults is not. Consequently, catastrophic fault coverage can be quantified more precisely than parametric fault coverage. Secondly, the number of passive components is significantly less than the number of active components. Since this was a first experimental test chip, we chose to inject all possible capacitor catastrophic faults and distributed the remaining capability amongst other fault types. The final fault list consisted of all possible single-capacitor shorts and single-capacitor open faults. Additionally, six capacitor parametric faults of various magnitudes were added to the first filter stage. These parametric faults simulated +10%, +20%, and +30% variations in the values of the integrating capacitors C5 and C6. In addition to the capacitor faults, three internal op-amp faults and eight interconnect open faults were also included in the fault list.

B. Fault Injection Network

It is not feasible to intentionally introduce defects at the physical level during fabrication. We require a method to deliberately inject defects in our test chip. Faults can be injected using a switch-based injection network. Shorts between two circuit nodes can be introduced by placing a normally-open switch between the shorted nodes. When the fault is to be injected, the switch is closed. An open-circuit condition which splits a single node into two separate nodes can be achieved by inserting a normally-closed switch into the interconnect between the two nodes. Capacitor parametric faults which increase the value of a capacitor can be injected as follows.

A path which consists of a series combination of a switch and a capacitor is added in parallel to the target capacitor. The switch is closed when a fault is to be injected, and the value of the target capacitor is to be augmented. A capacitor parametric fault which increases the value of a capacitor can be implemented by adding a normally-closed switch in series with an error capacitor. Fig. 5 illustrates these fault switch configurations. NMOS devices, used as switches in realizing the functionality of the filter, were also used as switches for injecting faults into the circuit. To maintain symmetry, fault switches were duplicated on both differential signal paths though only one is activated during fault injection. All the fault injection switches are controlled using decoders.

C. Test Chip Results

The fifth-order filter test chip was fabricated on a 2.0-μm N-well, double-poly, low-noise analog process provided by MOSIS. The size of the die is approximately 4 mm². Fig. 6 shows a layout of the test chip. Each of the op-amps in the filter incorporates the ICMV generator discussed in Section IV. The outputs of these five ICMV generators are multiplexed to a pair of comparators whose thresholds can be set using off-chip voltages. The outputs of each ICMV generator can

Fig. 4. Input checker design.
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Fig. 5. Fault switch configurations.

Fig. 6. Layout of the test chip.

also be observed through a unity-gain buffer. For our test chip, two fault groups were established: one for normally-open fault injection switches (to inject shorts and capacitor parametric faults), and the second for normally-closed fault switches (to inject opens). Each group contains 31 different faults, addressable through a 5-to-32 decoder. Since the control lines for the fault injection switches carry static signals, these control lines can be routed in poly. This allows a large number of fault switches to be added to the circuit without excessive area overhead (approximately 3%) in routing switch control lines. The fault injection switches are distributed throughout the chip and introduce very little area overhead, less than 1%. The fault switch decoders are located near the top of the chip and at the bottom of the chip in Fig. 6. The area overhead of the fault switch decoder circuitry is approximately 12%. The total area overhead for fault injection is approximately 16%.

1) Input Checker Performance: Faults are detected by monitoring the ICMV at each op-amp. However, some design-related offset voltages were observed in the ICMV generators and common-mode feedback circuits. For the ICMV generators, the offsets tended to be fairly consistent. The largest factor contributing to the ICMV generator offset was channel-length modulation. Recall that in the discussion of the input checker design, the current scaling had to be adjusted somewhat to accommodate channel-length modulation effects. This adjustment was based on an estimate of the channel-length modulation parameter, \( \lambda \). However, this parameter varies from process to process. In our case, \( \lambda \) was smaller than expected. This resulted in the ICMV generator output being smaller than the actual ICMV by approximately 40 mV. An improved checker design which should track over process variations is shown in Fig. 7. This checker circuit utilizes negative feedback to generate the ICMV measurement. Although this scheme would require slightly more overhead, the ICMV measurement would be more reliable. The offset voltages in the common-mode feedback circuits were more random in nature. These offsets varied from \(-15 \) mV to \(+30 \) mV. Use of common-centroid geometry in the layout of the differential pairs and current mirrors could have greatly improved the performance of the common-mode feedback circuits. Device sizes in the common-mode feedback circuits were quite small, and therefore matching in these devices was marginal. Increasing these device sizes slightly would have also improved the performance of the common-mode feedback.

Despite the presence of these offset voltages, we were able to measure the offsets and compensate for them in the test chip. Since it was possible to observe the ICMV response in the fault-free circuit, threshold voltages for fault detection could be set relative to the fault-free ICMV response with an offset voltage. It is reasonable to expect that a significant portion of the observed offset voltages could be eliminated by using the improved input checker design and through the use of proper layout techniques. A certain degree of random offset can still be expected. However, this offset is not likely to exceed \( \pm 10 \) mV. In addition to offset voltages, the checker must reject nominal transient variations in the ICMV. This issue is addressed in more detail below.

2) Fault Coverage: A 2500-Hz, 1.4-V peak-to-peak differential sinusoidal input was used as a test input. The 2500 Hz signal was chosen since it lies within the passband of the filter. Table I shows the fault coverage results for the test chip at various checker thresholds. With \( \pm 10 \) mV thresholds, it was possible to detect all of the injected faults with the exception of the capacitor parametric faults. For catastrophic faults, the ICMV variation is usually large in the filter passband. For
### Table I
Fault Detection Data for the Test Chip

<table>
<thead>
<tr>
<th>Threshold Window</th>
<th>Cap Open</th>
<th>Cap Shorts</th>
<th>Parametric</th>
<th>Op Amp</th>
<th>Interconnect Open</th>
<th>All Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>±10 mV</td>
<td>22</td>
<td>6</td>
<td>3</td>
<td>8</td>
<td>57</td>
<td></td>
</tr>
<tr>
<td>±20 mV</td>
<td>20</td>
<td>6</td>
<td>3</td>
<td>8</td>
<td>53</td>
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</tr>
<tr>
<td>±30 mV</td>
<td>20</td>
<td>6</td>
<td>3</td>
<td>8</td>
<td>53</td>
<td></td>
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<tr>
<td>±40 mV</td>
<td>18</td>
<td>6</td>
<td>3</td>
<td>8</td>
<td>51</td>
<td></td>
</tr>
<tr>
<td>±50 mV</td>
<td>18</td>
<td>6</td>
<td>3</td>
<td>8</td>
<td>51</td>
<td></td>
</tr>
</tbody>
</table>

Faults Injected: 22, 22, 6, 3, 8, 61

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![Fault-free ICMV response](image1)

**Fig. 8.** Fault-free ICMV response.

![ICMV magnitude response to a parametric fault in C5](image2)

**Fig. 9.** ICMV response to a short in C6.

The checker threshold voltages in Table I range from ±10 mV to ±50 mV. Transient variations in the ICMV will not trigger the checker at any thresholds. It is possible that random offset voltages could trigger checkers at low thresholds. In a well designed common-centroid layout such random offset voltages may be as large as 10 mV. However, it is not possible to assess the effects of random offsets with such a small sample size. Parametric fault coverage is more sensitive to variations in the checker thresholds. In the next section we discuss the detection of parametric faults.

#### 3) Parametric Fault Detection

The variation in the ICMV response to a parametric fault is more sensitive to the frequency content of the input excitation than for catastrophic faults. Special care is required to select an input which excites and detects a target fault. A test stimulus which targets a particular parametric fault can be found by simulating the ICMV frequency response in the presence of the fault. The parametric faults that were injected did not cause large excursions in the ICMV. For the +30% parametric fault in the integrating capacitor of the first stage, for example, we simulated the ICMV frequency response using a continuous-time model. These simulation results agreed well with experimental results. The frequency response curve is shown in Fig. 10.

Using this technique, we noticed that a peak in the ICMV frequency response occurred at around 12.5 kHz. However, for a 1.4 V\(p-p\) differential input sinusoid, the magnitude of this peak is only marginally sufficient to trigger the input checker. Instead of using a sinusoidal input, one may instead choose a square wave excitation which allows the harmonic contributions to push the magnitude of the ICMV well past the checker threshold. Using a 7500 Hz square wave, for example, it is possible to detect the two +30% parametric faults in the first filter stage using ±10 mV thresholds. Fig. 11 shows the ICMV response of the first filter stage to this fault using the 7500 Hz square wave excitation. A 2500-Hz sinusoidal input is within...
the passband of the filter, so the gains on both paths will be almost identical. A 7500-Hz square wave input concentrates the energy in the stopband of the filter where the difference in the two pole frequencies results in different signal gains.

D. Extension of Experimental Results

Since the total number of faults that could be injected was limited, we have attempted to provide additional fault coverage information via simulation. The measured performance of our test chip matched simulated performance very closely. This was true both during normal operation and under fault injection. Hence it is reasonable to use simulation to predict coverage for faults not emulated in hardware. The consistency between simulation results and test chip measurement is demonstrated in Figs. 11 and 12. In Fig. 11, an oscilloscope trace of the ICMV waveform is shown for a ±30% parametric fault in the first filter stage of the test chip. Fig. 12 shows the ICMV waveform resulting from a simulation of the same fault. The two waveforms are virtually identical. In both traces the ICMV variation is approximately 50 mV. The simulated and actual responses were compared for several other faulty and fault-free circuits. In all cases there was close agreement between them.

Given the close correlation, we have predicted fault coverages for other capacitor parametric faults using fault simulation. The results of these simulations are summarized in Table II. These simulations assume the checker thresholds are set at ±10 mV. Since the circuit is symmetric, a parametric fault in a capacitor on one of the differential signal paths is equivalent to the same parametric fault in the capacitor on the other differential signal path. The reader may note that positive and negative parametric variations are not equally detectable. This can be explained as follows. A fault which increases the gain through a particular filter stage is more easily detected than a fault that decreases the gain through that filter stage. For example, capacitors C17 and C18 are integrating capacitors in the fourth filter stage. Increasing the value of one of these capacitors decreases the overall gain of the fourth filter stage slightly. Therefore, these parametric faults are harder to detect than parametric faults which decrease the capacitance values. The paper concludes in the next section with a summary of our results.

VI. CONCLUSIONS

In this paper, we have implemented a system-level DFT technique for fully differential circuits. This work extends a DFT technique previously presented at the circuit level to the system level. The technique implemented is derived from a system-level DFT technique reported earlier [4]. The error detection scheme exploits the inherent encoding in fully differential circuits, the FDAC. Additional considerations for an analog system-level DFT technique, such as device and switching noise and device matching for example, were identified. The system level technique is based on using multiple code checkers at several points in a fully differential circuit. A test chip, a fifth-order Butterworth switched-capacitor filter, which implemented this technique was fabricated on a 2-μm double-poly N-well CMOS process. The test chip incorporated circuitry which enabled 61 single faults to be injected. Both catastrophic and parametric faults were included in the test chip. Experimental fault detection data indicates that this technique is effective at detecting both types of faults. Simulation data, validated by experiments, was used to verify the coverage for faults not injected in hardware. To the best of the authors' knowledge, this technique has not previously been verified practically through fabrication.
REFERENCES


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