High Speed Integrated Circuit Design

Frank Ellinger
Chair for Circuit Design and Network Theory
Outline

1. Adaptive antenna combining IC systems
2. Smart power amplifier IC systems
3. Local positioning RFICs and systems
4. High speed 60 GHz WLAN
5. High speed optical ICs
6. Beyond Moore nano-electronic circuit design
7. Some facts
8. Conclusions
1. Adaptive Antenna Combining in RF

**Pros**

- ☺ Only 1 IF/BB path
  ⇒ small size, power consumption and costs
- ☻ Easy system extension
- ☺ Interferer cancelled prior to ADC
  ⇒ Relaxed specs for ADC

**Challenges**

- ☹ Precise, compact, low-cost *analogue* phase & gain control ICs

**Avoid complex recursive adjustment:**

- ⇒ *Phase* control with min. impact on *gain*
- ⇒ *Gain* control with min. impact on *phase*

*(focus of this talk)*
Example for Architecture

- EU funded project MIMAX
- Coordinated by our chair
- 802.11a (C-band)
Example for a RX SoC Implementation

- 4 x adaptive signal branches from RF down to baseband interface
- Including digital circuits for amplitude and phase control
- Low cost 250nm IHP CMOS
- $P_{DC} \approx 3.3\text{V}, 130\text{mA}$

© Rohde & Schwarz
EEEfCom Innovation Award 2009
2. Class-F CMOS Power Amplifier for WPAN/LAN

**Input Matching, Bias**
- $V_{gs}$
- $10pF$
- $10pF$
- $9\Omega$
- $942pH$
- $3.4pF$
- $542pH$
- $1.66m$

**Output Matching, Filter**
- $V_{dd}$
- $10pF$
- $774pH$
- $4.9pF$
- $4.34pF$
- $54pH$
- $180fF$
- $L1$
- $L2$
- $L3$
- $534pH$
- $723pH$
- $534pH$
- $723pH$

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech.</th>
<th>$f$</th>
<th>$V_{DD}$</th>
<th>$S_{21}$</th>
<th>$P_{1dB}$</th>
<th>Eff. @ $P_{1dB}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>0.18 CMOS</td>
<td>5.6GHz</td>
<td>1.9V</td>
<td>10dB</td>
<td>18.4dBm</td>
<td>50%</td>
</tr>
<tr>
<td>Biondi, RFIC 03</td>
<td>BiCMOS</td>
<td>5.2GHz</td>
<td>2.7V</td>
<td>13dB</td>
<td>18.2dBm</td>
<td>50%</td>
</tr>
</tbody>
</table>

Adaptive PA Power Control

- BMBF projects CoolRepeater and CoolBaseStations & internal
- PAs have max. efficiency ($P_{RF}/P_{dc}$) only in saturation (at full output power)
- Back-off = $P_{out,sat}/P_{out}$ typically around 20dB, e.g. if terminal close to BS
- Back-off $\rightarrow$ 1 e.g. by adaptively decreasing DC supply voltage
- Transistor always in saturation where max efficiency possible
Control Methods

Envelope tracking

- Power known in baseband (BB)
- Slow dynamics due to delays between BB ⇔ PA
- Moderate efficiency improvement possible
- Demonstrated for GSM

Envelope following

- Supply voltage directly follows envelope
- Higher efficiency improvement possible
- Very fast control dynamics required
- Full control in analogue to maximize speed & BW
- No baseband connection required
Envelope Following

- Efficiency improvement depends on required dynamics/BW of standard
- CMOS losses considered
- SOA: dc generation by buck converter & saw tooth generator
- Slow/lossy since periodic control over full duty cycle (several periods)

Integrated Control System

- No limiting conventional buck c. & saw tooth
- Fast since *non-periodic*, goal-oriented control
- Integrated in 0.18 μm CMOS (7WL)
- Excl. PA and LC LP
- $V_{DC}$ and $I_{DC}$ up to 3.3 V and 280 mA
- **Efficiency enhancement of UMTS** class-AB PA systems with factor > 2 over average back-off

F. Haßler (CCN), internal report, publication pending
3. Local Positioning based on FMCW Radar

Reconfigurable Systems for Mobile Local Communication and Positioning

CCN:
- Coordination
- 5.8GHz 7WL RF transmitter/PA design
- 24GHz 7WL fractional-n synthesizer

Smart Factories

- **SIEMENS**
- 3-D accuracy <10cm
- Coverage up to 100m
- Real time < 0.1 s
- AGV
- Localisation of all supplies and tools
- Optimisation of material flow and management
- Reduced fabrication time, storage area, fabrication costs
- Market > 50 Mio. €
Interactive Guiding

National archaeological museum of Athens

- 3-D accuracy <30cm
- Coverage up to 100m
- Real-time based active mapping for advanced sightseeing in museums, shopping malls, amusement parks, etc.
- Location dependent actions increase amusement factor
- Assistant living and guiding
# 2-D Measurements (3-D similar)

![Image](image_url)  

**Xenia Forum at Siemens**

<table>
<thead>
<tr>
<th></th>
<th>RESOLUTION</th>
<th>UWB</th>
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</thead>
<tbody>
<tr>
<td><strong>Verified coverage</strong></td>
<td>800m²</td>
<td>« 400m²</td>
</tr>
<tr>
<td><strong>Accuracy</strong></td>
<td>4cm* - 18cm</td>
<td>15-30cm</td>
</tr>
<tr>
<td><strong>Bandwidth</strong></td>
<td>&lt; 150 MHz</td>
<td>1600 MHz</td>
</tr>
<tr>
<td><strong>EIRP</strong></td>
<td>&lt; 14dBm</td>
<td>&lt; -12dBm</td>
</tr>
</tbody>
</table>

* Anechoic chamber  ** Ubisense product  *** EU decision

⇒ **FMCW competitive approach**, e.g. compared to UWB

F. Ellinger et. al., EU Project RESOLUTION-Local Positioning Systems based on Novel FMCW Radar, *IEEE IMOC 2007*
4. WLAN Data Speed Roadmap

60 GHz SiGe Power Amplifier

M. Hellfeld and F. Ellinger, “Universal Millimeter Wave Power Amplifier Design Method verified at 60 GHz in SiGe”, submitted to IET Journal on Circuits, Devices and Systems
### 60 GHz SiGe VGLNA

**Overview of Recent V- and W-Band LNA Designs**

<table>
<thead>
<tr>
<th></th>
<th>This work</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
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<tbody>
<tr>
<td>Process $f_T$ /</td>
<td>190 GHz /</td>
<td>180 GHz /</td>
<td>190 GHz /</td>
<td>200 GHz /</td>
<td>200 GHz /</td>
<td>200 GHz /</td>
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<tr>
<td>active devices</td>
<td>SiGe-HBTs</td>
<td>SiGe-HBTs</td>
<td>SiGe-HBTs</td>
<td>SiGe-HBTs</td>
<td>SiGe-HBTs</td>
<td>SiGe-HBTs</td>
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<tr>
<td>Peak gain frequency $f_0$</td>
<td>63.5 GHz</td>
<td>60 GHz</td>
<td>79 GHz</td>
<td>59 GHz</td>
<td>61.5 GHz</td>
<td>79 GHz</td>
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<tr>
<td>$</td>
<td>S_{21}</td>
<td>$ at $f_0$</td>
<td>21.4 dB</td>
<td>18 dB</td>
<td>16 dB</td>
<td>14.5 dB</td>
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<td>$NF$ at $f_0$</td>
<td>6.0 dB</td>
<td>6.8 dB</td>
<td>n/a</td>
<td>5 dB</td>
<td>4.5 dB</td>
<td>10.2 dB</td>
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<tr>
<td>DC power</td>
<td>7.3 mW</td>
<td>66 mW</td>
<td>90 mW</td>
<td>8.1 mW</td>
<td>10.8 mW</td>
<td>105 mW</td>
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<tr>
<td>Remarks</td>
<td>variable gain</td>
<td>differential</td>
<td>differential</td>
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<td></td>
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</tr>
</tbody>
</table>

Highest gain vs dc power in silicon

60 GHz SiGe VCO

Lowest phase noise with such a wide frequency tuning range in Silicon

A. Barghouthi, F. Ellinger et. al, “Design of a 54 to 63 GHz Differential Common Collector SiGe Colpitts VCO”, International Conf. on Microwaves, Radar, and Wireless Communications, 2010
5. High Speed ICs for Optical Communication

Transmitter

Laserdiode

LWL

Photodiode

TIA

LA

CDR

DEMUX

Receiver
SiGe Broadband Amplifier for 80 Gb/s

State-of-the-Art T-Coil Peaking
- 30-50% BW enhancement
- Limitation by $S_{22}$ degradation

Our Novel Approach
- 200% BW enhancement
- Much less $S_{22}$ degradation


SiGe Broadband Amplifier for 80 Gb/s

Transmission Gain

50 Ω Output Matching

Measurement at 55 G/s
- highest rate of our test set
- Simulation up to 80 GB/s

Comparison with State of the Art SiGe Amps

<table>
<thead>
<tr>
<th>Reference</th>
<th>Small-Signal Bandwidth GHz</th>
<th>Single-Ended Gain dB</th>
<th>Gain Ripple dB</th>
<th>Output Matching dB</th>
<th>Supply Voltage V</th>
<th>Output Swing mV</th>
<th>DC Power mW</th>
<th>Technology</th>
<th>Output Stage Configuration</th>
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<tbody>
<tr>
<td>[12]</td>
<td>80</td>
<td>7</td>
<td>6.2</td>
<td>-6</td>
<td>5.5</td>
<td>N/A</td>
<td>500</td>
<td>N/A / &gt;200 GHz</td>
<td>Cascade</td>
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<td>[13]</td>
<td>62</td>
<td>-1</td>
<td>4.5</td>
<td>N/A</td>
<td>2.5</td>
<td>300</td>
<td>125</td>
<td>0.12μm / 200 GHz</td>
<td>Shunt Peaking</td>
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<tr>
<td>[14]</td>
<td>84</td>
<td>14</td>
<td>4.9</td>
<td>-6</td>
<td>5.5</td>
<td>1300</td>
<td>990</td>
<td>0.18μm / 250 GHz</td>
<td>Buffered Cascade</td>
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<tr>
<td>[15]</td>
<td>102</td>
<td>10</td>
<td>1.5</td>
<td>-8</td>
<td>2</td>
<td>N/A</td>
<td>73</td>
<td>0.12μm / 200 GHz</td>
<td>Distributed Amplifier</td>
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<tr>
<td>This work</td>
<td>69</td>
<td>10.5</td>
<td>1.5</td>
<td>-15</td>
<td>2.9</td>
<td>300</td>
<td>74</td>
<td>0.25μm / 180 GHz</td>
<td>Modified T-coil peaking</td>
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40 Gb/s SiGe TIA

<table>
<thead>
<tr>
<th>Reference</th>
<th>Tech</th>
<th>$Z_t/\Omega$</th>
<th>B/GHz</th>
<th>$I_{n,in}/\text{pA/}\sqrt{\text{Hz}}$</th>
<th>$P/\text{mW}$</th>
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<tbody>
<tr>
<td>Jin, JSSC 08</td>
<td>CMOS</td>
<td>350</td>
<td>31</td>
<td>$&lt;55.7$</td>
<td>60</td>
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<td>Weiner, JSSC 03</td>
<td>BiCMOS</td>
<td>140</td>
<td>50.0</td>
<td>$&lt;30$</td>
<td>200</td>
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<tr>
<td>This work</td>
<td>BiCMOS</td>
<td>4500</td>
<td>30</td>
<td>$&lt;25$</td>
<td>32</td>
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</tbody>
</table>

40+ Gb/s Laser Driver

**Comparison to State-of-the-Art Laser/Modulator Drivers in SiGe**

<table>
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<tr>
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<th></th>
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</thead>
<tbody>
<tr>
<td>[3]</td>
<td>40</td>
<td>n/a</td>
<td>1</td>
<td>4/5</td>
<td>2000</td>
<td>74 GHz</td>
<td>No peaking</td>
</tr>
<tr>
<td>[4]</td>
<td>40</td>
<td>22</td>
<td>2.4</td>
<td>8</td>
<td>3600</td>
<td>BiCMOS 75GHz</td>
<td>Distributed amplifier</td>
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<tr>
<td>[5]</td>
<td>40</td>
<td>22</td>
<td>0.1</td>
<td>2.2</td>
<td>190</td>
<td>0.18µm BiCMOS</td>
<td>Distributed amplifier</td>
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<tr>
<td>[6]</td>
<td>40</td>
<td>32</td>
<td>1.6</td>
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<td>900</td>
<td>HBT 80GHz</td>
<td>Inductive peaking</td>
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<tr>
<td>[7]</td>
<td>12.5</td>
<td>11.2</td>
<td>0.44</td>
<td>1</td>
<td>30</td>
<td>90nm CMOS</td>
<td>No peaking</td>
</tr>
<tr>
<td>[8]</td>
<td>40</td>
<td>24</td>
<td>0.44</td>
<td>1</td>
<td>30</td>
<td>90nm CMOS</td>
<td>Inductive peaking</td>
</tr>
<tr>
<td>This Work</td>
<td>40+</td>
<td>26</td>
<td>0.6</td>
<td>2.2</td>
<td>80</td>
<td>BiCMOS 180GHz</td>
<td>Positive feedback</td>
</tr>
</tbody>
</table>

40 Gb/s Modulator Driver with Breakdown Voltage Doubler

C. Knochenhauer, C. Scheytt, F. Ellinger, “A Compact, Low-Power 40 Gbit/s Modulator Driver with 6 V Output Swing in SiGe BiCMOS, to be submitted to IEEE JSSC
7. Beyond Moore Circuit Design

*Scaling is already dead but nobody noticed it had stopped breathing and its lips had turned blue*

B. Meyerson, IBM CTO, 2003

⇒ **Circuit R&D on** “Beyond Moore” technologies started, e.g.:

- CNT (simulation of CNT RF amplifier)
- Organic/printed (simulation of organic audio amplifier)
- Silicon Nano Wire (project proposal)
8. Conclusions

- **Core competence CCN:** High-speed and low power consuming analogue/RF ICs and systems
- Complete RFIC frontends and interfaces
- Rigorously optimized circuit blocks: PAs, LNAs, mixers, VCOs, synthesizers, DC/DC converters, TIAs, drivers, (ADC/DAC), etc.
- **Specific research areas:**
  - Adaptive antenna combining, RF MIMO and beamforming
  - Smart power amplifiers with high efficiency
  - Local positioning sensors based on FMCW radar
  - RFIC development 100 MHz - 220 GHz, up to 10 Gb/s
  - High speed ICs for optical data communication up to 80 Gb/s
  - Beyond Moore nano electronic circuit design (started)
Radio Frequency Integrated Circuits and Technologies

Frank Ellinger

The operation frequencies, bandwidths and data capacities of communications systems are continuously increasing by employing advanced technologies and aggressive scaling of device dimensions. However, the restrictions inherent in scaling make the design of radio frequency integrated circuits a demanding task. To meet the corresponding challenges designers must provide profound skills in several areas including circuit theory, silicon and compound semiconductor technologies, communications standards, system design, measurement techniques, etc. The book aims at addressing all these multidisciplinary issues in a compact and comprehensive form and in a single volume. Suitable for students, engineers and scientists, the manuscript offers the necessary theoretical background together with cookbook-like optimisation strategies and state-of-the-art design examples.
Dresden University of Technology
thanks you for your attention!

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