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Research Article

The Investigation of Field Plate Design in 500 V High Voltage NLDMOS

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This paper presents a 500 V high voltage NLDMOS with breakdown voltage (V_{BD}) improved by field plate technology. Effect of metal field plate (MFP) and polysilicon field plate (PFP) on breakdown voltage improvement of high voltage NLDMOS is studied. The coeffect of MFP and PFP on drain side has also been investigated. A 500 V NLDMOS is demonstrated with a 37 μm drift length and optimized MFP and PFP design. Finally the breakdown voltage 590 V and excellent on-resistance performance (R_{sp} = 7.88 ohm $*$ mm^2) are achieved.

1. Introduction

For the high voltage NLDMOS in BCD (Bipolar, CMOS, and DMOS) platform implicated in 500 V and even higher voltage, RESURF (reduced surface field) technology has been widely adopted [1, 2]. The major purpose of this method is to increase the breakdown voltage (V_{BD}) and improve the on resistance (R_{sp}) of NLDMOS through the reduction of the surface electric field of drift region. It not only helps to reduce the NLDMOS device size and R_{sp}, but also can meet breakdown requirement. For NLDMOS, one well-known technical approach is to introduce a p-type doped layer into n-type doped drift region and then realize the double RESURF or triple RESURF effect [3, 4]. This approach also has been extensively studied by many researchers [5, 6].

MFP or gate shield (Gshield) is a common method employed in RFLDMOS. One or two (even three) metal field plates cover on gate and part of adjacent drift region [7]. The function of this Gshield is to shield the impact from drain and reduce the miller capacitance, which is the feedback capacitance between gate and drain (C_{ds}). It improves the frequency characteristics of RFLDMOS and extends the application to higher frequency [8]. This metal field plate will change the electric field distribution of drift region and affect the breakdown voltage of the device.

In the published research results for 500 V and higher voltage NLDMOS, some researches refer to the devices structure with field plate [9–11]. However, in-depth study of metal and polysilicon field plate on such high voltage NLDMOS is still needed for further investigation. This paper presents a detailed study of MFP and PFP and their effect on 500 V high voltage NLDMOS. A 500 V NLDMOS optimized by MFP and PFP design has been demonstrated with smaller drift size and higher enough breakdown voltage. This research result also can be adopted as a good reference for other high voltage NLDMOS developments.

2. Device Structure

The schematic cross section of 500 V NLDMOS device is showed in Figure 1. When drain terminal is biased at operation voltage (V_{dd}), the voltage sustained in lateral direction and vertical direction is the same. The breakdown voltage of both directions needs to be higher than the operation voltage and at least has 10% margin. Figure 1 shows that the drift region of NLDMOS embraces deep n-type well (DNW) and p-type buried layer (PBL). The voltage drop of V_{dd} in the vertical direction mostly is allocated to the PN diode formed by DNW and p-type substrate (PSUB). Its breakdown

Table 1: Key reference sizes of this NLDMOS.

Item	Description	Size
PFP1	Polysilicon field plate, source side	7
PFP2	Polysilicon field plate, drain side	10
MFP1	Metal field plate, source side	22
MFP2	Metal field plate, middle	3
MFP3	Metal field plate, drain side	25
$E1$	MFP3 extending PFP2 (left side)	8

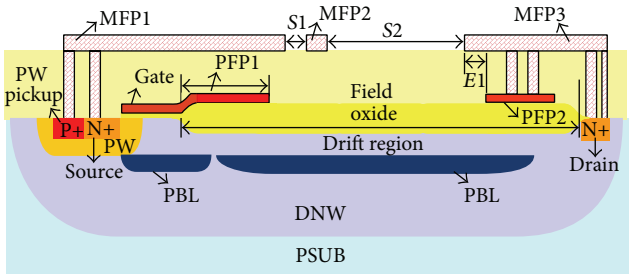

Figure 1: Schematic cross section of high voltage NLDMOS.

is higher than 1000 V and can be used in the application of 500 V NLDMOS. The drift region with DNW and PBL is designed considering RESURF effect. Drift region is fully depleted and sustains the lateral voltage when drain is biased. The doping condition of the drift region is determinate due to the technology platform and will not be discussed here. P-type well (PW) and p-type heavily doped region (P+) form the channel region. N-type heavily doped region (N+) forms the source and drain. Above the silicon, there are polygate, polysilicon field plate 1 (PFP1, close to source side), polysilicon field plate 2 (PFP2, close to drain side), metal field plate 1 (MFP1, source side), metal field plate 2 (MFP2, middle), and metal field plate 3 (MFP3, drain side). $S1$ is the space between MFP1 and MFP2. $S2$ is the space of MFP2 and MFP3. $E1$ represents the extension size of MFP3 over PFP2.

The effect of metal filed plate and polysilicon field plate on high voltage NLDMOS is investigated in this paper. Table 1 summarizes the key reference sizes of the device in Figure 1, which is a high voltage NLDMOS with V_{BD} = 772 V and drift region length = 67 μm.

The depth of DNW is 8 μm and the thickness of gate oxide is 43 nm. The field oxide thickness of PFP and MFP is 630 nm and 1 μm, respectively.

3. Experiment Results and Discussion

The breakdown voltage of high voltage device depends on the length of drift region if the drift region can be fully depleted. When the bias voltage of drain keeps on a rise, the electric field intensity will reach the critical value of silicon (E_c) and device breakdown occurs. Field plate does not change the critical electric field of silicon but reduces the peak value of electric field at a certain bias of drain and thus improves the device breakdown voltage. In an ideal case, when the device breaks down at off-state, the surface electric field is lower than E_c, which means the breakdown happens in the internal region of drift instead of on the surface of silicon. The breakdown of NLDMOS with field plate may not really occur in the internal region of drift, but the field plate can help to move the breakdown point away from the weak gate oxide region to field plate edge.

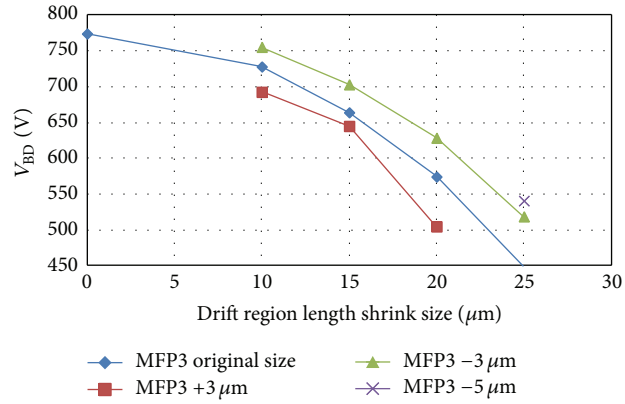

Figure 2: Breakdown voltage related to different drift length.

With the aid of process and device TCAD software, the different MFP and PFP designs and their effects on the breakdown voltage of 500 V NLDMOS have been simulated. The effect of different drift lengths also has been studied. In order to get a 500 V NLDMOS with shortest drift length and without scarifying breakdown voltage, the breakdown voltage drop caused by drift length shortening needs to be compensated by a dedicated field plate design.

Finally, a 500 V NLDMOS with small size and high breakdown voltage is obtained. The experiment result got from silicon matches the simulation data well and proves the correctness of study in this paper. This demonstrated 500 V high voltage NLDMOS meets the application requirement (higher than the 550 V, as least 10% tolerance) and shows excellent on-resistance performance.

4. The Impact of Metal Field Plate on Breakdown Voltage of NLDMOS

4.1. Effect of Metal Field Plate (Drain Side, MFP3) on V_{BD}. Figure 2 shows how the breakdown voltage changes NLDMOS as drift length shrinks at different MFP3 sizes. In this figure, the drift length shrink means shorter drift length. The reduction of MFP3 size means the increase of space $S2$ between MFP2 and MFP3. With the same MFP3, the breakdown voltage drops as drift region becomes shorter. When drift length shrinks 10 μm, the breakdown voltage drops from 774 V to 728 V and decreases by 46 V. If the drift length is determined, the breakdown voltage increases with smaller MFP3 size. When MFP3 is shortened by 3 μm, the breakdown voltage has an increase of 39 V and 51 V, respectively, for drift length reduction of 15 μm and 20 μm. It reveals that the breakdown voltage can be improved more effectively by MFP3 with shorter drift length.

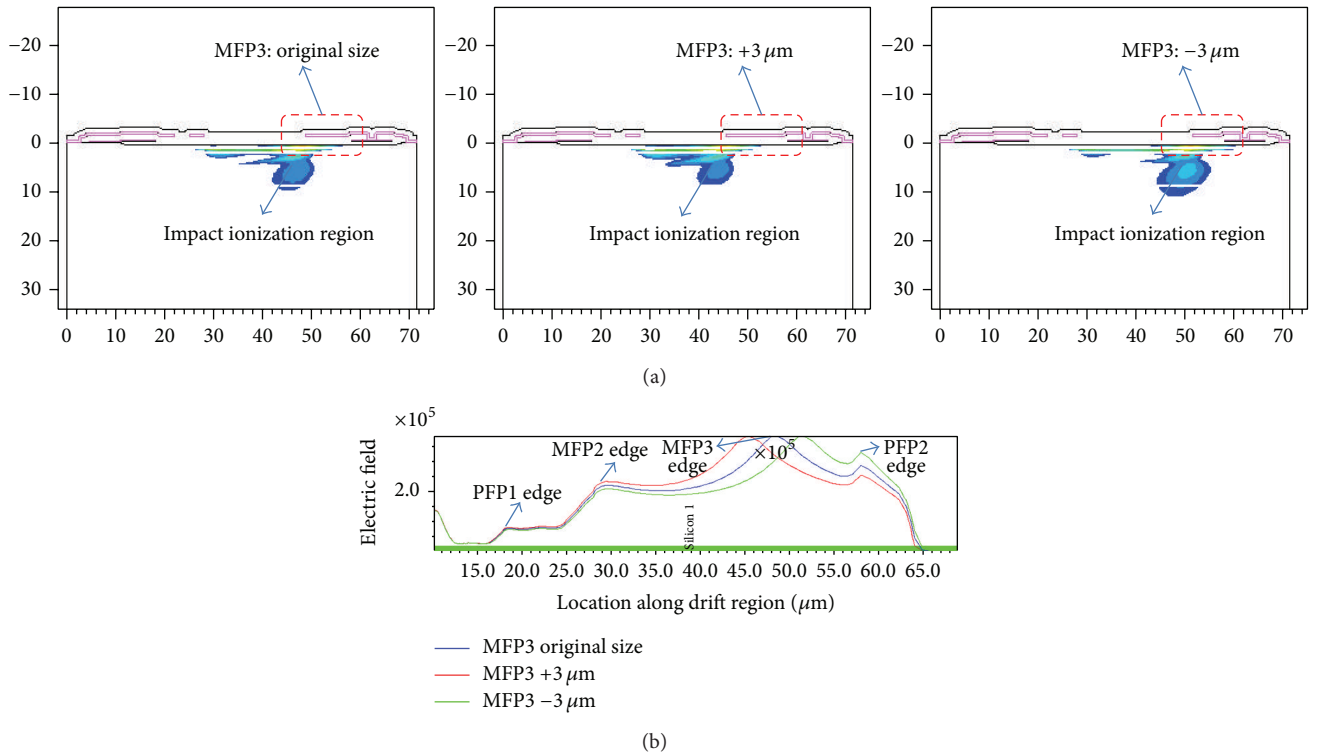

FIGURE 3: (a) Simulated impact ionization at breakdown voltage; (b) lateral electric field distribution of drift region from source to drain.

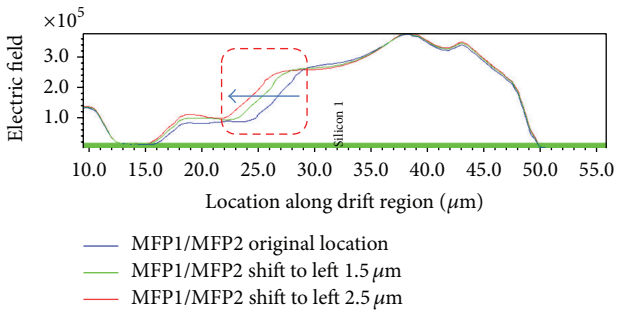

FIGURE 4: Lateral electric field distribution of different MFP2 location.

Figure 3(a) gives the impact ionization intensity pictures of 3 different MFP3 conditions: the length is changed 0 μm, +3 μm, and −3 μm. Based on the location of impact ionization, breakdown occurs at surface of drift region close to the left edge of MFP3. Figure 3(b) presents the lateral electric field distribution in the drift region from source to drain. It shows the electric field peaks locate at the right side edge of MFP2, the left side edges of MFP3 and PFP2. The highest one is peak at MFP3 edge and the breakdown also happens in this location. The electric field peak shifts to the drain side and breakdown voltage becomes higher when MFP3 size is reduced.

4.2. Effect of Metal Field Plate Location (Source Side) on V_{BD}. Figure 4 shows the simulation result of lateral electric field distribution with different MFP2 and MFP1 locations while keeping MFP3 size and space of MFP1 and MFP2 (*S*1) unchanged. According to the lateral electric field distribution shown in Figure 4, the electric field peak close to MFP2 right edge shifts to the left side as MFP1 and MFP2 shift to the left. Breakdown voltage increases by 44 V when the location changes by 2.5 μm. This reveals that the MFP2 location has effective impact on NLDMOS breakdown voltage. MFP2 moving to the left side helps to raise the breakdown voltage of the device.

TABLE 2: V_{BD} of different PFP1 experiment.

PFP size experiment	V_{BD}
0	728
PFP1 −2 μm	728.1
PFP1 +2 μm	727.1

5. The Impact of Polyfield Plate on the Breakdown Voltage of NLDMOS

Table 2 gives the simulation results of breakdown voltage for device with different PFP1 sizes. It shows that different PFP1 sizes have no obvious effect on breakdown voltage. The change of V_{BD} is less than 1 V when PFP1 increases or decreases by 2 μm.

Figure 5 is the lateral electric field distribution of PFP1 experiment. It shows the location of related electric field peak

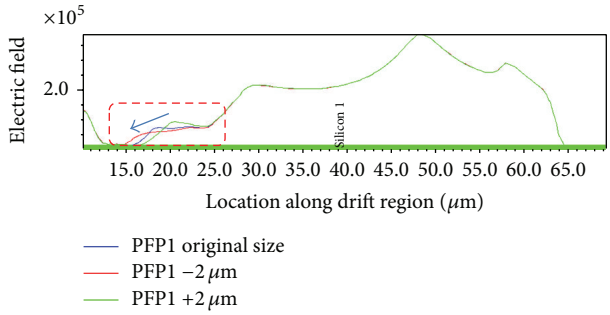

FIGURE 5: Lateral electric field distribution of different PFP1 size.

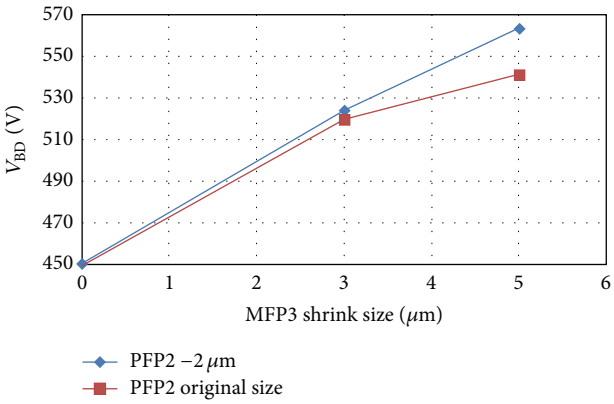

FIGURE 6: NLDMOS breakdown voltage related to MFP3 reducing sizes for different PFP2 length.

will shift as PFP1 edge location changes. The peak value in the left side is smaller than the right side.

6. Coeffect of Metal Field Gate (MFP3) and Polyfield Gate (PFP2) on the Breakdown Voltage of NLDMOS

From the above analysis, device with shorter MFP length shows higher breakdown voltage. Figure 6 tells that, at different PFP2 sizes, the improved level of breakdown voltage with the same MFP3 shrink is different. When MFP3 is reduced 3 μm, breakdown voltage is increased 70 V and 74 V, respectively, for PFP2 without change and with 2 μm reduction. The difference is 4 V and shorter PFP2 has higher breakdown voltage. When MFP3 continuously reduces by 5 μm, breakdown voltage increases by 92 V and 113 V. Their difference is enlarged to 21 V and the shorter PFP2 still has higher V_{BD}. The reason is that the highest electric field peak is changed from MFP3 left edge to PFP2 left edge as illustrated by Figure 7.

In further analysis of the NLDMOS breakdown voltage considering more MFP3 and PFP2 splits as shown in Figure 8, every PFP2 size has an optimized value of the MFP3 extending over PFP2 ($E1$). NLDMOS with this optimized $E1$ value has highest breakdown voltage. For different PFP2 size, the suitable $E1$ is between 2 μm and 5 μm. In the case of PFP2 original size, device with $E1 = 4$ μm shows highest breakdown

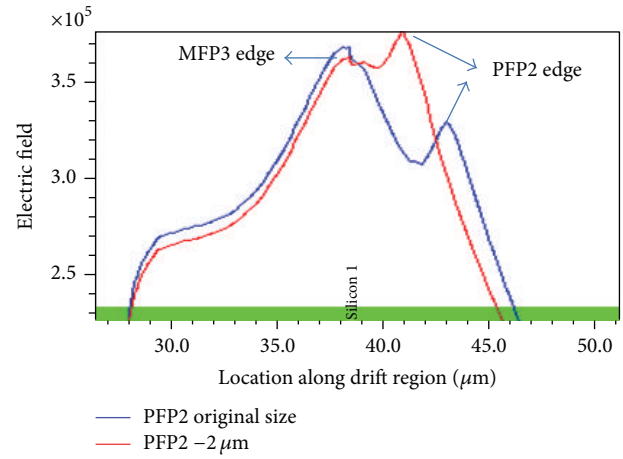

FIGURE 7: Lateral electric field distribution of MFP shrunk 5 μm for PFP2 no change and with 2 μm shrink.

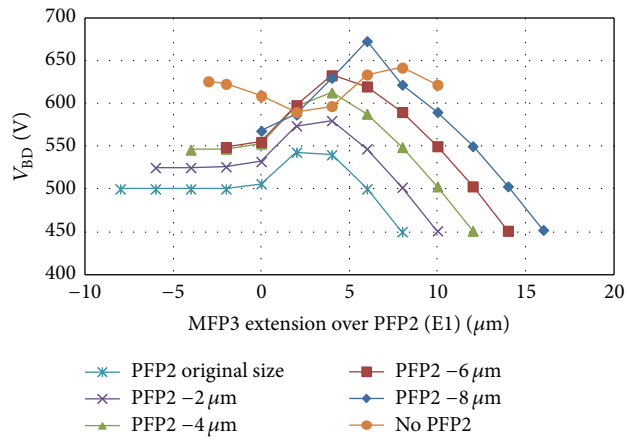

FIGURE 8: Breakdown voltage related to MFP3 extension over PFP2 ($E1$) for different PFP2 sizes.

voltage and V_{BD} starts to drop if $E1$ becomes smaller than this value. When MFP3 is shrunk 5 μm, the $E1$ is changed from 8 μm to 3 μm and the increase of breakdown voltage becomes less as Figure 6 shows.

7. Experiment Results

Based on the above study, a 500 V NLDMOS is designed with 30 μm drift length shrunk as well as metal and polysilicon field plate optimized. The breakdown voltage of simulated result and measurement data are 594 V and 590 V, respectively, as Figure 9 shows, and both results match well. The breakdown voltage meets the requirement of 500 V high voltage device.

Idvg characteristics curve of this device measured on silicon is in Figure 10. The R_{sp} calculated based on measured linear current of drain in Figure 10 is 7.88 ohm $*$ mm^2 and is about 25% less than the released data from another commercial company.

Table 3: Comparison of reference NLDMOS and this work.

Item	Reference	This work	Difference
Length of drift region (μm)	67	37	45%
V_{BD} (V)	772	590	24%

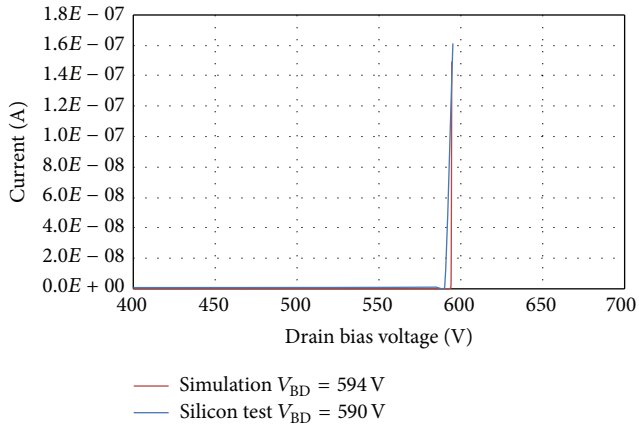

Figure 9: Breakdown voltage comparison of simulation and silicon data.

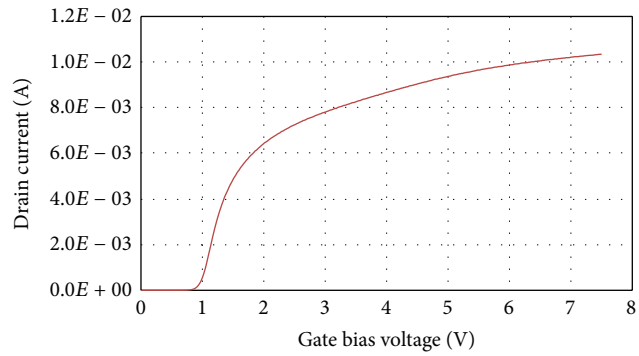

Figure 10: Idvg curve of this 500 V NLDMOS with area = 0.816 mm^2 at V_{dd} = 0.1 V. The R_{sp} is 7.88 ohm $*$ mm^2.

Compared with the referenced NLDMOS with 67 μm drift region length, the drift region of new device is shrunk by 47%. However, the V_{BD} of optimized 500 V NLDMOS is 590 V and only decreases by 24% compared to the V_{BD} of the reference one. It means that the breakdown voltage of the 500 V NLDMOS is improved a lot by this MFP and PFP design discussed in this paper. The result is summarized in Table 3.

8. Conclusion

Study of a 500 V high voltage NLDMOS and related field plate designs have been presented in this paper. The effect of metal and polysilicon field plate on the breakdown voltage has been investigated and the coeffect between MFP3 and PFP2 has also been studied. With the aid of research result, a demonstrated 500 V NLDMOS with 37 μm drift length and optimized field plate design achieves breakdown voltage of 590 V and R_{sp} of 7.88 ohm $*$ mm^2. This excellent on-resistance performance is about 25% less than the released data from another commercial company. The simulation and silicon data match well. The breakdown voltage has been greatly improved by proper field plate design. So the research result of MFP and PFP in this paper can be selected as a good reference for other high voltage designs. But the study on field plate presented in this paper does not consider the doping RESURF of drift region. It will be a direction in the further research of 500 V high voltage NLDMOS.

Conflict of Interests

The authors declare that there is no conflict of interests regarding the publication of this paper.

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