Current-Mode CMOS Implementation of a Fuzzy Min-Max Network

Yasuhiro Ota and Bogdan M. Wilamowski
Department of Electrical Engineering
University of Wyoming
Laramie, WY 82071, USA
ota@uwyo.edu, wilam@uwyo.edu

ABSTRACT
Current-mode CMOS implementations of a membership function circuit, min-max operators, and a defuzzifier circuit are proposed in this paper. The programmability of the proposed Gaussian-type function fuzzifier is achieved by varying the gate reference voltages and the sizes of transistors in the differential pairs. A closed-loop control scheme is employed between the fuzzifier and defuzzifier blocks to compensate the normalization of the denominator in the division of a centroid calculation in the defuzzifier block.

I. INTRODUCTION

In fuzzy systems there are three main steps: (1) fuzzification (membership function generation), (2) fuzzy inference or fuzzy rule evaluation, and (3) defuzzification. Excellent tutorial overviews on a utility of a fuzzy system and its application have been reported in many articles [1]-[4]. A Gaussian or triangular function is normally used in the fuzzification process. The second step, fuzzy rule evaluation or fuzzy inference, uses a technique called min-max inference to calculate numerical values representing the truth for certain consequent action based on a set of rules bearing the consequent. The defuzzification step is a process of combining all fuzzy outputs in a specific, crisp result that can be applied to each system output.

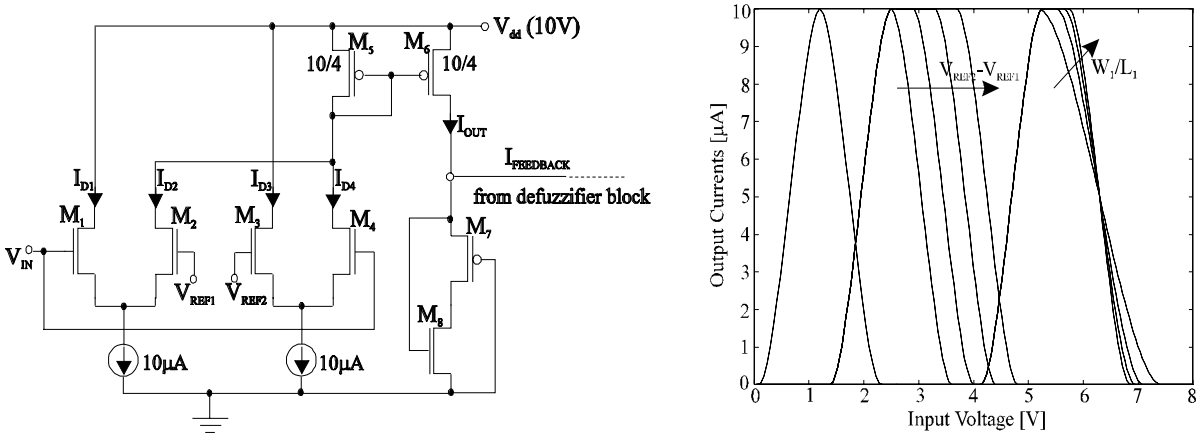
II. FUZZIFIER BLOCK

The first stage of a fuzzy system is the fuzzifier block. A membership function of an analog consequent is sampled to discrete grades. J. Choi *et al*. [5] introduced a voltage-input/current-output programmable Gaussian function network with capacitors for the programmability. Therefore, periodic refreshing is necessary to maintain an accurate programmed value on the capacitors. Also, the reference current needs to be adjusted to control the amplitudes of the output current in their design. A membership function circuit which can realize several types of membership functions using bipolar transistors was proposed in [4]. However, a disadvantage of this design is that it needs emitter-follower arrays for impedance transformation and level/temperature compensation.

The approach taken in this design is not biased in the subthreshold region so that a significant driving capability is achieved. In the strong-inversion region, the MOS transistors have a power-law dependence on the gate bias voltages. The strong-inversion operation of MOS circuits provides the features of high current driving, large dynamic range, and high noise immunity. It is also optimized for several design issues such as operation speed and precision to be suitable for scaleable fuzzy controller implementation. The transistors with large channel lengths are used to avoid the channel-length modulation effect and to lower the output conductance. The circuit schematic of the proposed Gaussian-type membership function is shown in Fig. 1(a). The average of the two reference voltages determines the mean of a Gaussian-type curve, and the input voltage is applied to the gates of M1 and M4. The transistors M7 and M8 are used as an active load [6]. For MOS transistors operating in the saturation region, the drain currents are approximated in a quadratic form and found in [7]. The output current I_{OUT} is then the sum of the two currents I_{D2} and $I_{D4,}$ and it is derived by [7] and given as

$$I_{OUT} = I + \frac{\alpha_1}{2}\sqrt{2\beta_1 - \alpha_1^{\,2}\beta_1^{\,2}} - \frac{\alpha_2}{2}\sqrt{2\beta_2 - \alpha_2^{\,2}\beta_2^{\,2}} \tag{1}$$

$$\text{where} \quad \alpha_i = \frac{V_{IN} - V_{REFi}}{V_{th}} \quad \text{and} \quad \beta_i = \frac{K' W_i V_{th}}{2 L_i I} \qquad (i = 1,2) \tag{2}$$



(a) (b)

Fig. 1. Gaussian-type membership function. (a) Circuit schematic of the membership function generator. M1 and M2 are sized as W_1/L_1, and M3 and M4 are sized as W_2/L_2. (b) Simulation result of the membership function circuit. It demonstrates the programmability of means, slopes (asymmetric curves), and trapezoidal shapes.

Fig. 1(b) illustrates the simulated characteristics of the output current I_{OUT} with various means by taking the average of the two reference voltages. It also depicts the programmability and availability of the membership functions with asymmetrical slopes and trapezoidal membership functions. The values of the control parameters α_i and β_i specified in expression (2) are chosen to obtain a desired shape of Gaussian-type curves. If symmetrical curves are desired, the transistor sizes of the two differential pairs must be the same. The controllability of the shape of the output current can be achieved by varying the difference of the two reference voltages. As can be seen, the output current curve approaches to a trapezoidal shape as the difference of the two reference voltages becomes larger. The fuzzifier circuit is also controlled by the output current of the defuzzifier block, which functions as a feedback signal to the fuzzifier [7].

III. FUZZY INFERENCE BLOCK

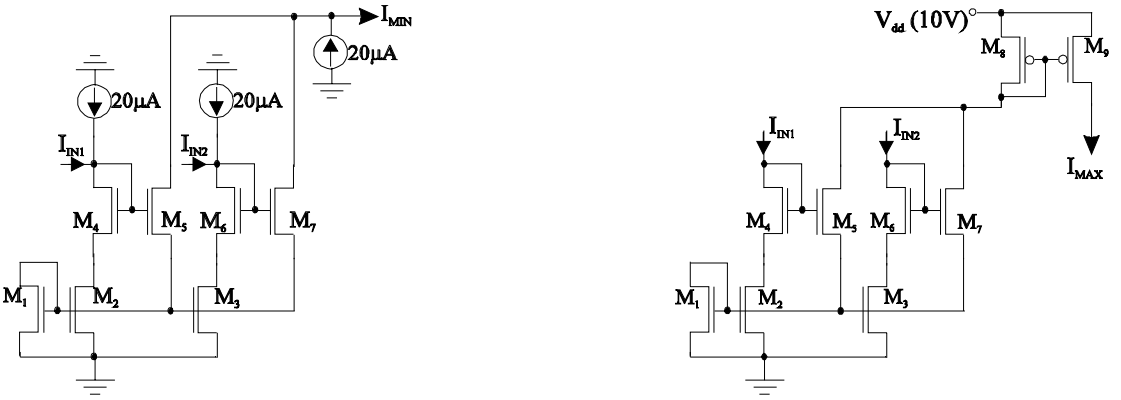
The most popular fuzzy logic functions which implement logical "AND" and logical "OR" are MIN and MAX, respectively. A design of min-max circuits using bipolar transistors in the emitter-coupled form was introduced by Yamakawa [4]. Because of the thermal drift and the 0.7-volt shift of emitter junction produced at the output of the comparator, it is necessary to add an extra compensator to adjust the offset in his design. The proposed design basically has a similar structure reported in [8]. However, the proposed design uses only *n*-channel CMOS for both the min and max circuits. The circuit schematics of the min-max operators are shown in Fig. 2. The min circuit consists of the max circuit block with extra current sources to complement the direction of currents and to apply the DeMorgan's rule. The min operator finds the *intersection* of fuzzy sets I_{IN1}, I_{IN2}, Λ, I_{INn}. Therefore, the min circuit functions to detect the smallest current of a set of *n* given input currents as

$$I_{MIN} = \min\left[I_{IN1}, I_{IN2}, \otimes, I_{INn}\right] \tag{3}$$

While the max operator finds the *union* of two fuzzy sets I_{IN1}, I_{IN2}, Λ, I_{INn}, and the max circuit functions such that

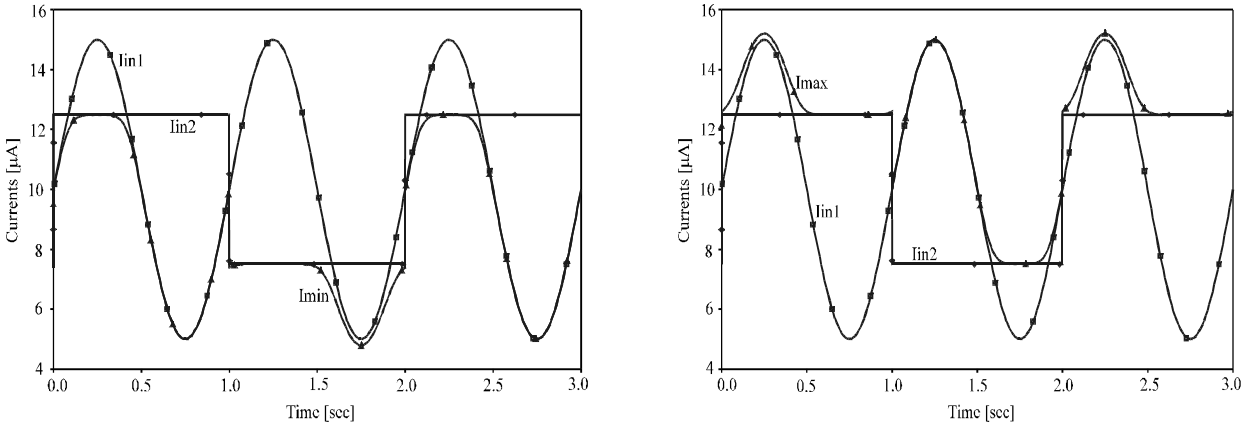
$$I_{MAX} = \max\left[I_{IN1}, I_{IN2}, \otimes, I_{INn}\right] \tag{4}$$

The SPICE simulation of the min-max operators with two input currents is shown in Fig. 3.



(a) (b)

Fig. 2. Circuit schematics of the min-max operators. All the transistors are of the same size. (a) Min circuit. (b) Max circuit.



(a) (b)

Fig. 3. SPICE simulation results of the min-max operators. (a) Min circuit characteristics. (b) Max circuit characteristics.

IV. DEFUZZIFIER BLOCK

The centroid, or the center of gravity (C.G.), method is simple and the most popular defuzzification method. Its algorithm is given as

$$C.G.=\frac{\sum_{i=1}^{n}\mu(z)_i \cdot z_i}{\sum_{i=1}^{n}\mu(z)_i} \tag{5}$$

where n represents the number of fuzzy sets on the universe of discourse, and $\mu(z)_i$ and z_i represent the membership function and the weighting value of the *i-th* fuzzy set, respectively. From a MOS analog circuit point of view, division has always been a troublesome operation in terms of time and area.. Many of the reported fuzzy controllers impose the condition that the denominator in expression (5) assumes the value 1 to avoid the division, or recur to the use of global normalization loops [4] [9].

The proposed design makes a use of a closed-loop feedback loop between the defuzzifier and fuzzifier blocks as shown in Fig. 4. The output current from the output of the transconductance amplifier is copied through

current mirrors and fed into the membership function circuits. Then the mirrored feedback currents shift output currents of the Gaussian-type curves up or down depending on the amount of the output feedback current. The purpose of the feedback is based on the principle of the normalization to make the denominator in expression (5) be constant. The detail description of the defuzzifier block along with its circuit schematic and the concept of the feedback current is given in [7].

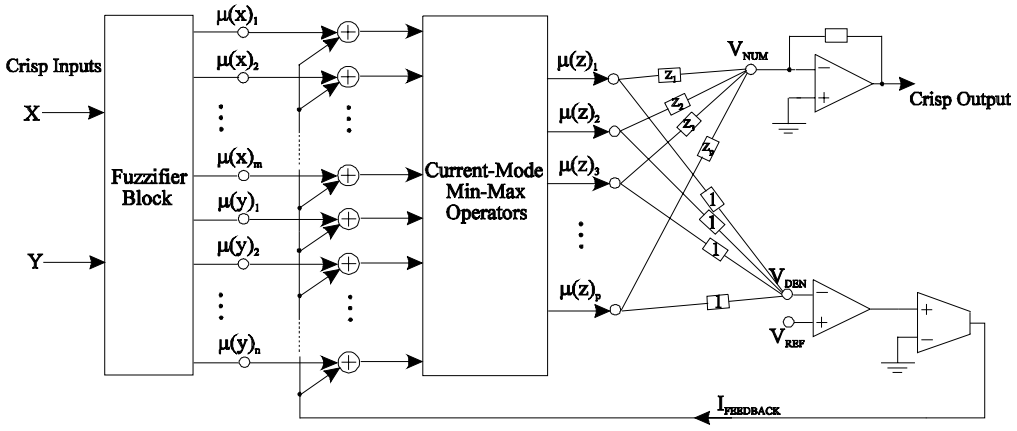


Fig. 4. Fuzzy min-max network with a feedback loop and a defuzzifier which avoids a division in the centroid calculation.

V. CONCLUSIONS

A programmable, current-mode CMOS implementation of a min-max fuzzy network using a feedback loop has been proposed in this paper. The output current of the defuzzifier block is used as a feedback signal which is fed to the input current of the membership function circuit. By using this scheme, the output voltage of the fuzzifier circuit is shifted up or down depending upon the magnitude of the output current of the defuzzifier block, achieving the quasi-normalization of the denominator in the centroid calculation. The main characteristics of the proposed architecture are high operation capacity, simple inference, and high precision.

REFERENCES

[1] L. A. Zadeh, "Fuzzy Logic," *IEEE Computer Magazine*, pp. 88-93, April 1988.

[2] P. K. Simpson, "Fuzzy Min-Max Neural Networks - Part 2: Clustering," *IEEE Trans. on Fuzzy Systems*, vol. 1, no. 1, pp. 32-45, Feb. 1993.

[3] J. R. Angulo and R. P. Loera, "Low Voltage Current-Mode and Voltage-Mode Min and Max Circuit Building Blocks for Analog CMOS Fuzzy Processors," *Proceedings: 3rd Int. Conf. on Fuzzy Logic, Neural Networks and Soft Computing*, Iizuka, Japan, 1994.

[4] T. Yamakawa, "A Fuzzy Inference Engine in Nonlinear Analog Mode and its Application to a Fuzzy Logic Control," *IEEE Trans. on Neural Networks*, vol. 4, no. 3, pp. 496-522, May 1993.

[5] J. Choi, B. J. Sheu, and J. C.-F. Chang, "A Gaussian Synapse Circuit for Analog VLSI Neural Networks," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, vol. 2, no. 1, pp. 129-133, March 1994.

[6] Y. Ota and B. M. Wilamowski, "VLSI Implementation of a Programmable Current-Mode Neural Network," *Proceedings: Intelligent Engineering Systems Through Artificial Neural Networks, ANNIE'94 Conf.*, St. Louis, USA, Nov. 1994, vol. 4, pp. 71-76.

[7] Y. Ota and B. M. Wilamowski, "CMOS Implementation of a Voltage-Mode Fuzzy Min-Max Controller," submitted to *Journal of Circuits, Systems, and Computers*, January 1995.

[8] I. Baturone, A. Barriga, and J. L. Huertas, "Multi-input Voltage and Current-Mode Min/Max Circuits," *Proceedings: 3rd Int. Conf. on Fuzzy Logic, Neural Networks and Soft Computing*, Iizuka, Japan, 1994.

[9] M. Sasaki, N. Ishikawa, F. Ueno, and T. Inoue, "Current Mode Analog Fuzzy Hardware with Voltage Input Interface and Normalization Locked Loop," *IEICE Trans. Fundamentals*, vol. E57-A (6), pp. 650-654, June 1992.

[10] I. Baturone, S. S. Solano, and J. L. Huertas, "Current-Mode Singleton Fuzzy Controller," *Proceedings: 3rd Int. Conf. on Fuzzy Logic, Neural Networks and Soft Computing*, Iizuka, Japan, 1994.