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Performance Evaluation of Complex Multiplier Using Advance Algorithm

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Abstract- In this paper VHDL implementation of complex number multiplier using ancient Vedic mathematics and conventional modified Booth algorithm is presented and compared. The idea for designing the multiplier unit is adopted from ancient Indian mathematics "Vedas". The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. Multiplication using Urdhva Tiryakbhyam sutra is performed by vertically and crosswise. The feature of this method is any multi-bit multiplication can be reduced down to single bit multiplication and addition. On account of these formulas, the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB. The implementation of the Vedic mathematics and their application to the complex multiplier ensure substantial reduction of propagation delay. The simulation results for 4 bit multiplication using Booth's algorithm and using Vedic sutra are illustrated.

Keywords –Signal Processing Algorithms; Vedic Multiplier; VHDL Implementation; Vedas; Complex number multiplier.

I. INTRODUCTION

Multipliers are key components of many high performance systems such as FIR filters, microprocessor, digital signal processor, etc. A systems performance is generally determined by the performance of the multiplier, since the multiplier is generally the slowest element in the system [2]. Complex number operations are the backbone of many digital signal processing algorithms which mostly depend on extensive number of multiplication. Complex number multiplication involves four real number multiplication and two additions/ subtractions [3]. While doing real number multiplication, carry needs to be propagated from the least significant bit (LSB) to most significant bit (MSB) when binary partial products are added. The overall speed is drop down by the addition and subtraction after binary multiplication [4] [5].

Vedic Mathematics is an ancient mathematics which is based on 16-sutras and 16-sub sutras invented by Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960). Mainly multiplication in Vedic mathematics in carried out using three sutras Nikhilam Navatascaraman Dasatah, Ekadhikena Purvena and Urdhva Tiryakbhyam [1]. Urdhva Tiryakbhyam sutra is the targeted Vedic sutra (algorithm) as it is suitable for all cases of multiplication. The most common multiplication algorithms used are Array multiplication and Booths algorithm. The computational time in case of Array multipliers are comparatively less since the partial results are calculated in parallel. Multiplication using Booths algorithms takes comparable computational time [11]. These algorithms are used for multi-bit and exponential operations that require large partial results and carry registers [3]. This paper presents multiplication algorithm that may be useful in the efficient implementation of signal processing algorithms. The framework of this multiplication algorithm is based on Urdhva Tiryakbhyam sutra of Vedic mathematics.

This paper is organized as follows. In section II the implementation methodology of complex number multiplication using Booth-Wallace algorithm, Urdhva Tiryakbhyam sutra of Vedic mathematics is explained with examples. Device utilization in both is compared and discussed in Section III. Results obtained for 4-bit complex multiplication are presented in section IV. Concluding remarks are presented in section V.

II. IMPLEMENTATION

While implementing complex number multiplication, the multiplication system can be divided into two main components giving the two separate results known as real part (R) and imaginary part (I).

$$R + j\,I = (A + j\,B)\,(C + j\,D) \qquad (1)$$

Gauss's algorithm for complex number multiplication gives two separate equations to calculate real and imaginary part of the final result. From equation (1) the real part of the output can be given by (AC - BD), and the imaginary part of the result can be computed using (BC + AD). Thus four separate multiplications and are required to produce the real as well as imaginary part numbers [10] [11] [12].

A. Complex number multiplication using conventional modified Booth Wallace multiplier –

Multiplication process is the critical part for any complex number multiplier design. There are three major steps involved for multiplication. Partial products are generated in first step. In second step partial product reduction to one row of final sums and carries is done. Third and final stage adds the final sums and carries to give the result. Since the Radix-4 modified Booth algorithm is capable to reduced the number of partial products by nearly equal to half, this algorithm is used in the first step of implementation of complex number multiplication using Booth's method. In the second step Wallace tree structure is used to rapidly reduce the partial product rows to the final two rows giving sums and carries. The multiplication design based on Radix-4 modified Booth algorithm consists of two main blocks known as MBE (Modified Booth Encoding) and partial product generator as shown in Fig. 2. Wallace Tree CSA structures have been used to sum the partial products in reduced time. In this regard, combining both algorithms in one multiplier, we can expect a significant reduction in computing multiplications [12].

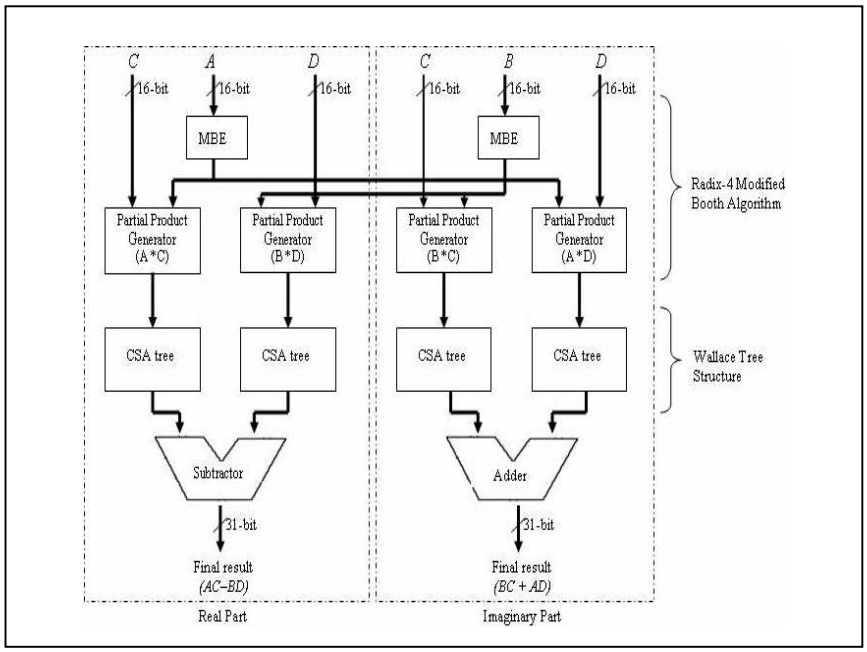

Figure 1. Block diagram of complex number multiplier

B. Vedic multiplication method

The proposed complex number multiplier is based on the Vedic multiplication formulae (Sutras). These sutras have been traditionally used for the multiplication of two numbers in decimal number system. In this work the same

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ideas are applied to binary number system, to make the proposed algorithm compatible with the digital hardware. The multiplication based on Urdhva Tiryakbhyam sutra is discussed below.

C. Urdhva Tiryakbhyam sutra

Urdhva Tiryakbhyam sutra is suitable for all cases of multiplication. It literally means "Vertically and crosswise" [8]. Multiplication using this sutra is performed by vertically and crosswise, vertically means straight above multiplication and crosswise means diagonal multiplication and taking their sum. The feature of this method is any multi-bit multiplication can be reduced down to single bit multiplication and addition [1]. The multiplication is illustrated below using an example. The crosswise and vertical multiplication be implemented starting either from right hand side or left hand side [7] [8].

Example 1: Multiplication of 42 and 13

Step 1: Starting at the left multiply two left hands most significant digits vertically and set down results underneath as the left hand most significant part of the answer.

```
4       2
1       3
4 ((4 * 1) = 4)
```

Step 2: Next multiple crosswise and add these partial results. Set down the result of addition as illustrate below.

```
4       2

1       3
4       4 (((4 * 3) + (1* 2)) = 14)
1
```

Step 3: multiply two rights hand least significant digits vertically and set down results underneath as the right hand least significant part of the answer.

```
4       2
1       3
4       4       6 ((2 * 3) = 6)
1
```

Step 4: Finally add the digits vertically as illustrated

```
4       2
1       3
4       4       6
1
5       4       6
```

Result of multiplication 42 * 13 = 546.

Thus the above method is equally applicable for binary multiplication. Fig. 3 shows the general multiplication procedure of the 4x4 multiplication. The multiplication of two 4-bit binary numbers a3a2a1a0 and b3b2b1b0 is performed starting from left hand side. Every step in fig. 3 has a corresponding expression as follows:

$$r0=a0b0 \quad (1)$$

$$c1r1=a1b0+a0b1 \quad (2)$$

$$c2r2=c1+a2b0+a1b1+a0b2 \quad (3)$$

$$c3r3=c2+a3b0+a2b1 + a1b2 + a0b3 \quad (4)$$

$$c4r4=c3+a3b1+a2b2 + a1b3 \quad (5)$$

$$c5r5=c4+a3b2+a2b3 \quad (6)$$

$$c6r6=c5+a3b3 \quad (7)$$

With c6r6r5r4r3r2r1r0 being the final product [3] [4] [8].

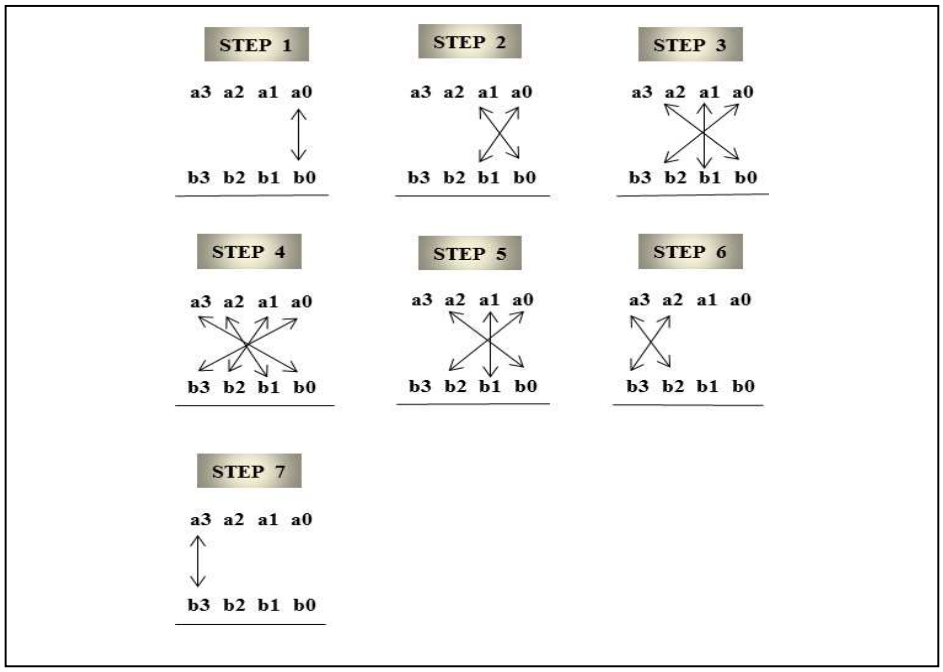

Figure2. Vertically crosswise multiplication of four bit binary number [3]

III. DISCUSSION

The four bit complex number multiplier using Urdhva Tiryakbhyam and Booth's algorithm is implemented using VHDL. The methodology used to implement the complex multiplier using Gauss's multiplication equations are described with the help of block diagram is shown in fig. 3. As discussed earlier complex multiplication requires four multiplications and an addition and subtraction.

The functional verification of the code through simulation is carried out using Xilinx ISE simulator. The complete code is synthesized using Xilinx synthesis tool (XST). Table 1 indicates the device utilization summary of the Vedic complex and Booth's complex multiplier. Figure 4 shows the device utilization and figure 5 & 6 shows the RTL schematic of 4-bit complex multiplier using Vedic and Booth's algorithm respectively. Since the methodology used for the implementation of complex multiplier in both case is quite same, still the device utilization and the combinational delay, in case of Vedic algorithm is less compared to Booth's algorithm.

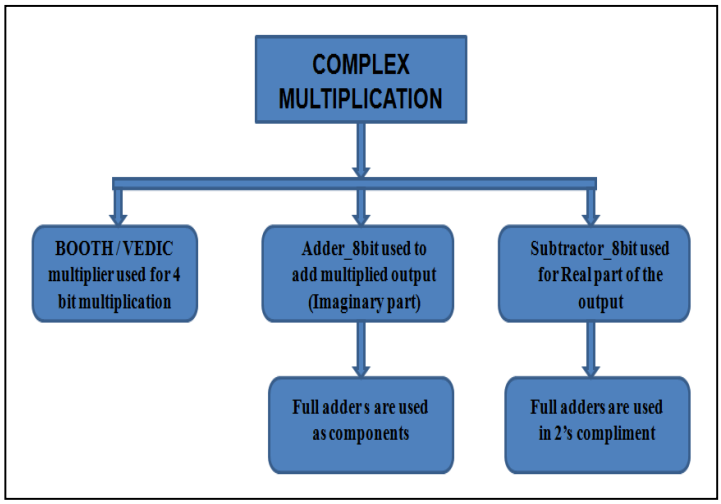

Figure 3. .Proposed methodology for complex number multiplication

TABLE I. DEVICE UTILIZATION SUMMARY

Algorithm	NO. of Slices	NO. of 4 input Slices	NO. Of IO's	No. of bonded IOB's	Delay in nS.
Vedic complex	**84**	**147**	**33**	**33**	**18.419**
Booth's complex	**100**	**174**	**33**	**33**	**19.997**

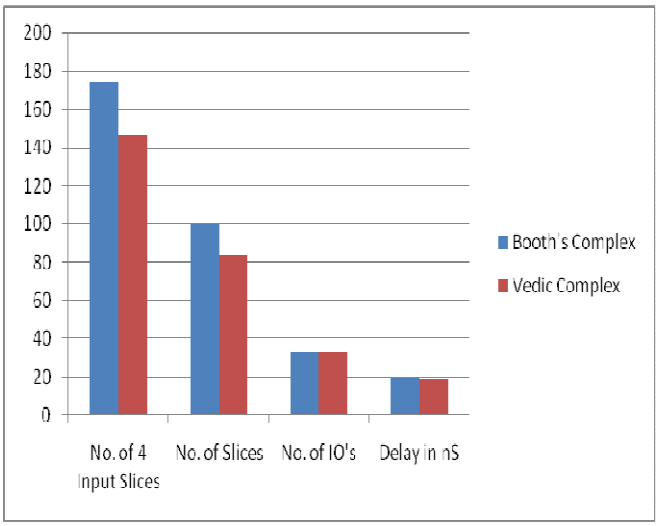

Figure 4. Comparative chart of device utilization

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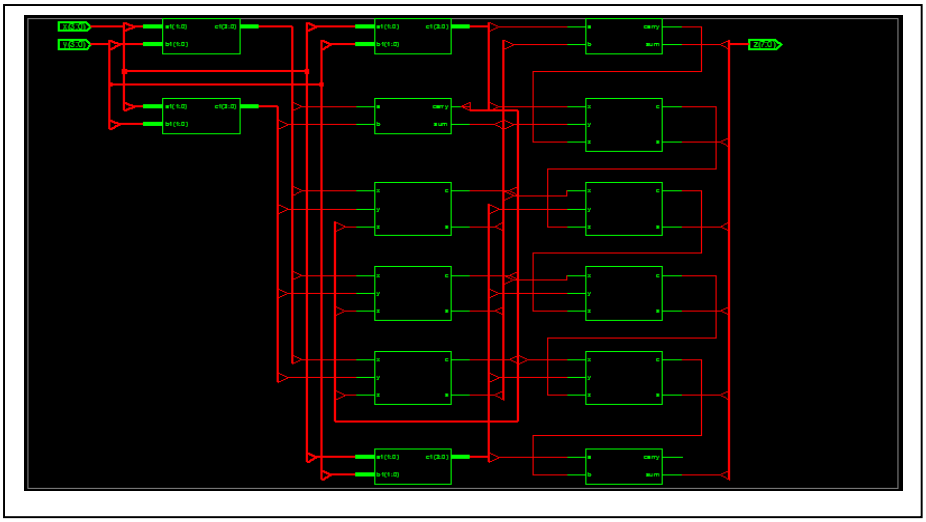

Figure 5. RTL schematic [partial] of 4-bit complex multiplier (Vedic multiplier)

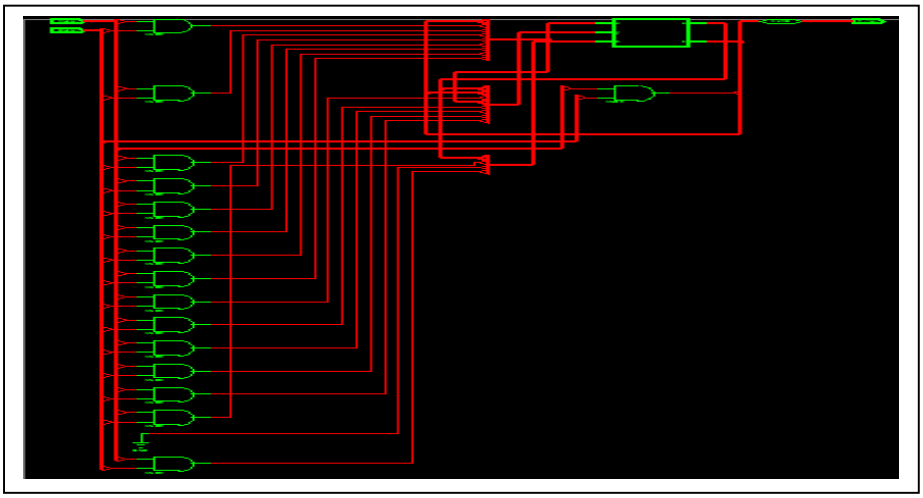

Figure 6. RTL schematic [partial] of 4-bit complex multiplier (Booth's)

IV. RESULTS

The work presented in this paper was implemented using VHDL and logic simulation was done using Xilinx ISE simulator and synthesis was done using Xilinx project navigator. The design was synthesized for Spartan3 (xc3s200-5-ft256) device. The obtained results are presented in table 1, and waveforms for 4-bit complex multiplication using Urdhva Tiryakbhyam and Booth's algorithm is shown in figure 7 & 8 respectively. The device utilization in case of Vedic complex is less (No. of Slices: 84 out of 1920 - 4%, Number of 4 input LUTs: 147 out of 3840 - 3%, Number of bonded IOBs: 33 out of 173 - 19%) compared to Booth's complex (No. of Slices: 100 out of 1920 - 5%, Number of 4 input LUTs: 174 out of 3840 - 4%, Number of bonded IOBs: 33 out of 173 - 19%). The delay required by Vedic complex multiplier is 18.419 ns, while it is 19.997 ns for Booth's complex.

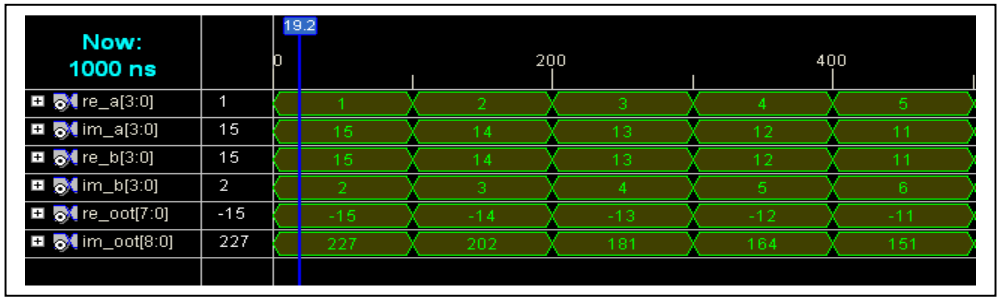

Figure 7. Simulation waveforms for 4-bit complex multiplication (Vedic)

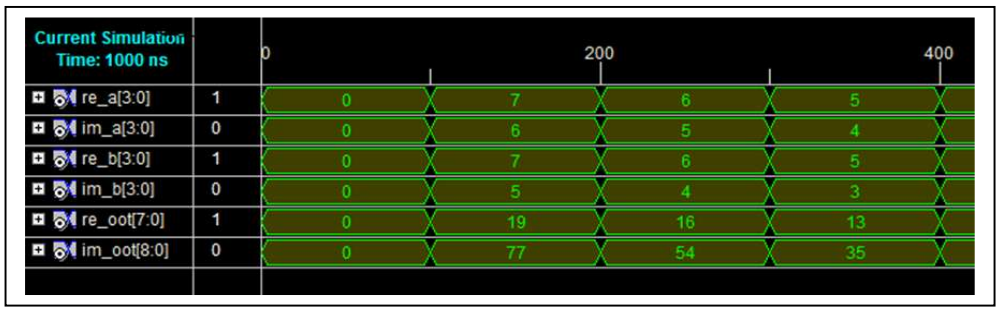

Figure 8. Simulation waveforms for 4-bit complex multiplication (Booth's)

V. CONCLUSION

In many real-time DSP applications number of complex multiplications are involved, in which high performance is a prime target. However, achieving this may be done at the expense of area, power dissipation and accuracy. The performance in terms of throughput of the processor is limited by the multiplication. So efforts have to be made to decrease the number of multipliers and to increase their speed. A high speed complex number multiplier design using Vedic Mathematics (Urdhva Tiryakbhyam sutra)is implemented using VHDL. This sutra is applicable to all cases of multiplication. The results show that Urdhva Tiryakbhyam sutra with less number of bits may be used to implement high speed complex multiplier efficiently in digital signal processing algorithms.

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