Silicon Etch with Integrated Metrology for Through Silicon Via (TSV) Reveal

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Abstract—Wet etch is a cost-effective process option to reveal through-silicon vias (TSVs). This paper addresses the methodology for using integrated wafer thickness measurements to provide complete process control.

Keywords—TSV; endpoint detection; TTV; reveal height; wet etch

I. INTRODUCTION

Cost and manufacturability are critical to the adoption of 3D packaging. Using a wet etch is a cost-effective method to reveal the through-silicon vias (TSVs). This method is complemented by integrating thickness measurements and endpoint detection to provide complete process control.

The TSV middle process appears to be the preferred integration scenario. For this process flow, the silicon wafer needs to be thinned to reveal the Cu TSV. The bulk of the silicon is removed by grinding. The removal of the remaining silicon needs to uniformly expose the TSVs while relieving the stress from the grinding operation. A single wafer wet etch with an integrated thickness measurement system accomplishes both tasks.

II. BACKGROUND

The process flows for the TSV middle integration scenario have been discussed previously. The TSVs have been etched into the silicon and may vary in depth across the wafer. The device wafer is mounted on a carrier using an adhesive layer. The adhesive layer can vary in uniformity, which will add to the total thickness variation (TTV) of the wafer during the grinding process. These non-uniformities can be radial in nature due to the process that caused them. Center-to-edge etch rate variations have been documented for the deep reactive-ion etching (DRIE) process. For adhesives applied by spin coating, a thicker film can result at the edge of the wafer. When the adhesive is thicker at the edge, the grinding process will make the silicon thinner at the edge.

As shown in Fig. 1, there are two values required to determine the amount of silicon to be etched. These are the nominal thickness of the silicon and the depth of the via. In addition to these nominal values is the radial variation that is observed across the wafer diameter.

There can be a big difference in the amount of silicon to be etched, depending on the uniformities of the post-grind silicon thickness and the via depth. These variations are illustrated in Table 1 in order to achieve a 2-µm reveal height.

<table>
<thead>
<tr>
<th>Example</th>
<th>Thickness Post Grind</th>
<th>Via depth</th>
<th>Etch depth to reveal</th>
</tr>
</thead>
<tbody>
<tr>
<td>nominal case</td>
<td>65</td>
<td>55</td>
<td>12</td>
</tr>
<tr>
<td>thicker silicon</td>
<td>70</td>
<td>55</td>
<td>17</td>
</tr>
<tr>
<td>thinner silicon</td>
<td>60</td>
<td>55</td>
<td>7</td>
</tr>
<tr>
<td>shorter via</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nominal case</td>
<td>65</td>
<td>50</td>
<td>17</td>
</tr>
<tr>
<td>thicker silicon</td>
<td>70</td>
<td>50</td>
<td>22</td>
</tr>
<tr>
<td>thinner silicon</td>
<td>60</td>
<td>50</td>
<td>12</td>
</tr>
<tr>
<td>longer via</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>nominal case</td>
<td>65</td>
<td>60</td>
<td>7</td>
</tr>
<tr>
<td>thicker silicon</td>
<td>70</td>
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<td>12</td>
</tr>
<tr>
<td>thinner silicon</td>
<td>60</td>
<td>60</td>
<td>2</td>
</tr>
</tbody>
</table>

The KOH wet etch process has been discussed previously. A two-step etch process can be used to improve etch rates, profile control, and surface smoothing. This higher etch rate portion of the process uses a non-selective, isotropic etchant, that provides improved surface characteristics compared with the anisotropic etchants. The second step of KOH or TMAH, which are anisotropic etchants, is selective to silicon and does not etch oxide or copper. A new anisotropic chemistry, Sachem Developmental Si Etchant SMC 42-1, has also been used for this process with excellent results.
III. INTEGRATED WAFER THICKNESS MEASUREMENT

Integration of a wafer thickness measurement sensor in the etch system provides closed-loop control of the etching process. The sensor is incorporated as a separate chamber in the system design, thereby eliminating the need for off-line thickness metrology. The ISIS StraDex f2-300 sensor uses spectral coherence interferometry at 1300-nm wavelength to obtain thickness measurements.

The sensor measures the actual thickness of only the device wafer and not the entire stack, which includes the carrier and adhesive. Measurements are taken across the diameter of the wafer. The measurement of the via depth is done previously in the front end-of-line (FEOL) process when the vias are etched. The data are provided for incorporation in the calculation of silicon etch depth and radial profile. Using the amount of silicon that was etched on the previous wafer, the etch rate can be computed and used for the next wafer to provide closed-loop process control. The projected etch time is calculated using this etch rate. The radial etch profile is selected based on the thickness of the silicon minus the depth of the TSV. A flow chart for this process sequence is shown in Fig. 2.

![Fig. 2 Process flow for measurement and etch](image)

Continual thickness measurement allows the etch rate to be determined and fed forward for the next wafer to be processed. Endpoint detection determines when the vias are observed, however an over-etch is required past that point for the reveal to achieve the desired height. Target reveal heights are generally 2-5 µm. If the final Si thickness measured is not within spec, the wafer can return to the etch chamber for further processing.

IV. ENDPOINT DETECTION

The use of endpoint detection (EPD) allows the system to determine when the vias are initially revealed. As discussed above, the radial via depth data is needed for the calculation of the etch profile. The use of EPD provides a check and balance for ensuring that the data provided for via depths is accurate. The etch process needs to continue beyond this endpoint in order to reveal the vias to the desired height. The overall etch time and process conditions are based on the thickness calculations and etch rate data acquired by the system software. Fig. 3 shows an example of the endpoint signal acquired as the vias are revealed.

![Fig. 3 Example of EPD](image)

During development of the TSV process, there have been changes in pattern density, via diameters, oxide liner thicknesses, and barrier materials. All of these parameters have some effect on the EPD signal. Enhancements to the optics and software algorithms will continue to develop along with the changes in the TSV process.

V. RESULTS

Some examples of wafer thickness measurements are shown in Fig. 4 and Fig. 5. The wet etch can compensate for radial non-uniformities by using an etch profile that etches faster or slower in the center of the wafer. Some examples of radial thickness variations are shown in Fig. 4.

![Fig. 4 Examples of thickness measurements post grind–radial symmetry](image)

Thickness variations can also be asymmetric and not perfectly radial, as illustrated in Fig. 5. A compromise is required in the etch profile. The thickness differences are averaged for the two sides of the wafer.
For the etch rate calculation, the silicon thickness and via depth data are required. Fig. 6 provides an example of the initial silicon thickness measurement, the via depths, and amount to be etched. In Fig. 7, the desired etch profile that is calculated is compared with the actual results after the etch process.

The thickness measurement after the silicon etch is shown in Fig. 8, along with a comparison to where the via depths are located for a 5-µm reveal height.

The etch profile calculation is based on the assumption that the via depths provided are accurate. Fig. 9 shows a comparison of the calculated and measured reveal heights after the etching process. The reveal heights were measured by two techniques: 1) KLA Profilometer and 2) ISIS topography sensor. Good agreement is observed for these measurements. Profilometer verification was done on one to five vias at a particular location. The ISIS topography sensor measured the selected array of ~20 vias at each location.

For this example, the initial thickness variation of the silicon was 4.4 µm. The TSV depth variation was 1.5 µm. If a uniform etch of the silicon had been done, without compensation, the reveal heights would have varied by the same 4.4 µm with some of the vias being exposed up to 10 µm. Using an etch profile to compensate for the incoming silicon thickness variation, the resulting reveal heights were within a ±1-µm window around the desired 5-µm reveal height. Fig. 10 and Fig. 11 provide SEM examination of the wafer and show a smooth silicon surface with the vias revealed by 5 µm.
VI. DISCUSSION

While a significant amount of work has been done to develop TSV processes, critical manufacturing challenges still remain. Variations are seen in TSV etch depth and silicon thickness post grind. Differences are observed from wafer-to-wafer and radially within a wafer. In order to provide more uniformly revealed vias after the etch, the process needs to compensate for these variations. The integrated thickness measurement allows a tailored etch recipe to be calculated for each wafer immediately prior to the etch. The post-etch measurement confirms the proper amount of silicon was etched.

The integrated thickness measurement eliminates the need for a separate metrology tool. This capability also shortens the rework cycle, if required.

VII. CONCLUSIONS

Integrated wafer thickness measurement provides closed-loop control of the etching process. Endpoint detection identifies the actual via reveal to ensure the correct amount of silicon is etched. Radial non-uniformities in the silicon thickness and via depths can be compensated for using the wet etch process.

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