An $I_{DDQ}$ Fault Model to Facilitate the Design of Built-In Current Sensor (BICSs)*

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Abstract

In this paper, we present an efficient and accurate $I_{DDQ}$ fault modeling technique for digital CMOS circuit. Both the normal and faulty "current" behaviors of a CMOS digital circuit can be described by this model. Also the parasitic capacitive and inductive parameters can be emulated. A formal method for creating this model from any given CMOS circuit is outlined. Using this model, circuit design of built-in current sensors (BICSs) can be designed and validated without introducing the actual circuit under test (CUT) which implanted a fault. Experimental data for the application to the design of BICSs is also given.

1 Introduction

In order to design and implement built-in self-testing (BIST) circuit, it is necessary to consider the physical defect that are likely to occur with the specific technology being used. However, digital circuit design is always done at the level of boolean logic other than the level of voltages, currents, and charges. Hence once the likely physical defects are known it is desirable to determine the effects that these defects have on the operation of the circuit and the fault coverage that the BIST circuit can achieve.

The built-in current sensor (BICS) [1, 2, 3] technique is one of the BIST circuits for CMOS technology. This approach comes from the basic property of a static CMOS circuit that the current consumption is very low during the steady state. By contrast, if the circuit under test (CUT) consumes an abnormal $I_{DDQ}$ it means that there may exist a defect inside the circuit. Thus one can determine whether the CUT is fault free or not by measuring the current consumption on the power bus during the steady state.

Unfortunately there are some problems in designing or using these BICSs. (1) Most of these designs are not designed in a parameterised way, namely, these BICSs are designed with respect to a special CUT, e.g., full adder in [1, 4]. (2) The CUT is a digital part while the BICS is analog. A mix-mode simulator is needed to simulate the whole CUT with BICS, otherwise, extra efforts should be made to translate the CUT's netlist which is gate level to the format of a device level simulator (e.g. SPICE). (3) Many reports suggest that the CUT should be partitioned before proper use of BICSs. Due to the lack of proper partition methodology, these BICSs are not well accepted to be incorporated into a given CUT. (4) Since the BICS is an analog part while the CUT is digital, it may be designed in separate departments or different engineers. The completeness of the CUT may be a critical part before the design of BICS. (5) BICS is used to detect the abnormal current usage of the CUT. Therefore a "defect" must be injected into the CUT to evaluate the performance of the BICS. It is always a time-consuming process to simulate different faults which have different fault conditions.

From the above discussion, an efficient fault model for digital circuit is then needed to facilitate the design of BICSs. Recently, several analog fault modeling techniques have been proposed in [5, 6]. However these techniques focus on the modeling "methodology", thus there still needs a lot of efforts in developing a practical fault model from any given circuit. Also these techniques are to model the "voltage" malfunction on the primary outputs for observation. Thus a further modification should be made in order to have a "current" function of a CUT.

The rest of this paper is organized as follows. In Section 2, the model is presented. Experimental data of this model on the design of Chang's BICS scheme is given in Section 3. Finally Section 4 concludes this paper.

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2 The $I_{DDQ}$ fault model

Most previous BICS designs were evaluated via a special digital CUT (e.g., a full adder in [4]) with some implanted specific faults. However, from the perspective of simulation process, it is a time-consuming process to evaluate the performance of the BICS on various faults of a complex CUT. Therefore an efficient CUT model is needed to increase the simulation throughput.

In this section, a formulized modeling technique for digital CUT is developed based on the methodology in [6]. Our object is to develop a fault model so that its characteristics is simple to minimize the simulation cost and accurate enough to represent the "current" behavior on the normal or faulty states. The level of abstraction is device level. This model is shown in Figure 1. We will describe the primitives used in this model as follows.

\[ \begin{align*}
\text{LVdd} & \rightarrow \text{BICS} & C_{exi} \\
\text{VIH} & \rightarrow \text{BICS} & \text{VOH} \\
\text{VIL} & \rightarrow \text{BICS} & \text{VOL} \\
\text{GND} & \rightarrow \text{BICS}
\end{align*} \]

Figure 1: The $I_{DDQ}$ fault model.

2.1 DC characteristics of a CMOS CUT

Different from the functional behavior that determines the relationship between inputs and outputs, the DC characteristics of a CUT is to confine the normal operation environment of a circuit. These specifications affect the analysis of power supply, package, thermal radiation, placement and routing, etc. In general, the following parameters should be considered: (1) the input high (low) voltage $V_{IH}$ ($V_{IL}$), (2) the output high (low) voltage $V_{OH}$ ($V_{OL}$), (3) the quiescent (transient) power supply current $I_{DDQ}$ ($I_{DDT}$), and (4) the high (low) noise margin $NM_H$ ($NM_L$). These parameters are shown in Figure 2.

\[ \begin{align*}
\text{IDD} & \rightarrow \text{logic 1} \\
\text{IDD} & \rightarrow \text{logic 0} \\
\text{IDD} & \rightarrow \text{IDDQ}
\end{align*} \]

Figure 2: (a) The specification range of $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $NM_H$ and $NM_L$. (b) The specification of $I_{DDQ}$ and $I_{DDT}$.

The $V_{IH}$, $V_{IL}$, $V_{OH}$, and $V_{OL}$ specify the logic level of a digital circuit. If the voltage level at a node is in the intermediate region, then its logic level will be indeterministic. Therefore it may result in an error function. A basic rule for the hardware design is that the voltage drop at node GND should be stably kept at the logic level "0", i.e., $V_{GND} < V_{IL} + N_L$ or $V_{GND} < V_{OL} + N_L$. Thus if a BICS is designed at the GND node, e.g., like the Chang's [4] and the Miura's designs [7], the voltage shift should be kept below $V_{IL} + N_L$ and $V_{OL} + N_L$.

Though BICSs are designed to monitor the quiescent current $I_{DDQ}$, however they should also support the maximum transient current $I_{DDT}$ in order to guarantee the reliability of the CUT. The value of $I_{DDT}$ affects not only the power bus width but also the dimensions of the devices in the BICSs.

$I_{DDQ}$ and $I_{DDT}$ can be generated by a series inverters [3]. The $W/L$ dimensions of the devices in each inverter can be specified to emulate the magnitudes of the transient and the static current. The stage number $n$ can be controlled to approximate the durations of the transient and steady states. The primary input of this circuit can be applied with a test pattern at a speed that the actual CUT operates at.

2.2 Bridging Fault Resistance

With the shrinkage in device dimensions, the signal paths run closer to each other. This increases the probability of shorts between adjacent paths. The inductive fault analysis performed in VLSI circuits found that bridging faults are a prominent fault type and appear to be one of the most important faults that causes large $I_{DDQ}$ [8]. Most previous researches on bridging faults testing, either logic testing or $I_{DDQ}$ testing, assume that the bridging resistance is zero.

However according to the analysis in [9], the bridge resistance (denoted as $R_{short}$) has a large impact on the testing results. The value of $R_{short}$ is
a distribution with the variation in defect size and material. Several types of test structure, e.g., serpentine and interleaved combs [10], can be used to measure the value of \( R_{\text{short}} \).

### 2.3 Parasitic Parameters

The other parameters which may affect the performance of the BICSs arisen from the parasitic capacitance or inductance are the decoupling capacitance \( C_{\text{EXT}} \), internal capacitance \( C_{\text{INT}} \), and pin inductance \( L_{\text{pin}} \).

- \( C_{\text{EXT}} \)
  
  The capacitor \( C_{\text{EXT}} \) is a decoupling capacitance shunt to the external power supply. It is well known that the faster the current changes the more delta-I noise it generates. The decoupling capacitor momentarily takes over the role of the power supply and provides charge to the chip until the potential level on the power bus settles down. Thus it will not affect the current status at \( V_{\text{GND}} \) node. However when a BICS is built at the \( V_{\text{DD}} \) location, \( C_{\text{EXT}} \) will be an important factor for the design of BICSs. The value of the decoupling capacitance must be selected so that it is large enough to minimize the transient noise [11].

- \( C_{\text{INT}} \)
  
  The capacitor \( C_{\text{INT}} \) is the total internal capacitance seen at \( V_{\text{DD}} \). It consists of the distributed capacitance of the interconnection lines, the transistor's parasitic capacitance, the on-chip decoupling capacitance, the compensation capacitance, etc. In [11] it is shown that \( C_{\text{INT}} \approx 1/10 C_{\text{EX}} \).

- \( L_{\text{VD}} \) and \( L_{\text{GND}} \)
  
  The inductive factor in signal line is a major factor in high speed circuit design, because even a low value inductor may cause a large voltage drop with a high current fluctuation. Sometimes these value are provided in the data sheet supplied by the component vendor [12]. Most of the inductance exists at the bonding wires, package pins and lead frames. For \( I_{\text{DDQ}} \) testing, we need only concern about these effects on the path that carry the power to or from the chip, i.e., the \( V_{\text{DD}} \) pin and \( G\text{ND} \) pin. We use \( L_{\text{VD}} \) and \( L_{\text{GND}} \) to denote these values.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{\text{EXT}} )</td>
<td>5</td>
<td>( \mu \text{F} )</td>
<td></td>
</tr>
<tr>
<td>( L_{\text{pin}} )</td>
<td>5</td>
<td>( \text{pH} )</td>
<td></td>
</tr>
<tr>
<td>( R_{\text{short}} )</td>
<td>20K</td>
<td>( \Omega )</td>
<td></td>
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</tbody>
</table>

Table 1 shows an example of the DC characteristics and some parameters of a CUT.

### 3 Case Study

In this section, we will show the application of the model on the design of BICSs. Here we choose the Favali's BICS scheme [2] as an example. Intuitively, this scheme (Figure 3) is very simple to design. Each gate requires two extra transistors (Q1 and M1) and the whole circuit requires another transistor (P1). All these transistors are used to convert an analog fault (i.e., those resulting \( I_{\text{DDQ}} \) faults) to a stuck-at fault. A test mode select line (N) is used to switch between the normal operation and the test operation. If the circuit is fault free, then at the normal mode (\( N=1 \)) the voltage at node \( V_{\text{I}}-V_{\text{GND}} \) is \( G\text{ND} \), while in the test mode (\( N=0 \)) signal \( E \) is \( V_{\text{DD}} \) because PMOS P1 is conducted. However, any \( I_{\text{DDQ}} \) fault which causes one of the \( V_{\text{I}}-V_{\text{GND}} \) nodes higher than \( G\text{ND} \) will result in \( V_{\text{E}} \) logic at \( G\text{ND} \).

Figure 4 shows the performance comparison of the Favalli's scheme under different \( R_{\text{short}} \). The upper curve represent the waveform of the \( I_{\text{DDQ}} \) and \( I_{\text{DDT}} \). The center curve represents the waveform of the signal N. The lower curves show the voltage waveforms at node E, where solid line and dash line are the simulation results for \( R_{\text{short}} = 2K\Omega \) and \( R_{\text{short}} = 200\Omega \), respectively. We can find that, when \( R_{\text{short}} = 200K \) this scheme cannot detect the \( I_{\text{DDQ}} \) fault because the flag E almost keeps at logic 1.

Figure 5 shows the performance comparison under different dimensions of \( M_n \) (\( W=100\mu \text{m} \) and \( W=20\mu \text{m} \)). The upper two curves are the same as that shown in Fig. 4. The third panel shows the voltage waveforms at node E for dimension \( W=100\mu \text{m} \) (solid line) and \( W=20\mu \text{m} \) (dash line). We can find that the dimension of transistor \( M_n \) seems have no effect on the testing results. The lower curves show the voltage waveforms at the virtual node \( V_n \) (node number 200). We can find that the voltage of \( W=100\mu \text{m} \) (solid line) at this node is lower than that of \( W=20\mu \text{m} \) (solid line). However both of them are still under the specification of \( V_{\text{IL}} \) and \( V_{\text{OL}} \) as that shown in Fig. 1.

Table 2 shows the performance comparison for the conditions "without" using the model and "with" the model. We can find that the simulation time with the model applied is dramatically decreased.

<table>
<thead>
<tr>
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<th>Value</th>
<th>Unit</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ \text{IN} } )</td>
<td>2.5</td>
<td>V</td>
<td>( V_{ \text{DD} }=5\text{V} )</td>
</tr>
<tr>
<td>( V_{ \text{IL} } )</td>
<td>-0.5</td>
<td>V</td>
<td>( 0.8 )</td>
</tr>
<tr>
<td>( V_{ \text{OH} } )</td>
<td>2.5</td>
<td>V</td>
<td>( V_{ \text{DD} }+0.5 \text{V} )</td>
</tr>
<tr>
<td>( V_{ \text{OL} } )</td>
<td>-0.5</td>
<td>V</td>
<td>( 0.8 \text{V} )</td>
</tr>
<tr>
<td>( \text{IDDQ} )</td>
<td>400\mu</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>( \text{IDD} )</td>
<td>2.5m</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>( C_{\text{EXT}} )</td>
<td>5</td>
<td>( \mu \text{F} )</td>
<td></td>
</tr>
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<td>( R_{\text{short}} )</td>
<td>20K</td>
<td>( \Omega )</td>
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</table>
4 Conclusion

A current mode fault model for representing the circuit behavior of digital CMOS circuit is proposed. A formal translation method to translate from any given digital CMOS CUT to this model is outlined. With this model, both of the CUT (digital) and BICS (analog) can be concurrently designed. The "concurrent engineering" can be executed through the help of this model. Thus these can make the design of BICSs more efficient and reliable.

References


