World Applied Sciences Journal 3 (6): 974-978, 2008
ISSN 1818-4952

Design of a Novel Reversible Multiplier Circuit Using HNG Gate in Nanotechnology

[1]Majid Haghparast, [1]Somayyeh Jafarali Jassbi, [2]Keivan Navi and [2]Omid Hashemipour

[1]Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
[2]Faculty of Electrical and Computer Engineering, Shahid Beheshti University, Tehran, Iran

Abstract: Reversible logic circuits are of interests to power minimization having applications in low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. In this paper we propose a novel 4x4 bit reversible multiplier circuit. The proposed reversible multiplier is faster and has lower hardware complexity compared to the existing counterparts. It is also better than the existing counterparts in term of number of gates, garbage outputs and constant inputs. Haghparast and Navi recently proposed a 4x4 reversible gate called "HNG". The reversible HNG gate can work singly as a reversible full adder. In this paper we use HNG gates to construct the reversible multiplier circuit. The proposed reversible multiplier circuit using HNG gate can multiply two 4-bits binary numbers. The proposed reversible 4x4 multiplier circuit can be generalized for NxN bit multiplication. We can use it to construct more complex systems in nanotechnology.

Key words: Reversible logic gates . reversible logic circuits . reversible multiplier circuits . quantum computing . nanotechnology based systems

INTRODUCTION

One of the major goals in VLSI circuit design is reduction of power dissipation. As demonstrated by R. Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss [1]. It is proved that the loss of each one bit of information dissipates at least KTln2 joules of energy (heat), where $K=1.3806505x10^{-23}m^2kg^{-2}K^{-1}$ (joules $Kelvin^{-1}$) is the Boltzmann's constant and T is the absolute temperature at which operation is performed [1]. Reversible logic circuits have theoretically zero internal power dissipation because they do not lose information. Hence,. In 1973, Bennett showed that in order to avoid KTln2 joules of energy dissipation in a circuit, it must be built using reversible logic gates [2]. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e. not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs [4-6]. Thus, the number of inputs and outputs in reversible logic gates or circuits are equal. Such gates or circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [3-5]. Reversible logic has received significant attention in recent years. It has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology. It is not possible to construct quantum circuits without reversible logic gates. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits because in a reversible logic circuit, we are not allowed to use fan-out and feedback [4].

A reversible logic circuit should have the following features [5]:

- Use minimum number of reversible gates.
- Use minimum number of garbage outputs.
- Use minimum constant inputs.

The output that is not used for further computations is called garbage output [6]. The input that is added to an nxk function to make it reversible is called constant input [7].

Multiplication is a heavily used arithmetic operation in many computational units. It is necessary for the processors to have high speed multipliers. In this paper, a novel reversible multiplier circuit using reversible HNG gates is presented. We show that the

Corresponding Author: Majid Haghparast, Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran

proposed reversible multiplier circuit is better than the existing designs in term of number of gates, number of garbage outputs, number of constant inputs and hardware complexity.

MATERIALS AND METHODS

Reversible logic: An n-input n-output function F is said to be reversible if there is a one-to-one correspondence between the inputs and the outputs. Therefore, the input vector can be uniquely determined from the output vector.

Reversible logic gates: An nxn reversible gate can be represented as:

$$I_V = (I_1, I_2, I_3, \ldots, I_n)$$
$$O_V = (O_1, O_2, O_3, \ldots, O_n)$$

Where I_V and O_V are input and output vectors respectively. Several reversible logic gates have been proposed in the past years. Between them are: Feynman gate, FG [8], Toffoli gate, TG [9], Fredkin gate, FRG [10], Peres gate, PG [11], New Gate, NG [12], TSG gate, TSG [6], MKG gate, MKG [13] and HNG gate, HNG [15]. In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies.

Feynman gate (FG), also known as controlled-not gate (1-CNOT), is a 2x2 reversible gate that can be described by the equations: P=B and Q=A⊕B, where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

Toffoli gate (TG), also known as controlled controlled-not (CCNOT), is a 3x3 reversible logic gate. The Toffoli gate can be represented as:

$$I_V = (A, B, C)$$
$$O_V = (P = A, Q = B, R = AB \oplus C)$$

Where I_V and O_V are input and output vectors. The Toffoli gate is shown in Fig. 2.

Fredkin gate (FRG), also known as controlled permutation gate, is a 3x3 reversible logic gate. It can be represented as:

$$I_V = (A, B, C)$$
$$O_V = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Where I_V and O_V are input and output vectors. It is shown in Fig. 3. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input vector is the same as the Hamming weight of its output vector.

Peres gate (PG), also known as New Toffoli Gate (NTG), combining Toffoli Gate and Feynman Gate is a 3x3 reversible logic gate. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$$

Where I_v and O_v are the input and output vectors. The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

New gate (NG), is a 3x3 reversible gate. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = AB \oplus C, R = A'C' \oplus B')$$

Where I_v and O_v are the input and output vectors. The New gate is shown in Fig. 5.

TSG gate is a 4x4 reversible logic gate. The TSG gate is shown in Fig. 6, where each output is annotated with the corresponding logic expression.

MKG gate is a 4x4 reversible logic gate. The MKG gate can be represented as:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = C, R = (A'D' \oplus B') \oplus C,$$
$$S = (A'D' \oplus B').C \oplus (AB \oplus D))$$

Where I_v and O_v are the input and output vectors. The MKG gate is shown in Fig. 7, where each output is annotated with the corresponding logic expression.

HNG gate is a 4x4 reversible logic gate. The HNG gate can be represented as:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = B, R = A \oplus B \oplus C,$$
$$S = (A \oplus B).C \oplus AB \oplus D)$$

Where I_v and O_v are the input and output vectors. The HNG gate is shown in Fig. 8, where each output is annotated with the corresponding logic expression. The corresponding truth table of the HNG gate is depicted in Table 1. For more information about reversible logic gates see [13-16].

One of the prominent functionalities of the HNG gate is that it can work singly as a reversible full adder unit [15]. If $I_v = (A, B, C_{in}, 0)$, then the output vector

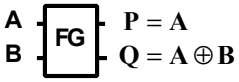

Fig. 1: Feynman gate

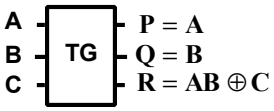

Fig. 2: Toffoli gate

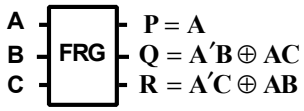

Fig. 3: Fredkin gate

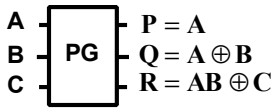

Fig. 4: Peres gate

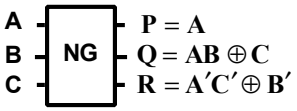

Fig. 5: New Gate (NG)

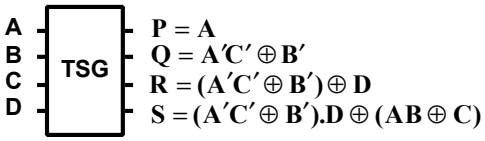

Fig. 6: TSG gate

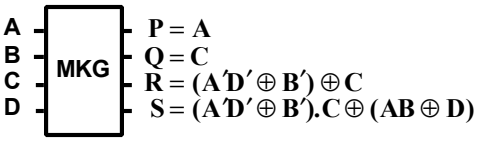

Fig. 7: MKG gate

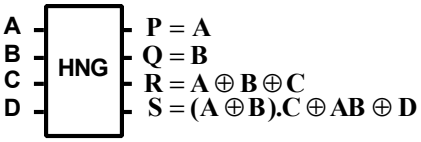

Fig. 8: Reversible HNG gate in [15]

becomes: O_v=(P=A, Q=C_{in}, R=Sum, S=C_{out}). Therefore, we have both of the required outputs. Implementation of the HNG gate as the reversible full adder is shown in Fig. 9. The proposed reversible full adder circuit uses only one reversible logic gate. It produces only two garbage outputs. It requires only one constant input and it needs only one clock cycle to perform the operations [15]. It is proved that the proposed reversible full adder in [15] is better than the reversible full adder circuits in [6, 13] in term of hardware complexity [15]. Let

Table 1: Truth table of proposed reversible HNG gate in [15]

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

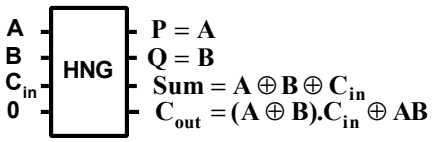

Fig. 9: Reversible HNG gate as a reversible full adder [15]

				x_3	x_2	x_1	x_0
			x	y_3	y_2	yx_1	y_0
				x_3y_0	x_2y_0	x_1y_0	x_0y_0
			x_3y_1	x_2y_1	x_1y_1	x_0y_1	
		x_3y_2	x_2y_2	x_1y_2	x_0y_2		
	x_3y_3	x_2y_3	x_1y_3	x_0y_3			
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig. 10: Partial products in a 4x4 multiplication

a = A two input EX-OR gate calculation
ß = A two input AND gate calculation
d = A NOT calculation
T = Total logical calculation

For [6]: T=6a+3ß+3d, for [13]: T=5a+3ß+3d and for [15]: T=5a+2ß. Thus, the proposed reversible full adder in [15] is better than the reversible full adder circuits in [6, 13] in term of hardware complexity [15]. We will use HNG gates to construct the novel reversible multiplier circuit.

A Novel Reversible Multiplier Circuit Using HNG gates: The operation of the 4x4 multiplier is depicted in Fig. 10. It consists of 16 partial product bits of the form $x_i.y_i$.

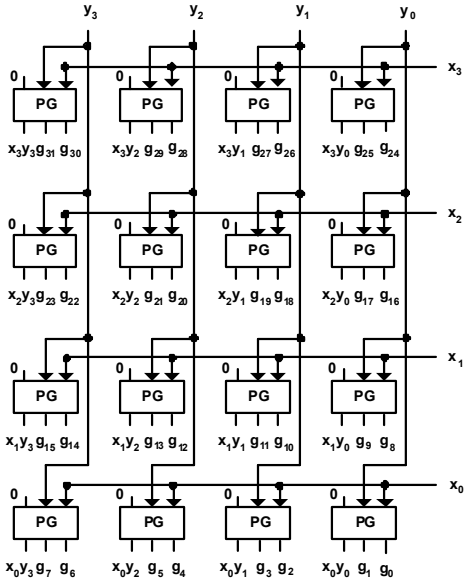

Fig. 11: Reversible partial products generation circuit using Peres gates [19]

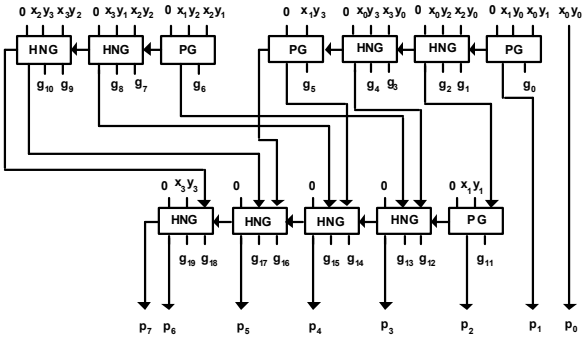

Fig. 12: Proposed 4x4 reversible multiplier circuit using HNG gates and Peres gates

Our proposed reversible 4x4 multiplier circuit has two parts. First, the partial products are generated in parallel using Peres gates as shown in Fig. 11. Then, the addition is performed as shown in Fig. 12.

The basic cell for such a multiplier is a full adder (FA) accepting three bits. We use HNG gates as reversible full adder which is depicted in Fig. 9. The proposed reversible multiplier circuit uses eight reversible HNG full adders. In addition, it needs four reversible half adders. It is possible to use HNG gate as half adder, but we use Peres gate as reversible half adder because it has less hardware complexity and quantum cost compared to the HNG gate.

RESULTS AND DISCUSSION

Evaluation of The Proposed Reversible Multiplier Circuit: The proposed reversible multiplier circuit is more efficient than the existing circuits presented in [17-19]. Evaluation of the proposed circuit can be comprehended easily with the help of the comparative results in Table 2.

Table 2: Comparative experimental results of different reversible multiplier circuits

	No. of gates	No. of garbage outputs	No. of constant inputs	Total logical calculation
This work	28	52	28	80a+36ß
[19]	28	56	32	92a+52ß+36d
[18]	29	58	34	110a+103ß+71d
[17]	40	56	31	80a+100ß+68d

The only difference between partial products generation block in our design with the existing designs in [17, 18] is the use of Peres gates instead of Fredkin gates. This structure is proposed in [19]. We use it because the Perse gates have less logical calculation and less quantum cost than the Fredkin gates.

One of the main factors of a circuit is its hardware complexity. We can prove that our proposed circuit is better than the existing approaches in term of hardware complexity.

Let

a = A two input EX-OR gate calculation
ß = A two input AND gate calculation
d = A NOT calculation
T = Total logical calculation

For [17] the Total logical calculation is: T=80a+100ß+68d, for [18] the Total logical calculation is: T=110a+103ß+71d, for [19] the Total logical calculation is: T=92a+52ß+36d and for our proposed reversible multiplier circuit, the Total logical calculation is: T=80a+36ß. Therefore, the proposed reversible multiplier circuit is better than the existing circuits in term of complexity.

Garbage output refers to the output of the reversible gate that is not used as a primary output or as input to other gates. One of the other major constraints in designing a reversible logic circuit is to lessen number of garbage outputs. Our proposed reversible multiplier circuit produces 52 garbage output, but the design in [17] produces 56 garbage outputs, the design in [18] produces 58 garbage outputs and the design in [19] produces 56 garbage outputs. So, we can state that our design approach is better than all the existing counterparts in term of number of garbage outputs.

Number of constant inputs is one of the other main factors in designing a reversible logic circuit. The input that is added to an nxk function to make it reversible is called constant input [7]. Our proposed reversible multiplier circuit requires 28 constant inputs, but the

design in [17] requires 31 constant inputs, the design in [18] requires 34 constant inputs and the design in [19] requires 32 constant inputs. So, we can state that our design approach is better than all the existing designs in term of number of constant inputs.

Comparing our proposed reversible multiplier circuit with the existing circuits in [17-19], it is found that the proposed design approach requires 28 reversible logic gates but the existing design in [17] requires 40 reversible gates and the existing design in [18] requires 29 reversible gates. So, the proposed circuit is better than [17, 18] in term of number of reversible logic gates, which is one of the other main factors in reversible circuit design. It is to be noted that the existing design in [19] also requires 28 reversible gates.

From the above discussion we can conclude that the propounded reversible multiplier circuit is better than all the existing counterparts.

CONCLUSION

In this paper, we presented a novel 4x4 bit reversible multiplier circuit using HNG gates and Peres gates. Table 2 demonstrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of gates, garbage outputs and constant inputs. Furthermore, the restrictions of reversible circuits were highly avoided. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology. All the proposed circuits are technology independent since quantum logic and optical logic implementations are not available.

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