Floorplanning for Partially-Reconfigurable FPGAs via Feasible Placements Detection

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Marco Rabozzi: marco.rabozzi@mail.polimi.it
Antonio Miele: antonio.miele@polimi.it
Marco D. Santambrogio: marco.santambrogio@polimi.it
Rationale and Novelty

• Problem statement
  – Given a partially-reconfigurable FPGA, find on-chip area constraints to meet the design requirements

• Novelty:
  – Efficient exploration of the solution space driven by tight LP relaxations of the problem
  – Control on the shapes and positions of allowed areas
  – Possibility to customize the objective function by giving an arbitrary cost to each different area
Floorplanning problem

• Given:
  – The FPGA description
  – A set $N$ of reconfigurable regions (RRs)
  – The resource requirements $\forall n \in N$

• Goal:
  – Find a rectangular area for each region, such that:
    • No two regions overlap
    • Complete tiles are covered
    • All the resource requirements are met
    • A given objective function is optimized
Proposed Approach

- Reconfigurable regions + Resource requirements
- FPGA
- Floorplan solution
- Feasible placements generation
- Possible regions placements
- MILP model
- MILP Solver
  \[ \min c_1^t x + c_2^t y \]
- Invalid and redundant placements
- User-defined linear Objective Function
MILP model overview

• Sets:
  – **N**: set of regions (A, B, C)
  – **P<sub>n</sub>**: set of feasible placements for region **n** (\(P_A=\{1,2,3\}, P_B=\{4,5\}, P_C=\{6,7\}\))

• Variables:
  – \(x_{n,p}\): binary variable set to 1 if and only if region **n** is assigned to placement **p**

• Constraints:
  – No conflicting placements
  – One placement for each region

\[
\begin{align*}
x_{A,1} + x_{C,7} & \leq 1 \\
x_{A,2} + x_{B,4} & \leq 1 \\
x_{B,5} + x_{C,6} & \leq 1 \\
x_{A,3} + x_{B,4} + x_{C,6} & \leq 1
\end{align*}
\]

Derived from a clique of size 3: tighter formulation + constraints compaction
Benchmark results

- 20 designs with different number of regions and device occupancy rates to test the effectiveness of the proposed approach (PA)

- Global wire length objective function to compare to [1] and [2]

- MILP solver execution time limited to 1800 seconds

<table>
<thead>
<tr>
<th># RR</th>
<th>Average wire length improvement w.r.t. [1]</th>
<th>Average execution time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>6.99%</td>
<td>7.48%</td>
</tr>
<tr>
<td>10</td>
<td>7.56%</td>
<td>12.05%</td>
</tr>
<tr>
<td>15</td>
<td>8.83%</td>
<td>19.46%</td>
</tr>
<tr>
<td>20</td>
<td>5.47%</td>
<td>19.98%</td>
</tr>
<tr>
<td>25</td>
<td>5.52%</td>
<td>19.84%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Occupancy</th>
<th>Average wire length improvement w.r.t. [1]</th>
<th>Average execution time (sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>70%</td>
<td>8.44%</td>
<td>19.87%</td>
</tr>
<tr>
<td>75%</td>
<td>5.49%</td>
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<tr>
<td>80%</td>
<td>6.20%</td>
<td>13.33%</td>
</tr>
<tr>
<td>85%</td>
<td>7.36%</td>
<td>9.56%</td>
</tr>
</tbody>
</table>

THANK YOU!
FOR ADDITIONAL QUESTIONS CONTACT ME
marco.rabozzi@mail.polimi.it
Feasible placements generation

• A placement $p$ for region $n$ is feasible if it covers all the resources required by region $n$ and does not overlap with user defined invalid areas

• Placements generation strategies:
  – $P_n$: all feasible placements
    • Provable optimal solutions
    • High exploration cost
  – $P_{n}^{irr}$: irreducible placements
    • Provable optimal solutions for area minimization
    • Preserve problem feasibility
    • Low exploration cost
  – $P_{n}^{w}$: width-reduced placements
    • Suitable for wire length optimization
    • Medium exploration cost

Examples of feasible placements

Requires: 3x $\square$ 1x $\square$

$\in P_{n}^{w}$: The width cannot be reduced
$\notin P_{n}^{irr}$: The height can be reduced

Invalid areas

$\in P_{n}^{w}$, $\in P_{n}^{irr}$: No possible shrinking

$\notin P_{n}^{w}$, $\notin P_{n}^{irr}$: The width can be reduced