Theoretical and Practical Aspects of IDDQ Settling - 
Impact on Measurement Timing and Quality

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Abstract

This paper discusses the parameters involved in making fast and reliable quiescent current (IDDQ or ISSQ) measurements, with particular attention to the test setup and the point of measurement. For that purpose a detailed theoretical and practical study was made of the IDDQ settling behaviour in function of proper measurement instrument positioning. The conclusions are that instrument positioning is a critical factor in function of achieving fast, high resolution, reliable and repeatable IDDQ measurements needed to support advanced decision making strategies and Nanotechnology IDDQ application, and that the use of add-on instrumentation offers the best perspectives to reach these goals.

1. Introduction

It is well known that defects affecting functionality or reliability manifest themselves in the supply (IDD) or ground (ISS) current behaviour of a device [1]. Quiescent current (IDDQ – ISSQ, in the remainder of this paper we will use IDD to refer to both the supply or ground current) testing is now well established and has been recognised as a test method required to assure high product quality and reliability and to achieve the automotive 0ppm targets. The use of transient or dynamic current (IDDT) testing is also being explored but real application is still floundering due to implementation difficulties.

The goals of this paper are to describe, quantify and demonstrate the impact of the test setup on the current settling and the overall performance of the IDDQ test strategy, and to propose solutions to cope with this and to come to an economical optimal IDDQ test implementation.

Fast high-resolution instrumentation and suitable test pattern generation tools are no longer show stoppers. In the past test setup related issues played only a minor role, being masked out by low performance test equipment, but with the arrival of high performance measurement hardware, they are now becoming dominant in function of further improving the test method and fully exploiting the potential of high performance measurement hardware, as will be demonstrated throughout this paper.

To assure proper and reliable IDDQ measurements one needs to wait till the current has reached its quiescent state what directly affects the measurement speed. Depending on the location in the supply path, the current settling behaviour varies significantly. The closer the instrument is placed to the Device Under Test (DUT), the faster and more repeatable the measurement can be done. The fact that the test setup and in particular the position of the measurement instrument plays a critical role in this is sometimes overlooked and excellent specifications of tools are sometimes mistaken as a guarantee that the specified precision and speed does automatically provide valid and accurate final data, regardless of loading, distance, interference and other conditions.

To better quantify this, a complete analysis has been done of the IDDQ settling behaviour, both theoretically, using realistic models, as well as practically, using industry proven IDDQ monitors. The performance of three IDDQ sensing solutions (on-chip, off-chip remote and off-chip local) has been compared using a mathematical analytic method (using a simplified model evaluated manually), a mathematical numerical method (Matlab), a simulation method (Spice) and finally by practical experiments.

It will be shown that the farther the DUT and IDDQ monitor are separated, the longer the IDD settling takes. Theoretical as well as practical results confirm that of the three types of instruments discussed, the use of a well positioned load board based off-chip IDDQ instrument is the most optimum solution.

The remainder of this paper is organised as follows. The next section gives a short background on available IDDQ measurement solutions and IDDQ measurement parameter considerations. The section thereafter lists and discusses the setups used and the results of calculations, simulations and measurements. In a final section conclusion are drawn.
2. Background

2.1 Overview of IDDQ measurement solutions

There are three main locations in the power supply path where IDDQ measurement tools can be placed: on-chip, when using built-in current sensors (BIC), off-chip located on the interface board when using add-on equipment (load board based module - LBM), or off-chip remote, when using ATE embedded measurement tools like a Parametric Measurement Unit (PMU) or Digital Power Supply (DPS) instrument, as illustrated in figure 1. Every location has its pros and cons as will be discussed further.

![Figure 1: Overview of IDDQ measurement points.](image)

- **On-chip instrumentation.**
  On-chip IDDQ measurements rely on the availability of a BIC. This approach only has to cope with the inherent on-silicon capacitance (figure 1, insertion point C), and it is not negatively influenced by any off-chip decoupling capacitance. There is only the DUT specific current settling to wait for and such solutions offer both fast (MHz - GHz) and sensitive measurements (nA-pA resolution). BIC solutions enable real time on-line and concurrent IDD testing as well. Despite their advantages, their linearity and accuracy are typically no better than 1 to 10% of the measurement range. The DUT might suffer a BIC induced supply voltage droop affecting signal timing. There is also the problem of BIC testability, the silicon overhead, need for extra pins/supply and it is not really established in the test industry.

- **Remote Off-chip instrumentation (ATE based).**
  ATE instrumentation based IDDQ measurements, using a PMU or DPS instrument, are easy to implement. A major drawback, as will be shown, is the remote position of the instrument (figure 1, insertion point A), as the distance between DUT and the IDDQ instrument can easily exceed 1 meter, considerably affecting current settling and performance specifications of the PMU, unless special precautions are taken that aversely affect measurement time. This approach is further sensitive to noise and interference and does only provide reliable and highly repeatable results when measurements are performed at low speed.

**Local Off-chip instrumentation.**
Using a LBM offers the best trade-off from an IDD settling perspective, but even then proper positioning of the instrument itself is of great importance. For optimal performance the instrument is to be placed near to the DUT (distance range of a few centimetres) and in-between the local on-pin decoupling caps and the global bulk decoupling (figure 1, insertion point B), so that it only drives the mandatory on-pin decoupling. This trade-off brings combined advantages, namely the flexibility and versatility of ATE based solutions combined with short measurement times (1-100µs), sensitiveness (nA-pA) and dedicated and optimized features easily supporting advanced IDDQ test strategies. They do not affect the DUT behaviour, have an application track record and enable future IDD measurement extensions. Disadvantages are that the implementation has to be foreseen on the interface board and that one instrument per measurement channel is needed not to degrade performance.

2.2. IDDQ measurement parameter considerations.

The basic requirement for a high quality and repeatable IDDQ measurement is (1) that the DUT is in a proper quiescent state (what is assured if proper IDDQ test vectors are deployed) and (2) that the current is settled prior to the start of the measurement. Not meeting the second part of the requirement means that it is not a quiescent current measurement from its definition and might result in an outcome that is inaccurate, unstable or even invalid. Especially when considering NanoTechnology IDDQ test applications, proper settling is a must to enable reliable detection of small defect induced current additions on top of large background leakage currents.

Secondly the supply current path must be able to cope with high transient current spikes, when the DUT changes state, avoiding DUT supply voltage droops affecting DUT behaviour. This poses the need for of a proper decoupling scheme. The amount of capacitive loading seen by the IDDQ instrument calls for driving capability and impacts current noise, negatively affecting IDDQ measurement resolution unless additional filtering is applied at the cost of measurement time.

Industrial case studies indicate that proper IDDQ test implementation requires tens to hundreds and sometimes even a few thousands of IDDQ test points. As such there is a need to be able to make the IDDQ measurement as good and as fast as possible.

Technology advances and modern delta-IDDQ methods place additional requirements to the IDDQ instrumentation [7]. Such methods still works well with an adequate 0.1% absolute accuracy error, but in addition the IDDQ monitor and the whole test setup must have excellent AC specifications, especially the signal to noise ratio must be...
in the order of 100 dB (0.001%) or more to enable to
distinguish very small \( \text{IDDQ} \) differences, to assure high
measurement stability and repeatability. If a high number
of test vectors are run and the measurement is too slow, the
\( \text{IDDQ} \) instrumentation will measure undesired drifts caused
by environmental changes rather than the actual delta-\( \text{IDDQ} \)
changes during the measurement.

3. Theoretical analysis & experimental results

A complete analysis was done to properly investigate
the \( \text{IDD} \) settling phenomenon. Realistic models considering
the dominating elements were used for the theoretical
analysis and real \( \text{IDDQ} \) monitors and circuits equivalent to
the models used for the practical experiments. The \( \text{IDD} \)
settling and its impact on the performance of the main
\( \text{IDDQ} \) sensing solutions (BIC, LBM, ATE) are compared
below using manual mathematical analytical/numerical
calculations, simulations and finally by real experiments.

To illustrate what was done only the most typical cases
are discussed, as a detailed discussion of the large amount
of complex data, obtained for various cases and conditions,
is beyond the scope of this paper. General conclusions are
however based on the overall results and the experiences
gathered.

3.1 Calculation setup & results

For the basic calculations a generic RLC circuit, as
shown in figure 2, excited by a pulse current source was
used. Although simple, it properly reflects the settling
behaviour in the time domain and allows an easy
understanding of the relations.

\[ \frac{d^2 i(t)}{dt^2} + \frac{R}{L} \frac{di(t)}{dt} + \frac{1}{LC} i(t) = 0 \]

The solutions to this equation are: \( i(t) = V_0 \frac{e^{-\alpha t}}{\beta L} \left( e^{\beta t} - e^{-\beta t} \right) \),
where \( \alpha = \frac{R}{2L} \) and \( \beta = \sqrt{\frac{R^2}{4L^2} - \frac{1}{LC}} \). There is a critical
resistance \( R = R_{CR} = \frac{L}{C} \), which results in the fastest
current settling, given by \( i(t) = V_0 \frac{e^{-\alpha t}}{\beta L} t \).

When \( R > R_{CR} \), \( \alpha > \omega_0 \) and \( \beta \) is real and positive then the
current settles slowly without any overshoot given by
\[ i(t) = \frac{V_0}{\beta L} e^{-\alpha t} \sinh(\beta t). \]

When \( R < R_{CR} \), \( \alpha < \omega_0 \) and \( \beta = j \sqrt{\omega_0^2 - \alpha^2} = j \omega \) then
the current behavior shows damped oscillations, essentially
prolonging settling and is described by
\[ i(t) = \frac{V_0}{\alpha L} e^{-\alpha t} \left( e^{j\omega t} - e^{-j\omega t} \right) = \frac{V_0}{\alpha L} e^{-\alpha t} \sin(\omega t) \]

With an angular frequency of \( \omega = \frac{1}{\sqrt{LC - 4R^2}} \).

These calculations demonstrate that an optimal serial
resistance \( R_{CR} \) exists, for which the circuit has the fastest
settling as illustrated by figure 3. This figure depicts the
dependency between settling time and serial resistance for
two cases: excitation pulse \( \text{IDD} = 1\, \text{A}, \, C = 1\, \mu\text{F}, \, L = 1\, \mu\text{H} \)
and \( \text{IDD} = 1\, \text{mA}, \, C = 100\, \text{nF}, \, L = 10\, \text{nH} \). The oscillations are
considered settled when the amplitude is below 0.1% of
the initial value (i.e. 1mA and 1\muA respectively). For the
100nF/10nH/1mA case the critical resistance is close to
500m\Omega, for the 1\muF/1\muH/1\text{mA} case the critical resistance is
about 1\Omega. Practically the setup related interconnection
resistance is function of different factors and cannot be
optimized only with regards to the critical value.

3.2 Simulation setup & results

The simulation model used is shown in figure 4. For the
simulation experiments the ideal pulse current source of
the calculation model is replaced by a fixed voltage source
and a MOSFET is used to generate the current pulse, better
matching reality. Subject to the simulation experiments
were nine basic component parameter combinations
reflecting realistic situations, as detailed in table 1.

\( C_L \) reflects the amount of decoupling capacitance seen
from a particular measurement position. \( R_s \) reflects the
combination of the interconnect resistance (series resistance)
and eventually an added "sense" resistor serving measurement purposes. In general: the higher the
switching current, the higher the amount of (total)
decoupling capacitance (\( C_L \)) needed and the lower amount
of series resistance that can be tolerated to prevent from the harmful supply voltage droop at the DUT pins. C\textsubscript{L} acts as a charge buffer for the transient current pulse. To compensate for voltage droops across the supply network typically use is made of supply sense lines. This is a slow type of compensation/regulation that cannot cope with the high frequency current spikes and therefore a sufficient amount of (distributed) decoupling is needed to assure reliable DUT operation.

Figure 4: IDDQ settling simulation setup

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
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<td>10m</td>
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<td>5</td>
<td>0.5</td>
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<td>10m</td>
<td>10μ</td>
<td>5</td>
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</tr>
<tr>
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<td>10m</td>
<td>1μ</td>
<td>5</td>
<td>0.5</td>
</tr>
<tr>
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<td>10</td>
<td>100p</td>
<td>5K</td>
<td>40</td>
</tr>
<tr>
<td></td>
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<td>10n</td>
<td>10</td>
<td>1μ</td>
<td>5K</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td>Remote</td>
<td>1μ</td>
<td>10</td>
<td>100μ</td>
<td>5K</td>
<td>40</td>
</tr>
<tr>
<td>Low (1μA)</td>
<td>On-chip</td>
<td>1n</td>
<td>1K</td>
<td>10p</td>
<td>5M</td>
<td>4K</td>
</tr>
<tr>
<td></td>
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<td>10n</td>
<td>1K</td>
<td>10n</td>
<td>5M</td>
<td>4K</td>
</tr>
<tr>
<td></td>
<td>Remote</td>
<td>1μ</td>
<td>1K</td>
<td>10μ</td>
<td>5M</td>
<td>4K</td>
</tr>
</tbody>
</table>

L\textsubscript{s} is distributed over power line length of 1mm, 1cm and 1m

V\textsubscript{DC} = 5.0 V

Table 1: Simulation Component parameters

Figure 5 shows a simulation plot, comparing the IDD behaviour at the three IDDQ observation points of interest considering a 1 mA IDDQ measurement range. In this example, the settling response for the 100mA transient pulse lasting 10μs and settling down to a 100μA IDDQ current is displayed. The plot is double logarithmic to properly display the several orders of difference between the excitation transient pulse’s high value and the low IDDQ value and to cover the high difference in settling time between on-chip and remote off-chip observation points. The simulation was performed using the medium range parameters from Table 1. The remote off-chip model also includes a realistic model of the interconnection, taking the parasitics of a 1m long connection into account. The plot subtracts the 100μA IDDQ level enabling to easily read the settling time needed to reach a 1μA boundary corresponding with 0.1% of the nominal full scale.

The rising edge of the transient pulse response indicates that the BIC sees a good transient response potentially suitable for I DDT test extension. An LBM solution also observes a reasonable transient behaviour, which can be further improved, if the 1μF loading is decreased to a still acceptable 100nF, when I DDT measurement extension is desired. However, using an ATE solution, the pulse does not even reach 100mA in 10μs time, so a fast or even medium speed measurement of a transient I DDT is not possible in this case.

The falling edge of the transient pulse indicates that the IDD on-chip is settling to its final IDDQ value very fast and reaches the 0.1% band within 1μs. As expected, in the LBM case more time is needed and a settling time of about 100μs is needed prior to taking reliable and accurate IDDQ measurements. An instrument placed remotely 1m away from the DUT needs to wait approximately 10ms before it can start to take IDDQ measurements with the desired 0.1% repeatability. The interconnection parameters and distributed decoupling of the remote off-chip setup act as a filter lowering and prolonging the transient pulse response, which really disqualifies this setup for possible I DDT measurement extension.

Since the used equivalent internal resistance of 10Ω of the LBM is relatively high compared to the impedance of the parasitic serial inductance, the response is rather damped and follows approximately the simple RC time constant equation (where R is the internal resistance of 10Ω and C is the decoupling capacitance), corresponding with the considerations in section 3.1.

For high range measurement solutions the inherent serial resistance of the measurement solutions no longer dominates the interconnect impedance. As such there is no longer a damping effect resulting in high overshoots and undershoots and damped oscillations visible in the transient behaviour. For low range measurement solutions, having a high internal resistance, the settling time becomes
larger. These effects are confirmed by both the simulations and theoretical calculations.

3.3 Measurement setup & results

Most published papers on IDDQ measurement solutions are based only on a theoretical analysis or on simulations and most of the solutions presented were never validated in an industrial environment. Having available the necessary means, the challenge was taken to compare the theoretical results with practical ones.

Firstly, the earlier described simulation model (figure 4) was implemented by soldering discrete SMD components to keep minimal distance for LBM and BIC equivalents. Next the performance of various cases was measured using additional laboratory equipment. The results shown in figure 6, as a typical example, correspond well with the simulated results shown in figure 5.

![Figure 6: IDDQ settling – experimental results](image)

Next real IDDQ monitors were used instead of discrete model elements and the performance was again verified. The QD-1011 [8], a proven industrial IDDQ monitor, was used for off-chip solution experiments positioned in both local and remote locations. Since the QD-1011 can act as an embedded ATE solution as well as an LBM, it was much easier to compare the results of the same instrument positioned differently rather than comparing two different types of IDDQ instrumentation, what is outside the scope of this paper. For the LBM case the QD-1011 is located on the interface board close to the DUT (distance of about 1 cm). Figure 7 shows the LBM setup using a dedicated small tester, used to control the QD-1011 and the IDD current, while the settling response was evaluated using a digital storage scope and digital multimeters, further supported by results from the QD-1011 itself.

Since QD-1011 has buffered analogue output as well as digital readout ability, it was no problem to verify that the results obtained by monitor itself closely matches the results of the SMD component model, just the response was slightly delayed due to additional filtering present inside the monitor.

Emulating the ATE case was done by positioning the QD-1011 close to power supply and using a 1 m long power line to connect it to the interface board carrying the DUT. Four different types of power lines were considered namely: a shielded coaxial cable, an unshielded flat cable, PCB supply planes and a wire loop. The related parasitics of each of the setups, serial inductance and parallel capacitance, were measured to ensure that the parameters in the different models used correspond with reality. The lowest parasitics and the fastest transient performance is obtained when using PCB planes, while the best resolution is reached when using a shielded coaxial cable offering interference elimination. The wire loop exhibited the worst performance of all power connections.

![Figure 7: Measurement setup with QD-1011](image)

The BICMON [4] was used to represent the on-chip solution. However, BICMON has no digital readout ability (except a pass/fail bit) and the analogue output cannot be directly accessed, so the verification was done indirectly. Although digital storage scopes are not able to directly measure signals with differences of several orders of magnitude like present in the simulations, the practical results match relatively well the simulated results.

To further validate the results and in an attempt to eliminate the influence of instrument connections to the setup in a next stage of the investigation the digital scope was replaced by an in-line, industry proven IDDT transient monitor, namely the QT-1411 [8]. While digital oscilloscopes have usually an 8 bit resolution, hardly covering 2 orders of magnitude, the QT-1411 offers true 14-bit resolution enabling to cover over 4 orders of magnitude making it suitable to distinguish between the high IDDT transient pulse and the low IDDQ level.

The outcome of these experiments confirmed the proper matching of the theoretical, simulation and practical results.

3.4 Performance of a generic resistor IDDQ sensor

Taking the above into consideration this section investigates whether or not a simple sense resistor serves as the base for good IDDQ measurement instrument.
RS and inductance LS in the supply path, which require to DUT is inherently associated with a higher serial resistance and vice-versa. A higher distance between instrument and signal to noise ratio generating less accurate IDDQ resistance (sense resistor) is required, resulting in reduced droop [3]. A simple 10mΩ solution can make measurements a few orders faster and provide even more accurate results than ATE embedded instrumentation.

Due to its positioning, LBM solutions can in the same way make hundreds to thousands of IDDQ measurements, enabling high IDDQ fault coverage and supporting advanced IDDQ test strategies as well as additional test optimization approaches, in contrast to ATE based instrumentation that in the same time only can make a limited number of measurements resulting in only a poor IDDQ coverage.

Although this paper deals primarily with the settling of the quiescent current and its impact on the measurement, similar conclusions are valid also for transient current measurements, where the requirement for short distance DUT to IDDQ monitor is even more critical in order to eliminate parasitics and distortion of the transient current.

### References


[8] Datasheets of QD-1011 and QT-1411 available on the website www.qstar.be

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**Table 2: Performance of simple sense resistor as IDDQ sensor versus dedicated local off-chip monitor**

Table 2 summarises the performance of current sensors based on using different simple sense resistors (in function of the target measurement range) with a typical loading capacitance of 1µF. From the data it can be seen that using a simple sense resistor does not satisfy the contradictory IDDQ measurement requirements (high-speed and at the same time high-resolution). A simple 10mΩ sensor enables fast settling time but at the same time it has a very poor SNR caused by the need for very high amplification, resulting in poor resolution. A 10Ω sensor offers reasonable SNR, but it causes an unacceptable voltage drop for high switching currents. A 1kΩ sensor is completely unacceptable from voltage perspective and makes only sense when the IDDT is very low. In contrast a solution like the QD-1011 combines the best of all three solutions mentioned. It uniquely combines the advantages of the 3 resistors listed above. Its compensated bypass allows to carry the transient current with an equivalent internal resistance less than 10mΩ, the IDDQ settling corresponds to a 10Ω resistance and its SNR approaches that of a 1kΩ resistance.

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Rs</th>
<th>C_L</th>
<th>f</th>
<th>BW</th>
<th>G</th>
<th>V_IN</th>
<th>V_OUT</th>
<th>SNR_db</th>
<th>V_diss</th>
<th>V_diss sett</th>
<th>SNR %</th>
</tr>
</thead>
<tbody>
<tr>
<td>RS=10mΩ</td>
<td>0.01</td>
<td>1 E-08</td>
<td>1</td>
<td>16</td>
<td>10k</td>
<td>10</td>
<td>16-01</td>
<td>20</td>
<td>0.001</td>
<td>1µ (70%)</td>
<td>10</td>
</tr>
<tr>
<td>RS=1kΩ</td>
<td>10</td>
<td>1 E-05</td>
<td>10k</td>
<td>10</td>
<td>16-04</td>
<td>80</td>
<td>1</td>
<td>7</td>
<td>70</td>
<td>0.01</td>
<td></td>
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<tr>
<td>RS=1kΩ</td>
<td>1kΩ</td>
<td>1 E-03</td>
<td>160</td>
<td>1</td>
<td>16-06</td>
<td>100</td>
<td>(120)</td>
<td>5</td>
<td>(100)</td>
<td>7</td>
<td>0.001</td>
</tr>
</tbody>
</table>

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Although this paper deals primarily with the settling of the quiescent current and its impact on the measurement, similar conclusions are valid also for transient current measurements, where the requirement for short distance DUT to IDDQ monitor is even more critical in order to eliminate parasitics and distortion of the transient current.

## 4. Conclusions

The paper clearly demonstrates that issues inherent to the test setup, such as the IDDQ settling phenomena, determine the overall IDDQ measurement performance (speed and accuracy) and influence as well the application of IDDQ testing for NanoTechnologies..

Due to the current setting the distance between the instrument and the DUT has a big impact on the current measurement. The higher the value of the RLC combination, seen by the instrument, the longer the IDDQ settling time and the lower the IDDQ measurement speed and vice-versa. A higher distance between instrument and DUT is inherently associated with a higher serial resistance Rs and inductance Ls in the supply path, which require to be decoupled effectively by a higher value of parallel capacitance C_l.

To efficiently drive a high capacitive load a low series resistance (sense resistor) is required, resulting in reduced signal to noise ratio generating less accurate IDDQ measurements. Theoretical as well as practical results confirmed that interface board based IDDQ measurement solutions can make measurements a few orders faster and

<table>
<thead>
<tr>
<th>Description</th>
<th>Unit</th>
<th>Value</th>
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<tbody>
<tr>
<td>Sense resistor</td>
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<tr>
<td>Loading capacitance</td>
<td>F</td>
<td>1000</td>
</tr>
<tr>
<td>RC time constant</td>
<td>n</td>
<td>1</td>
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<td>-3dB bandwidth</td>
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<tr>
<td>Amplifier gain</td>
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<tr>
<td>Input voltage noise density</td>
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<td>Total output voltage noise</td>
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<tr>
<td>Signal to noise ratio</td>
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<tr>
<td>Voltage drop caused by Rs</td>
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<td>Settling time caused by Rs</td>
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<tr>
<td>Signal to noise ratio</td>
<td>%</td>
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</table>

Voltage drop is related to IDDT= 100mA and Settling time to IDDQ = 1mA +/- 0.1% (+/-1µA). LS = 10nH

Values in brackets are the theoretically calculated results replaced by realistic experimental results. Red values indicate unacceptable performance.