A comparative study of charge pumping circuits for flash memory applications

O.Y. Wong *, H. Wong, W.S. Tam, C.W. Kok

Department of Electronic Engineering, City University of Hong Kong, Tat Chee Avenue, Kowloon, Hong Kong, China

Article info

Article history:
Received 15 September 2011
Accepted 30 September 2011
Available online 1 November 2011

Abstract

Flash memories are now widely used in many portable electronic devices, in embedded systems and are even as replacement for computer hard disks. In flash memory systems, high-voltages (up to about 10 V) are indispensable for programming operations. In many cases, however, such programming voltages are not directly available from the supply, and are usually generated by embedded voltage converting or charge pumping circuits. These circuits produce the required programming voltage from available external supplies with voltages in the approximate range of 1–5 V. The power conversion efficiency, the chip size, the voltage regulation, as well as the loading characteristics have been the major concerns for such circuits. The present paper discusses some recently proposed charge pumping circuits for flash memory applications. We focus on the effects of the dynamic gate control, the 4-phase gate-boosting and cross-coupled configuration for enhancing the performance of the charge pump circuits. Several different charge pumps operated under different working conditions are then investigated in detail.

1. Introduction

Flash memory is a dominant non-volatile memory component nowadays. Its attracting features includes small size, high density, high robust, lost cost and simple accessory circuits. It has been widely used in portable electronic devices like cellular phones, digital music player and digital cameras, for many years. As its fabrication process is compatible with that of the mainstream CMOS technology, it has also been used in many embedded systems and micro-controllers for microcode storage. Recently, the use of flash memory as solid-state drive (SSD) to replace the hard disk in personal computers has also become very popular. SSDs were also introduced into high-end systems such as enterprise...
data center [1]. It is expected that the market of flash memory will continue to grow and constitute up to 12% share of the total semiconductor market in 2015 [2].

Charge pump is an indispensable component in a flash memory module [3–5]. The need of charge pump in flash memory systems is due to the mismatch between the supply voltage of the CMOS technology and the write/erase voltage of the flash memory cells. In digital CMOS circuits, low operation voltage is preferred because of the power consumption and the constant electric field scaling consideration. The operation voltages are expected to be reduced further in coming technology node [6]. However, the write and erase operation of flash memory required a high electric field to inject or to remove the charges from an isolated charge storage. Fig. 1 shows the supply voltage of CMOS technology and the write/erase (W/E) voltage of NOR and NAND type flash memories over the past years. The W/E voltages of the flash memory cells are much higher than the CMOS supply voltage and the down scaling also moves in a much slower pace when compared with the CMOS supply voltage scaling. Hence, different charge pumps are needed in the peripheral circuits associated to the memory cell array to step up or down the prescribed low supply voltage such that the write/erase operation of the cells is possible. Although several attempts have been introduced to reduce the W/E voltage of the flash memory, the W/E voltage is still much higher than the current CMOS supply voltage [5]. For example, the CMOS supply voltage is scaled down to 1 V in 2009 [7], but the W/E voltage of the SONOS memory cell, which is a kind of flash memory that allows a lower operation voltage [8], is still above 10 V for NAND-type and is about 5–7 V for NOR-type flash memory. It was reported that the W/E voltage in Fe-NAND flash memory can be greatly reduced to about 6 V [10,11]. Some new materials such as high-k-dielectric [12,13] and nanocrystallite or nanowire structure [13,14] are also reported to be able to reduce the W/E voltage. The voltages are still much larger than the normal operation voltage of state-of-the-art CMOS logics. Hence, charge pumping circuit is not only an indispensable component in the flash memory systems, but also a challenging issue in the design and process optimization [10,11,15–17].

The high W/E voltages were used in early non-volatile memory because of the use of thick isolating insulator. The voltages were significantly reduced after the use of ultrathin tunneling oxide [18]. In flash memory, the data are written and erased by means of injection and extraction of electrons to and from the floating gate or the charge trapping layer through two mechanisms - Channel Hot Electrons (CHE) injection and Fowler–Nordheim (FN) tunneling [19,20]. Maintenance of this energy barrier is important for charge retention in the floating gate or the charge trapping layer and thus the non-volatility of the data stored in the memory cells. Therefore, lowering these energy barriers (i.e. reducing the dielectric thickness) will decrease the data retention time although lower W/E voltage is possible. This is the reason for keeping high W/E voltage of the flash memory for many years. The intrinsic tunnel oxide thickness limit should be above 3 nm [18] otherwise the retention time will not be acceptable and that will be approached very soon (see Fig. 1). Hence, it is expected that the W/E voltage of flash memory cannot be scaled too low in the future technology nodes. On the other hand, some new non-volatile memory technologies such as Ferro-electric Random Access Memory (FeRAM), Magnetoresistive Random Access Memory (MRAM), Phase Change Memory (PCM) and Conductive Bridging Memory (CBRAM), also require a high W/E voltage [19].

Another advantage of using charge pump in flash memory systems is its fully-integration capability. It does not need any inductors and external capacitors. This property is superior for the flash memory to be used in portable devices that size is always one of the major concerns. Fig. 2 shows an example of the architecture of the NOR flash module [19]. Different charge pumps with different requirements are required to make the read, write and erase operations of the memory cell. To program the cells by CHE injection, a 3–5 V positive high power charge pump and a 6–9 V positive charge pump are required, respectively, to bias the bit line (BL) and word line (WL) voltages of the cell array. To erase the cells by FN tunneling, a 5–8 V positive charge pump is required for biasing the WL, source line (SL) and the well of the cells and a (−) 6–8 V negative charge pump is needed to generate the WL voltage. To read the cells, a regulated 2–4 V charge pump is needed to apply on the WL line. The design of these charge pumps becomes more challenge as the supply voltage available in the flash memory system has kept on decreasing. Conventional implementation of charge pump circuits is no longer suitable to be used in the modern flash memory systems that may operate at as low as 1 V. As mentioned in Refs. [10,11,15], the charge pumps have poor efficiency at low supply voltage. Hence, although the power consumption of the memory core decreases as a result of reduced supply voltage, the overall power dissipation may not be reduced accordingly. Moreover, as the ratio between the W/E voltage and CMOS supply voltage increases, it required more stages to be cascaded in order to generate the required voltages. This trend greatly increases the silicon area occupied by the charge pump and thus the size of the whole chip. Thus, different new charge pump topologies

Fig. 1. A plot of $V_{CE}$ of CMOS technology, W/E voltage and tunnel oxide thickness of NOR-type and NAND-type flash memories from 2001 to 2018. Data taken from Ref. [7].

Fig. 2. Architecture of NOR-type flash memory. Redrawn based on Ref. [16].
and structures are required in order to overcome these issues. In this paper, we will address the problems of conventional charge pump circuits. An overview on some proposed charge pump topologies and structures will also be given in Section 2. In Section 3, we shall critically discuss existing positive charge pump structures, we shall highlight the ways to improve the voltage gain including dynamic gate control, 4-phase gate-boosting and cross-coupled schemes with consistent circuit simulation. These results provide a reference for the selection of charge pump circuit under the constraints of efficient, loading current and chip size. Finally in Section 4 is a conclusion section where we further introduced some advanced charge pump circuits reported recently.

2. Overview on existing charge pump circuits

Charge pump is a kind of DC–DC converter that consists capacitors and a switch network controlled by some clock signals only. A high potential, either positive or negative, can be generated by the charge sharing actions among different capacitors during two or more clock phases. A high voltage is then developed at the output capacitor. The ideal voltage conversion ratio, \( M = \text{ideal output voltage/supply voltage} \), depends on the switch network configuration of the charge pump circuit. Higher \( M \) value can be obtained by cascading more unit stages, which usually has same configuration, in a charge pump circuit. Considering the relationship between the ideal voltage conversion ratio \( M \) and the number of cascaded stage \( n \), different charge pump topologies, such as linear with \( M = n \) [21–24], Fibonacci \((M = F_n, \text{where } F_n \text{ is equal to the } n\text{th Fibonacci number in the Fibonacci series})[25]\) and exponential \((M = 2^n)[26]\), have been proposed. Among these topologies, linear charge pump is the most popular one. In fact, linear charge pump is easier to be designed and implemented because the voltage difference between different stages is regular and relatively low, when compared with the others. Although much higher voltage gains can be achieved with fewer components in the Fibonacci and exponential topologies for the same \( n \) value, larger component size is required in these topologies in order to obtain the same performance as the linear ones [27,28]. Also, the components in these circuits are expected to withstand much higher electric field stress.

Among the literatures about the linear charge pump circuits, such as the heap pump [24], Cockcroft–Walton [21] and Dickson charge pump structures [22,23], most of them were concerned about the analysis, optimization methods, design and improved structure of the Dickson charge pump. Dickson charge pump structure has advantage of relatively smaller parasitic effect when compared with the heap pump and Cockcroft–Walton structures [29]. Hence, we shall concentrate on discussing this charge pump structure in this review. We shall discuss the positive charge pump structures in the following sections, unless has specifically mentioned as a negative charge pump structure. In fact negative charge pumps are similar to the positive ones in terms of operation principle and structure.

Fig. 3 shows a conventional Dickson charge pump structure. An opposite 2-phase clock signal is applied at the negative terminals of the coupling capacitors \((C_{1–4})\). Thus, each coupling capacitor (except the coupling capacitors in the first and last stages) is said to be charged by the pumping voltage from its previous stage during its charging phase \((\Phi_1 \text{ for the odd-numbered stages and } \Phi_2 \text{ for the even-numbered stages in Fig. 3})\) and pumped by the supply voltage during the pumping phase \((\Phi_2 \text{ for the odd-numbered stages and } \Phi_1 \text{ for the even-numbered stages})\). Accordingly, the charge can be transferred from the coupling capacitors on the input side to output capacitor of the charge pump as a result of charge sharing. Eventually, a high electric field will be developed at the output capacitor.

Conventionally, this kind of circuits was implemented using diode-connected NMOS switch network. It has two well-known problems. First, the high voltage is passed from one stage to the next stage and causes a threshold voltage drop. This threshold voltage drop reduces the voltage gain in each stage. Therefore, the conventional Dickson charge pump has low voltage gain. Second, the threshold voltage of the NMOS transistor across the diode-connected transistor chain increases from the input side to the output side due to the body effect [30]. In fact, the body effect exists in the NMOS switches of every positive charge pump circuit with \( M > 1 \) provides that it is implemented in N-well process because voltages higher than the supply have to be transferred by the switches and the substrates are always tied to the ground. The body effect further reduces the voltage gain per stage as the number of stage \( n \) increases. Eventually, the output voltage of the charge pump saturates and does not increase further even more stages are cascaded. Mathematically, the output voltage of Dickson charge pump circuit, \( V_{\text{out,Dickson}} \), without considering the parasitic capacitance and the loading current, can be modeled given by:

\[
V_{\text{out,Dickson}} = n \sum_{k=1}^{n} \{ V_{\text{DD}} - V_{\text{th}}(M_k) \} \\
= n \sum_{k=1}^{n} \left[ V_{\text{DD}} - \left( V_{\text{th}} + \gamma \left( \sqrt{V_{\text{th}}(M_k)} + 2\eta - \sqrt{2\eta} \right) \right) \right]
\]

where \( V_{\text{th}}(M_k) \) donates the threshold voltage of the \( k \)th diode-connected transistor, \( V_{\text{th}} \) is the threshold voltage for zero substrate bias, \( \gamma \) is the body effect parameter, \( V_{\text{sub}}(M_k) \) is the source-to-substrate biasing voltage of \( M_k \) and \( 2\eta \) is the surface potential for strong inversion. As shown in Eq. (1), the voltage gain is small because the accumulated threshold voltage drop per stage. Also,
$V_{sat}(M_k)$ increases with $k$ and makes the output voltage saturate easier. Hence, conventional Dickson charge pump is not suitable to operate at low supply voltage situation.

To avoid the threshold voltage drop problem in conventional Dickson charge pump structure, a better MOS transistor-based switch which is called as charge transfer switch (CTS) is proposed [31,32]. As shown in Fig. 4, with a better biasing signal applied at the gate of the CTS, the transistor is now biased in the linear region instead of saturation region in the diode-connected case. As a result, the charge can be transferred from one coupling capacitor to the other with negligible voltage drop and it can be shut down completely to prevent any reverse charge leakage. Unfortunately, to bias the transistors in a high voltage circuit is not as easy as that in low voltage circuits. Proper high voltage biasing signals are required for either N-type or P-type transistors. Thus, in order to achieve a high voltage gain, different charge pump structures must be used. The proposals include dynamic inverter, gate boosting and cross-coupling.

2.1. Dynamic inverters

As the CTSs in Dickson charge pump structure cannot be controlled efficiently by connecting their gates to a fixed node in the circuit. For example, the CTS in each stage of NCP1 [33] cannot be shut down completely by directly connecting its gate to the output of the next stage, a dynamic inverter is used to control the gate of each CTS. Dynamic inverter likes an ordinary inverter, except the source of both PMOS and NMOS are connected to two different nodes (see Fig. 5a). As a result, the voltages required to turn on or turn off the P-type/N-type CTSs in different clock phases can be passed dynamically from two different nodes in the charge pump circuit. A generalization of this strategy for the design of the dynamic inverters in a charge pump circuit is given in Ref. [34].

Here, some Dickson charge pump structures using this kind of dynamic inverters for CTS gate voltage control are discussed briefly. Wu and Chang [35] adopted N-type CTSs and connect the dynamic inverters in backward control configuration. That is, the signals connected to the dynamic inverter in a particular stage are taken from its latter stages. Two problems associated with this configuration. First, a diode-connected transistor chain is needed to be connected in parallel to the CTSs in order to establish the required initial node voltages; second, the threshold voltage drop at the output stage still exists as in the last stage, a diode-connected transistor is still in use. The existence of the diode-connected transistor chain will introduce extra silicon area as well as some parasitic elements to the circuit. The threshold voltage drop in the last stage might be eliminated by using PGI-1, PGI-2 or PGI-3 structures [36]. Alternatively, P-type CTSs together with the forward control scheme for the last two stages might be used [37]. That is, the signals connected to the dynamic inverters in the last two stages are taken from their previous stages instead of their latter stages. This method solves the threshold voltage drop issue. However, an additional diode-connected transistor chain is still required. Mensi et al. [38] proposed a charge transfer block scheme to solve this problem. In this circuit structure, the dynamic inverter is connected neither to the forward path nor the backward path. Thus, no any diode-connected transistor chain is needed. However, the threshold voltage drop in the last stage still cannot be resolved. Also, the overdrive voltages for the CTSs increase with the number of stages in this circuit and it increases the design complexity. To overcome both problems, Cheng et al. adopted a modified forward control scheme with P-type CTSs for all the stages [39]. In the forward control scheme, as the gate biasing control signals for the dynamic inverter only depend on the signals in its previous stages, it does not require any diode-connected transistor chain and no threshold voltage drop occurs at the output stage. In addition, the structure is more regular and that reduces the design complexity. Although using P-type transistors instead of the N-type transistors for the CTSs would occupy larger silicon area for the same on-resistance, using P-type CTSs in positive voltage charge pump circuits has the advantage of being allowable of using body-biasing schemes to resolve the body-effect problem, even only standard N-well process is used. The body-effect problem in charge pump circuit will be discussed later.

2.2. Gate boosting circuit

Gate boosting circuit consists of a small boosting capacitor and a transistor connected to the gate of the CTS (see Fig. 5b). As shown in Fig. 5b, when a clock signal is applied to the boosting capacitor, the gate voltages of the CTSs can be either stepped up or down. However, 4-phase clocking scheme is required for controlling the CTSs. Note that the sizes of the gate boosting capacitor and the additional transistor are comparatively small as compared to that of the coupling capacitor and the CTS, as the boosting circuit only needs to drive the gate capacitance of the CTS.

Fig. 4. Implementation of Dickson charge pump circuit using (a) N-type CTSs and (b) P-type CTSs.
Examples of charge pump structures with this gate boosting techniques are given below. Both positive [31] and negative [40] 4-phase gate-boosting charge pump structure were proposed. Again, as the control signals for the transistor of the boosting circuit are taken from its following stage, the threshold voltage drop occurs in the last stage. This problem can be solved by using N-type and P-type CTSs, respectively, for the negative and positive charge pumps [41–43]. To further improve the overdrive voltages of the CTSs from $V_{DD}$ to $2V_{DD}$, larger voltage swing of clock signals (0–$2V_{DD}$) was proposed to be used in the boosting capacitors [44,45]. It requires an extra silicon area and large power consumption for using the voltage doubler. A 2-phase clocking scheme instead of the 4-phase ones is also proposed [46]. In this circuit, the overdrive voltages of the CTSs are closed to zero and would have low current driving capability, however.

2.3. Cross-coupled structure

In fact, the gate of all the CTSs in a charge pump circuit may also be controlled effectively by the signals of its complementary section. This can be done by connecting two oppositely-operated charge pumps in parallel. That is, no any extra circuit is needed. Fig. 5c shows a cross-coupled structure based on this idea [47–50]. The gates of the N-type and P-type CTSs in each path are self-boosted directly by the outputs of coupling capacitors in its counter path. This configuration has the advantage of simple structure.

The body-effect issue in charge pump circuits can be alleviated by proper biasing of the body of the CTSs. As shown in Fig. 4a and b, three methods, namely floating-well [51], adoptive body biasing circuit [52], and body–source junction diode [53] may be adopted. However, all the three schemes require the implementation of either PMOS transistors in an N-well or NMOS transistors in a P-well. That is, the charge pump structures have to be implemented in a triple-well process in order to get rid of the body-effect. In the floating-well approach [51], the P or N-well is left floating. Although it is a simple method to erase the body-effect, the substrate leakage current may degrade the efficiency of the charge pump circuit [52]. Thus, adoptive body biasing circuits which eliminate the body-effect of a transistor by always connecting its body to the highest/lowest voltage (either drain or source terminal) was developed [52]. However, extra transistors are required. The body–source diode connection where the drain and the body of the transistor are connected together can also solve the body-effect [53]. With this connection, the CTSs in a charge pump circuit
can be completely shut down. When the CTSs turn on, the body-source junction diode can help to conduct once it is in forward-biasing. This approach has the advantages of simple, area-efficient and better conduction speed. These three approaches are illustrated in Fig. 6a–c.

In next section, we will investigate and compare the performances of the charge pump circuits using the aforementioned three methods. The voltage gain and power efficiency under different working conditions, area occupation, process requirement, gate-oxide reliability, as well as cascading capability, will be compared and discussed in detail based on some simulation results. These results provide some useful information on the choosing of the proper charge pump circuit to implement the high-voltage generation functional block in a particular flash memory system.

3. Characteristics comparison

In this section, we will look at the performance of three commonly used high voltage-gain positive charge pump circuits: dynamic biasing, gate boosting and cross-coupled structure. Total five charge pump structures are compared and the schematics of the unit cells are shown in Fig. 7a–e. The unit cells shown in Fig. 7a and b belong to the dynamic biasing charge pump structure [39], while the NMOS in the unit cell shown in Fig. 7a was configured via the body–source junction diode approach [53] in order to remove the body effect. The circuit in Fig. 7b does not employ any measure to overcome the body effect was also studied as a reference. They are labeled as DBCP1 and DBCP2 for convenience. Fig. 7c shows the unit cell with gate boosting technique [41–43]. It consists of PMOS transistors only and is donated as GBCP. Circuits in Fig. 7d and e belong to the cross-coupled structure [47–50]. The N-type CTSs shown in Fig. 7d adopt the body–source junction diode approach [53] to solve the body effect problem. The corresponding circuit that suffers from the body effect is depicted in Fig. 7e. These structures are donated, respectively, as CCCP1 and CCCP2. As mentioned in the previous section, all these charge pumps have a high voltage-gain and are free of threshold voltage drop as compared with the conventional one. Hence, these five circuits should mostly fulfill the stringent requirements of modern flash memory systems in terms of electrical characteristics. They are different in some other performances which are discussed in the rest of this section.

3.1. Simulation details

To compare the performance of these charge pumps, we redesign all the circuits based on an actual process. SMIC 0.18 μm CMOS process was used for the simulation. Different ideal voltage conversion ratios, M, were achieved by cascading different number of unit cells as shown in Figs. 8a–c. The unit cells of the dynamic biasing (DBCP1 and DBCP2), gate boosting (GBCP) and cross-coupled (CCCP1 and CCCP2) charge pumps are cascaded in the ways shown in Figs. 8a–c, respectively. The 2-phase and 4-phase clock drivers shown in Fig. 9a and b are used to provide the 2-phase clock signals for DBCP1, DBCP2, CCCP1 and CCCP2, and the 4-phase clock signals for GBCP. Table 1 lists all the details of these 5 charge pump circuits.
Fig. 8. Cascading topologies for (a) DBCP1/2, (b) GBCP, and (c) CCCP1/2.

Fig. 9. Schematics of (a) 2-phase clock driver for DBCP1/2 and CCCP1/2 and (b) 4-phase clock driver for GBCP.
To make a fair comparison, the following rules are used in the designs:

1. The total width(s) of the CTS(s) and the capacitance value(s) of the coupling capacitor(s) in each unit cell of different circuits are the same. It is because the driving capability in all the charge pumps can be increased by using larger CTSs and coupling capacitors. To have a fair comparison, the unit cells are designed such that the width of $M_{k,p,CTS}$ in Fig. 7a–c is equal to the sum of widths of $M_{k,a,p,CTS}$, $M_{k,b,p,CTS}$, $M_{k,a,n,CTS}$, and $M_{k,b,n,CTS}$ in Fig. 7d and e. This also means that silicon areas occupied by the CTS(s) and coupling capacitor(s) in each unit cell of the five circuits are almost the same.

2. The number of unit cell in these five charge pumps are so chosen that their ideal output voltages (under no loading condition) are the same.

3. A loading capacitor $C_{load}$ with capacitance value of 100 pF is connected to the output of for all the charge pumps.

4. The sizes of the transistors in the last stages of all the clock drivers are the same. In fact, the sizes of these transistors are critical to the charge pump performance as they are involved in the charging and discharging paths of the coupling capacitors.

The sizes of the transistors and capacitors in each unit cell of the five circuits are listed in Table 2. They are all so designed that almost full charge transfer among the coupling capacitors can be achieved under the same operation frequency of 10 MHz. The transistor and capacitor sizing’s are same for different stages unless specified otherwise. Ideal capacitors are used in the simulation. That is, the parasitic elements introduced by the coupling capacitors are not included in the simulation results. Duty clock cycle of 50% is assumed in the following analysis and simulation.

3.2. Simulation results

The simulated output voltages of DBCP1 ($n = 10$), DBCP2 ($n = 10$), GBCP ($n = 10$), CCCP1 ($n = 9$) and CCCP2 ($n = 9$) with different output currents at 1.5 V and 1.2 V supply voltages are plotted in Figs. 10 and 11, respectively. Note that same supply voltage is applied to $V_{DD1}$ and $V_{DD2}$, which are the supply voltages of the clock drivers in Fig. 9a and b and that of the core part of the charge pump circuits in Figs. 8a–c, respectively. The power efficiencies of DBCP1 ($n = 10$), DBCP2 ($n = 10$), GBCP ($n = 10$), CCCP1 ($n = 9$) and CCCP2 ($n = 9$) with different loading currents, with including or excluding the power dissipated by the logic circuits in the clock driver of each charge pump circuit, at 1.5 V and 1.2 V supply voltages, are plotted, respectively, in Figs. 12 and 13. The output voltages of these charge pump circuits are also simulated for different number of stage, $n$, under two different loading currents, 10 $\mu$A and 150 $\mu$A, at two supply voltages, 1.2 V and 1.5 V, and the simulation results are shown in Figs. 14–17.

3.3. Discussion

3.3.1. Output voltage

Fig. 18a depicts the operation of the $k$th and $(k + 1)$th stage of DBCP1 and DBCP2 during the time period $\Phi_2$ ($clk1 = V_{DD1}$ and $clk2 = 0$ V), where non-ideal elements including:

- the equivalent parasitic capacitance $C_P$ associated to the output node $o_{ck}$ of the coupling capacitor in the kth stage;
- the gate capacitance $C_{Gk}$ of the CTS in the kth stage;

### Table 1
Summary of the five charge pump circuits investigated in this paper.

<table>
<thead>
<tr>
<th>Name of charge pump</th>
<th>Unit cell</th>
<th>Cascading topology</th>
<th>Clock driver</th>
<th>Ideal output voltage (no load condition)</th>
<th>Ideal voltage conversion ratio, $M$</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBCP1</td>
<td>Fig. 6a</td>
<td>Fig. 7a</td>
<td>Fig. 8a</td>
<td>$nV_{DD1}$</td>
<td>$n$</td>
</tr>
<tr>
<td>DBCP2</td>
<td>Fig. 6b</td>
<td>Fig. 7a</td>
<td>Fig. 8a</td>
<td>$nV_{DD1}$</td>
<td>$n$</td>
</tr>
<tr>
<td>GBCP</td>
<td>Fig. 6c</td>
<td>Fig. 7b</td>
<td>Fig. 8b</td>
<td>$(n + 1)V_{DD1}$</td>
<td>$n + 1$</td>
</tr>
<tr>
<td>CCCP1</td>
<td>Fig. 6d</td>
<td>Fig. 7c</td>
<td>Fig. 8a</td>
<td>$(n + 1)V_{DD1}$</td>
<td>$n + 1$</td>
</tr>
<tr>
<td>CCCP2</td>
<td>Fig. 6e</td>
<td></td>
<td>Fig. 8a</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 2
Summary of the sizes of the transistors (and capacitors) in the unit cells of DBCP1/2, GBCP1/2 and CCCP1/2 in Fig. 6a–e, and the output stages of the 2-phase and 4-phase clock driver in Fig. 8a and b.

<table>
<thead>
<tr>
<th>Name of charge pump</th>
<th>Name of transistor/capacitor</th>
<th>W/L (µm/µm)/capacitance (pF)</th>
<th>Name of charge pump</th>
<th>Name of transistor/capacitor</th>
<th>W/L (µm/µm)/capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBCP1 (see Fig. 6a)/DBCP2 (see Fig. 6b)</td>
<td>$M_{k,p,CTS}$</td>
<td>20/0.22</td>
<td>GBCP (Fig. 6c)</td>
<td>$M_{k,p,CTS}$</td>
<td>20/0.22</td>
</tr>
<tr>
<td></td>
<td>$M_{k,a}$</td>
<td>1.5/0.22, 3/0.22 (for $k = n$)</td>
<td></td>
<td>$C_k$</td>
<td>0.5/0.18</td>
</tr>
<tr>
<td></td>
<td>$M_{k,b}$</td>
<td>8/0.22</td>
<td></td>
<td>$M_{k,a}$</td>
<td>5/0.22</td>
</tr>
<tr>
<td></td>
<td>$C_{a}$</td>
<td>30</td>
<td></td>
<td>$C_{a,1}$</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>$C_{b}$</td>
<td>15</td>
<td></td>
<td>$C_{a,2}$</td>
<td>0.8</td>
</tr>
<tr>
<td>CCCP1 (see Fig. 6d)/CCCP2 (see Fig. 6e)</td>
<td>$M_{k,a,p,CTS}/M_{k,b,p,CTS}$</td>
<td>2/0.18</td>
<td></td>
<td>Name of clock driver</td>
<td>Name of transistor</td>
</tr>
<tr>
<td></td>
<td>$G_{a}/G_{b}$</td>
<td>15</td>
<td></td>
<td>Name of clock driver</td>
<td>Name of transistor</td>
</tr>
<tr>
<td>2-phase clock driver (see Fig. 8a)</td>
<td>$M_{o,k}$</td>
<td>180/0.22</td>
<td>4-phase clock driver (see Fig. 8b)</td>
<td>$M_{o,k}$</td>
<td>180/0.22</td>
</tr>
<tr>
<td></td>
<td>$M_{o,k}$</td>
<td>45/0.18</td>
<td></td>
<td>$M_{o,k}$</td>
<td>45/0.18</td>
</tr>
<tr>
<td></td>
<td>$M_{o,k}$</td>
<td>60/0.22</td>
<td></td>
<td>$M_{o,k}$</td>
<td>60/0.22</td>
</tr>
<tr>
<td></td>
<td>$M_{o,k}$</td>
<td>15/0.18</td>
<td></td>
<td>$M_{o,k}$</td>
<td>15/0.18</td>
</tr>
</tbody>
</table>
the leakage charge $Q_{ke}$ flowing from the coupling capacitor $C_k$ to $\text{out}_{k-1}$ during the transition time (rising edge) of the clock signal applied to $C_k$;

- the finite on-resistance $R_{on}(M_{k,p,CTS}), R_{on}(M_{k,p,1})$ and $R_{on}(M_{k,n,1})$ of $M_{k,p,CTS}, M_{k,p,1}$ and $M_{k,n,1}$; and
- the equivalent resistance $R_{on,driver}$ added to the charge and discharging paths of the coupling capacitors by the finite on-resistance of the transistors in the output stage of the clock driver;

were considered in the simulation.

Note that the operation of the $k$th and $(k+1)$th stage of DBCP1/2 during $\Phi_1$ is just the same as that of the $(k+1)$th and $k$th stage during $\Phi_2$. The notations $Q(C_k, \Phi_{1/2}), Q(C_{pk}, \Phi_{1/2})$ and $Q(C_{ck}, \Phi_{1/2})$ denote the total charge flowing in/out of the coupling, equivalent...
parasitic and gate capacitance of the kth stage in \( \Phi_1 \) or \( \Phi_2 \). During the steady-state operation, the amount of charge flowing in and out of each capacitance during \( \Phi_1 \) and \( \Phi_2 \) should be the same [54]. With this consideration, together with the assumption that the complete charge transfer can be achieved among the coupling capacitors such that the voltage drop due to the on-resistance of the transistors along the charging and discharging paths is not important at this moment, and that the values of \( C_b \), \( C_p \), \( Q(C_b, \Phi_1/2) \), \( Q(C_p, \Phi_{1/2}) \), \( Q(C_g, \Phi_1/2) \) and \( Q_{E,k} \) for different \( k \) are the same due to their regular structures and donate as \( C, C_{DPBCP}, C_{QCp}, Q_{Cc}, Q_{Cg} \) and \( Q_{E}, \text{DBC}_{DPBCP} \). For simplicity, the output voltages of DBCP1 and DBCP2 can be expressed as:

\[
V_{o,DBC1/2} = V_{DD} + (n-1) \left( \frac{1}{C + C_{DPBCP}} \right) \left[ CV_{DD} - \frac{I_o}{f} - 2Q_{E,DBC} - 3Q_{Cc} \right] - Q_{Cc} C_{DPBCP}. \tag{2}
\]

where \( I_o \) is the loading current and \( f \) is the operation frequency of the charge pump. Similarly, for GBCP case, the operation status of the kth and \((k+1)\)th stages during \( \Phi_1 \), \( \Phi_2 \), \( \Phi_3 \) and \( \Phi_4 \) are depicted in Fig. 18b, with similar notations. \( C_b \) is the boosting capacitance in the gate boosting circuits of GBCP. Adopting the same mathematical approach, the output voltage of GBCP is derived as follow:

\[
V_{o,GBCP} = V_{DD} + (n-1) \left( \frac{CV_{DD}}{C + C_{GBCP} + C_g + C_b} - \frac{I_o}{f(C + C_{GBCP})} \right). \tag{3}
\]

For CCCP circuit, the operation of the kth and \((k+1)\)th stages during \( \Phi_k \) (\( clk1 = V_{DD} \) and \( clk2 = 0 \) V) is depicted in Fig. 18c with similar notations. The subscripts \( a \) and \( b \) in the notations donate the CTSs or capacitors in Path A and Path B of the circuit, as indicated in Fig. 7d and e. Note that \( C_{b,a} \) and \( C_{g,b} \) in Fig. 18c donate the total gate capacitance connected to the nodes \( N_{k,a} \) and \( N_{k,b} \) in the kth stage, which is the sum of the gate capacitance of the CTSs \( M_{a,n},CTS \) and \( M_{b,n},CTS \) and the sum of the gate capacitance of the CTSs \( M_{a,n},CTS \) and \( M_{b,n},CTS \) respectively. Again, with the same method and assumptions, the output voltages for CCCP1 and CCCP2 are derived as follow:

\[
V_{o,CCC1/2} = V_{DD} + n \left( \frac{1}{C + C_{CCC} + C_g} \right) \left[ CV_{DD} - \frac{I_o}{f} - Q_{CCC} \right]. \tag{4}
\]

where \( C \) (in Eqs. (2)–(4)) = \( 2C_{b,a} = 2C_{b,b} \), \( C_g \approx 2C_{g,a} = 2C_{g,b} \) for the transistor sizing shown in Table 2 and \( C_{CCC} = C_{b,a} = C_{b,b} \) for all \( k \).

From Eqs. (2)–(4), we can see that the output voltages of DBCP1/2, GBCP and CCCP1/2 can be represented by an equivalent circuit with a voltage source connected to an output resistor, as shown in Fig. 19. The equivalent values of \( V_{out} \) and \( R_{out} \) in Fig. 19 for different charge pump structures are listed in Table 3. Eqs. (2)–(4) are derived based on the assumption that the operation frequency is small enough such that the \( R-C \) time constants along the charging and discharging paths of the coupling capacitors are negligible and the complete charge transfer condition can be achieved. In this case, the on-resistance of the transistors along the paths can be neglected. However, if the \( R-C \) time constant is comparable to the charge transferring period of the paths, which is the usual case in a real situation, the value of \( R_{out} \) in Fig. 19 can be further modified as [43]:

\[
R_{out,mod} = \frac{\tau}{R_{out} C_{eq}}. \tag{5}
\]

where \( R_{eq} \) and \( C_{eq} \) are the equivalent resistance and capacitance along the charge transferring paths, and \( \tau \) is the charge transferring period for the coupling capacitors, which should be equal to \( 1/(2f) \) in the case of 2-phase clock operated with 50% duty (i.e., for the DBCP1/2 and CCCP1/2 case). For the 4-phase case (e.g., GBCP), \( \tau \) should be a little bit smaller than \( 1/(2f) \), depending on the non-overlap portions among the clock signals. Further note that the on-resistance of a transistor is given by:

\[
R_{on} = \frac{k_{pp}(W/L)}{4}\left[\frac{1}{I_{DS}} - \frac{1}{V_{thp} V_{DS}}\right], \tag{6}
\]

where \( k_{pp}(W/L) \) is the transconductance of the transistor, \( M_{pp} \), and it is proportional to the \( W/L \) ratio of the transistor. \( V_{thp} \) is the threshold voltage of the transistor, which depends on the source-to-body biasing voltage.

Considering Eqs. (2)–(6), we can see that the reduction on the voltage gain of a charge pump is caused by several factors including the charge sharing among the coupling, parasitic, gate and boosting capacitors, as given by the 2nd term in Eqs. (2)–(4), and 5th and 6th terms in Eq. (2), periodically charge sharing actions among the coupling capacitors to provide the loading current at the output as indicated in the 3rd term in Eqs. (2)–(4), and will further be modified by the relationships given in Eqs. (5) and (6) if the charge transfer is incomplete, as well as the reverse current flowing from the coupling capacitors on the high voltage side to that on the low voltage side during the clock transition as given in the 4th term in Eqs. (2) and (4). Under small loading current condition, it is expected that the internal voltage drop of a charge pump (see the 2nd, 4th to 6th terms in the equations and the term \( V_{thp} \) in Table 3) is more significant than the voltage drop due to the
output resistance of the charge pump (see the 3rd term and the $R_{out}$ in Fig. 19). On the other hand, when the loading current is large, the voltage loss in output resistance would be more significant.

Comparing the simulated output voltages of the five charge pump circuits under small loading current condition (see Fig. 10), it is observed that CCCP1/2, GBCP and DBCP1/2 can achieve the highest, moderate and lowest voltage gain, respectively. This observation can be explained by comparing the internal voltage drop caused by the circuit non-idealities in these structures. Considering the charge sharing effect among the coupling and parasitic capacitors in these circuits, smallest charge sharing effect is found in CCCP1/2 circuits as there is no any extra circuitries connected to the outputs of the coupling capacitors. That is, the total number of components connected to the output of each coupling capacitor is smallest among the circuits. Therefore, the equivalent parasitic capacitance at the output nodes of the coupling capacitors $C_{p,CCCP}$ in CCCP1/2 is smallest among the circuits. In DBCP1/2, the charge sharing effect between $C_{p,DBCp}$ and $C$ is large due to the large value of $C_{p,DBCp}$ contributed by the auxiliary components connected to the output of each coupling capacitor. Moreover, largest amount of charge is lost (or shared) from the coupling capacitor in each stage in order to charge the gate capacitor of the CTS through the dynamic inverter during the clock transitions because the voltage swings at the gates of the CTSs in this structure are as large as $\sim 3V_{DD}$, while that of GBCP and CCCP1/2 are about $2V_{DD}$ and $V_{DD}$ only. This voltage loss is indicated by the 5th and 6th terms in Eq. (2), where $Q_{cg}$ is approximately equal to $3V_{DD}C_g$. In GBCP circuit, the existence of an extra gate boosting capacitor $C_b$ connected with the coupling capacitor in each stage results in a large charge sharing loss between the coupling capacitor $C$ and the gate boosting capacitor $C_b$, as indicated by the 2nd term in Eq. (3). Note that $C_b$ is usually designed with a much larger capacitance value than that of $C_g$ in order to reduce the voltage drop at the gate of the CTS due to charge sharing effect. Considering the reverse currents in different charge pump circuits, the reverse current can be avoid in GBCP by a proper design of the 4-phase clock, as shown in Fig. 18b. That is why Eq. (3) does not include the $Q_b$ term. Comparing the reverse currents in DBCP1/2 and CCCP1/2 structures, the reverse current found in DBCP1/2 should be larger than that in CCCP1/2. This can be explained by comparing the charging/discharging paths of the gate capacitors of the CTSs in these two structures. During the clock transition, the output node of the coupling capacitor in the $k$th stage ($out_k$ in DBCP1/2 and $N_{k,a}$ in CCCP1/2) is coupled by $clk1$ signal to a higher voltage (see Fig. 20a and b). Once the output node of a coupling capacitor is pumped to a higher voltage by the clock signal ($out_k$ and $N_{k,a}$ in Fig. 20a and b), it should be isolated from the output node of the coupling capacitor in its previous stage ($out_{k-1}$ in DBCP1/2 and $N_{k-1,a}$) immediately by shutting down the CTS ($M_{k,p,CTS}$ in Fig. 20a and $M_{k,a,CTS}$ in Fig. 20b) connected in between them to prevent reverse charge; the time required to shut down the CTS(s) completely depends on how fast the gate capacitor of the CTS is charged (for PMOS) or discharged (for NMOS) to a required voltage level, which is in turn determined by the $RC$ time constant along the charging/discharging path. In the case of DBCP1/2 circuits, the existence of the resistance $R_{on}(M_{k,p})$ causes a large $RC$ time constant along the charging path of the gate capacitance $C_g$. Thus, the time for shutting down the CTS $M_{k,p,CTS}$ is comparatively long and large reverse current exists. On the other hand, as the gate capacitor $C_{g,k,a}$ is attached directly to the output node of the coupling capacitor $C_{p,DBCp}$, the reverse current is much smaller. The reverse current in the CCCP1/2 circuit is determined by the charging/discharging path of $C_g$. When the output node of the coupling capacitor is pumped to a higher voltage by the clock signal, the reverse current is determined by the $RC$ time constant along the charging path of $C_g$. Therefore, the reverse current in CCCP1/2 is much smaller than that in DBCP1/2. This is because the charging/discharging path of $C_g$ in CCCP1/2 is much smaller than that in DBCP1/2.
N_{k,a} and no resistance presents along the discharging path of the gate capacitance C_{g,k,a} in the case of CCCP1/2. Therefore, the gate capacitor C_{g,k,a} can be discharged quickly and M_{ina,CTS} can be shut down within a short time to stop the reverse current. In addition, the voltage swing at the gate capacitance C_{g,k} in DBCP1/2 is about 3V_{DD}, which is much larger than that at the gate capacitance C_{g,k,a} in CCCP1/2. Therefore, much longer time is expected to shut down the CTSs in DBCP1/2.

As far as the reverse current concerned, the magnitude of the reverse current in CCCP1/2 is smaller than that in DBCP1/2. It is because in CCCP1/2 circuits, 2 CTSs with larger on-resistance (the W/L ratios of the CTSs in the unit cell of CCCP1/2 are smaller than that in DBCP1/2, see Table 2) are connected in series between two adjacent coupling capacitors. On the other hand, only 1 CTS with smaller on-resistance is found in between two adjacent coupling capacitors. As a result, the reverse current loss in CCCP1/2 is smaller than that in DBCP1/2 (i.e., Q_{R,CCCP} > Q_{R,DBC}). Considering the output voltage drops due to both charge sharing effect and reverse current as discussed before, it can be concluded that the lowest output voltage can be obtained from DBCP1/2 circuits. The output voltages of GBCP and CCCP1/2 are comparable at small loading current. This conclusion agrees with the simulation result as shown in Fig. 10.

It should be noted that when the output current drawn from the charge pump increases, we should also consider the voltage drop due to the output resistance R_{out} of the charge pump circuit, as indicated in the equivalent circuit shown in Fig. 19. The variation of the output voltage V_o depends on how this output resistance varies with the loading current. As mentioned earlier, R_{out} of a charge pump is modified according to the function coth(τ/(R_{eq}C_{eq})) in Eq. (5), which indicates that if the R_{eq}C_{eq} value of the charge pump is much smaller than τ, the R_{out} value for different charge pump circuits are merely given by the expressions in Table 3. It does not depend on the on-resistance of the CTSs and the loading currents of the circuits. However, once R_{eq}C_{eq} is comparable to τ, the on-resistance can be increased significantly [53]. There is no problem if the value of R_{eq} for a charge pump circuit can always keep constant such that R_{out} is constant also. However, that is not the case in most of the charge pump circuits. R_{eq} varies under different working conditions in most charge pump circuits as it depends on the on-resistance of the transistors which may vary with the voltages at their gate, body and source terminals during

\[ V_o = V_{DD} \left( 1 - \frac{Q_{R,CCCP}}{Q_{R,DBC}} \right) \]
the operation. In the other words, the value of $R_{\text{req}}$ varies with the overdrive voltages of the CTSs in a charge pump circuit, in the way according to Eq. (6). The relationship among $V_{\text{ov}}$, $R_{\text{req}}$, and $R_{\text{out}}$ is illustrated in Fig. 21. This leads to the variation on the slope of the $V_{\text{ov}}$ characteristic of the charge pump (see Figs. 10 and 11). Considering the operation of the five charge pump circuits in Figs. 18a–c, the overdrive voltage(s) of the CTS(s) in the $k$th stage of DBCP1, DBCP2, GBCP, CCCP1 and CCCP2 are derived and listed in Table 3, where $D_{\text{V}}(C_k, U_{\text{x}})$ donates the magnitude of the voltage variation across the coupling capacitor $C_k$ during $U_{\text{x}}$. $V_{\text{th}}(M_k, p/n-\text{CTS})$ donates the threshold voltage of the CTS $M_k$, $p/n$-CTS in the $k$th stage, which will increase with the source-to-body biasing voltage in case body effect is present (see the case of CCCP2 in Table 3). When we compare the magnitudes of $V_{\text{ov}}$ in these charge pumps by assuming that the values of $C_{\text{pDBCP}}$, $C_{\text{pGBCP}}$, $C_{\text{pCCCP}}$, $C_g$ and $C_b$ are much smaller than that of $C$, the CTSs in DBCP1/2 should have highest overdrive voltages (the overdrive variation on the coupling capacitor $\Delta V(C_k, \Phi_{1/2})$ is usually small, compared to $V_{DD}$), and that in CCCP2 should have the smallest value due to the present of the body effect (indicated by the term $V_{\text{th}}(M_k, p/n-\text{CTS})/V_{SB}$). Therefore, $R_{\text{out}}$ for CCCP2 and DBCP1/2, respectively, have the largest and smallest slopes of the curves for CCCP2 and DBCP1/2 shown in Figs. 10 and 11. Further note that the NMOS $M_{k,\text{diff}}$ in the unit cell of DBCP2 is not used as the CTS in the charge pump (it is not included in the charging/discharging paths of the coupling capacitors). Hence, it has less influence on the output voltage performance of the charge pump even it suffers from the body effect. It leads to more or less the similar performance as that of DBCP1 shown in Figs. 10 and 11. When we look at the variation on the overdrive voltage with the loading current in these charge pump circuits, we can see that besides the GBCP structure, the overdrive voltages of the CTSs in the charge pumps decrease with increasing the loading current, and the reduction on $V_{\text{ov}}$ is more significant in CCCP1/2, especially when the supply voltage is low. It results in the increment of the $R_{\text{out}}$ value in these charge pump circuits when the loading current is large. That is why the slopes of the curves for DBCP1/2 and CCCP1/2 have some noticeable increases as the loading current increases. The change is most significant in the case when CCCP1/2 worked under low supply voltage. Hence, it is unfavorable for CCCP1/2 to be used at low supply voltage for a large load, especially in the case of CCCP2 which suffers from the body effect also. On the other hand, DBCP1/2 structures are more suitable to be used at low supply voltage with large loading current application because of the $2V_{DD}$ term in the expression of $V_{\text{ov}}$ in this structure. GBCP is also suitable for this application although the $V_{\text{ov}}$ value of this structure is only about half of that of DBCP1/2. This is because the $V_{\text{ov}}$ value of GBCP does not change with the loading current in this structure. This induction is confirmed with the simulation results shown in Figs. 10 and 11.

### 3.3.2. Power efficiency

The ideal power efficiency of a Dickson charge pump circuit can be expressed as:

$$P_{\text{eff, ideal}} = \frac{V_o I_o}{V_{DD} M_{t}} \times 100\%,$$

where $M$ is the ideal voltage gain of the charge pump. Details of Eq. (7) derivation can be found in Ref. [23]. Hence, if the output voltage of the charge pump $V_o$ is equal to $MV_{DD}$, 100% power efficiency can

---

**Fig. 18c.** Illustration showing the operation of the $k$th and $(k+1)$th stages of CCCP1/2 during $\Phi_2$ ($\text{clk}1 = V_{DD/2}$ and $\text{clk}2 = 0 \text{ V}$).

**Fig. 19.** Equivalent circuit for the output voltage of the charge pump circuit.
be achieved. However, current drawn from the supply is not always delivered to the load. It may charge some parasitic capacitances, or leaks away as reverse currents. This can be observed in Figs. 18a–c. For example, let’s consider the sum of the current flowing out of the coupling capacitor $C_k$ in Fig. 18a, which is equivalent to the current drawn from the supply ($clk1$ in Fig. 18a). Besides the current flowing towards $C_{k+1}$, which will finally be transferred to the output node as a loading current, additional currents (or charge) flow out of the coupling capacitor due to the existence of the reverse current $Q_{ck}$ and to charge the gate capacitance $C_gk$ and the parasitic capacitance $C_p$. This draws extra current from the power supply and accounts for the power loss due to internal power dissipation. Therefore, the power efficiency, which includes the internal power dissipation, is modified as:

$$P_{\text{eff}} = \frac{V_{oh}}{V_{DD}(I_{oh} + I_{loss})} \times 100\%,$$

(8)

where $I_{loss}$ is a lump sum of some extra currents drawn from the power supply. It includes the current required to drive the other logic circuits.

Let $I_{loss} = 0\,A$, Eq. (8) becomes:

$$P_{\text{pump eff}} = \frac{V_o}{MV_{DD}} \times 100\%.$$

(9)

It reduces to Eq. (7) and is considered as the pumping efficiency of the charge pump circuit. That is, the pumping efficiency is purely determined by the output voltage of a charge pump circuit and should be the maximum power efficiency that can be achieved by a charge pump circuit. It is expected that the power efficiencies of the five charge pump circuits more or less follow the same trend as that of the output voltages as discussed in the previous section. Fig. 22 plots the pumping efficiencies of DBCP1/2, GBCP and CCCP1/2 with different loading currents (obtained from the simulated output voltages in Fig. 10) and compares the pumping efficiencies with their simulated power efficiencies (including the power dissipated by the clock driver) at a supply voltage of 1.5 V. Here the power efficiencies are calculated according to the following expression:

$$\text{Power efficiency} = \frac{\text{power output}}{\text{power input}} \times 100\% = \frac{V_{I_{DD}}}{V_{DD}/2(I_{DD1} + I_{DD2})} \times 100\%,$$

(10)

where $I_{DD1}$ and $I_{DD2}$ refer, respectively, to the currents flowing through the sources $V_{DD1}$ and $V_{DD2}$, which are connected to the core part of the charge pump circuit and the corresponding clock driver. It is observed that the power efficiencies of all the five charge pumps follow closely with their pumping efficiencies (given by Eq. (9)) when $I_o$ is large. It is because the internal power loss caused by the $I_{loss}$ term in Eq. (8), is weak dependent on $I_o$ and becomes insignificant when $I_o$ is large. When $I_o$ is small, the internal power loss is the dominant power loss in a charge pump circuit and the power efficiency approaching zero when $I_o \sim 0\,A$. Comparing the power efficiency performance of different charge pump circuits in Figs. 12 and 13, we found that the power efficiency follows similar trends of the output voltage. However, when the loading current is very small, the power efficiency of GBCP drops to less than 50% even the pumping efficiency is as high as that in CCCP1/2. It indicates that the internal power loss in GBCP circuit is much greater than that of CCCP1/2. It is a disadvantage of the 4-phase clock-operated GBCP circuit. With the 4-phase clock operation, more clock transitions take place in each clock cycle (see Figs. 18a–c). Whenever a clock transition occurs, charging and discharging of some parasitic capacitance take place and cause a power loss. Therefore, the power efficiency of GBCP is much smaller than that of CCCP1/2 when the loading current is small, although output voltage may still maintain high. The simulation results also show that the CCCP1/2 circuits can achieve the best power efficiency among the other charge pump structures under the high supply voltage and low loading current situation. Up to 80% efficiency can be obtained even 9 stages cascading. On the other hand, we found that the power efficiency degradation due to the dynamic power dissipation on the clock drivers is only a few percent in all cases.

### 3.3.3. Area

Comparing the requirement of extra components (other than the CTSs and coupling capacitors), GBCP circuit requires one
transistor and one capacitor for the gate boosting circuits in each unit cell. In addition, since a 4-phase non-overlapping clock signal driver is required, the GBCP should consume the largest silicon area among the five charge pump circuits. For DBCP1 and DBCP2 circuits, only two extra transistors for the dynamic inverter and a simple 2-phase clock driver are required, and their sizes are moderate. CCCP1 and CCCP2 do not require any extra component. In addition, as the intrinsic voltage gain $M$ of this structure is higher than that of the other two by 1 (see Table 1). Fewer stages can be used to achieve the same conversion ratio. Thus, CCCP1/2 is the most area-efficient one among these circuit structures.

### 3.3.4. Process requirement and reliability problem

As discussed before, the body effect of the CTSs will seriously degrade the charge pump performance (comparing the curves of CCCP1 and CCCP2 in Figs. 10 and 11). A body-effect free positive charge pump circuit can be implemented by using the N-well process, if only PMOS is needed (e.g. GBCP). However, if N-type CTSs are needed in a positive charge pump circuit, triple-well process is unavoidable. CCCP1 circuit falls in the class and it requires extra masks and thus higher cost in fabrication.

As high electric field is often found in a charge pump circuit, it gives rise to some reliability issues of the transistors. The high electric field will cause hot-carrier effects which gives rise to the threshold voltage shift of the transistors [18]. The high-field will also cause a large gate leakage current [20,55] and in some cases may even cause the gate oxide to break down [56,57]. For the reliability point of view, charge pump structures with the smaller potential differences between the terminals of the transistors are more favorable. Here we investigate the maximum voltage difference across the gate, drain and source terminals of the transistors during the operation. For the CCCP1/2 structure, the maximum voltage difference between different terminals of the transistors is $V_{DD}$ while that for DBCP1/2 and GBCP are $2V_{DD}$. Therefore, the reliability of CCCP1/2 should be higher than that of the others. In fact, the CCCP1/2 structure is well-known with the advantage that it can be implemented using a low voltage process.

### 3.3.5. Cascading capability

A charge pump with high cascading capability in which the output voltage increases greatly with the number of stage $n$, is desirable. For the five high voltage-gain charge pump circuits, except
Table 4
Summary on the comparison of DBCP1/2, GBCP and CCCP1/2.

<table>
<thead>
<tr>
<th>Name</th>
<th>Voltage gain/power efficiency</th>
<th>Additional area for the auxiliary circuits</th>
<th>Process requirement</th>
<th>Reliability</th>
<th>Cascading capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBCP1</td>
<td>High VDD (1.5 V)</td>
<td>Small (I_o)</td>
<td>LOW FAIR (1 PMOS and 1NMOS per unit cell, 2 phase clock driver)</td>
<td>N-well process (the B–D/S junctions of the NMOS need to withstand high voltage)</td>
<td>POOR</td>
</tr>
<tr>
<td></td>
<td>Low VDD (1.2 V)</td>
<td>Large (I_o)</td>
<td>FAIR LOW (I_o)</td>
<td>FAIR (max. volt. diff. between D/S/(G = 2) VDD for all the transistors)</td>
<td>FAIR at low VDD and large (I_o)</td>
</tr>
<tr>
<td>DBCP2</td>
<td>High VDD (1.5 V)</td>
<td>Small (I_o)</td>
<td>LOW FAIR (1 PMOS and 1NMOS per unit cell, 2 phase clock driver)</td>
<td>Triple well process</td>
<td>POOR</td>
</tr>
<tr>
<td></td>
<td>Low VDD (1.2 V)</td>
<td>Large (I_o)</td>
<td>FAIR (I_o)</td>
<td>FAIR (max. volt. diff. between D/S/(G = 2) VDD for all the transistors)</td>
<td>FAIR at low supply volt. and large (I_o)</td>
</tr>
<tr>
<td>GBCP</td>
<td>High VDD (1.5 V)</td>
<td>Small (I_o)</td>
<td>FAIR LARGE (1 PMOS and 1 capacitor per unit cell, 4 phase nonoverlapped clock driver)</td>
<td>N-well process</td>
<td>GOOD</td>
</tr>
<tr>
<td></td>
<td>Low VDD (1.2 V)</td>
<td>Large (I_o)</td>
<td>HIGH FAIR (I_o)</td>
<td>FAIR (max. volt. diff. between D/S/(G = 2) VDD for all the transistors)</td>
<td>GOOD</td>
</tr>
<tr>
<td>CCCP1</td>
<td>High VDD (1.5 V)</td>
<td>Small (I_o)</td>
<td>HIGH SMALL (2 phase clock driver)</td>
<td>Triple well process</td>
<td>GOOD</td>
</tr>
<tr>
<td></td>
<td>Low VDD (1.2 V)</td>
<td>Large (I_o)</td>
<td>LOW (I_o)</td>
<td>GOOD (max. volt. diff. between D/S/(G = VDD) for all the transistors)</td>
<td>GOOD at low VDD and large (I_o)</td>
</tr>
<tr>
<td>CCCP2</td>
<td>High VDD (1.5 V)</td>
<td>Small (I_o)</td>
<td>LARGE (2 phase clock driver)</td>
<td>N-well process (the B–D/S junctions of the NMOS need to withstand high voltage)</td>
<td>POOR</td>
</tr>
<tr>
<td></td>
<td>Low VDD (1.2 V)</td>
<td>Large (I_o)</td>
<td>LOW (I_o)</td>
<td>GOOD (max. volt. diff. between D/S/(G = VDD) for all the transistors)</td>
<td>FAIR at high VDD and small (I_o)</td>
</tr>
</tbody>
</table>

CCCP2 where the N-type CTSs suffer from the body effect, all other configurations can be cascaded to a higher number of stage with negligible output voltage saturation. The simulation results show that the output voltages of all the charge pumps, except CCCP2, rise linearly with the number of stage. For CCCP2 case, the output voltage becomes saturated when the loading current is large or the supply voltage is low. It is because the threshold voltages of the N-type CTSs in this charge pump increase with the stage number and increases the \(R_{	ext{out}}\) significantly. Thus, the output resistance of the charge pump increases with \(n\) and the output voltage may no longer increase even more stages are cascaded. It is also noted that the cascading capability of DBCP1/2 is comparatively low. The output voltage increases slower with the number of stage under all working conditions. It is because the voltage gain of each stage is smaller. Among all the charge pump circuits, the cascading capability of GBCP is high under all the working conditions. The cascading capability of CCCP1 is also high provides that the supply voltage is high enough and the loading current is small.

To sum up, Table 4 summaries the various characteristics including the voltage gain and power efficiency under different working conditions, area occupation, process requirement, gate-oxide reliability and cascading capability of DBCP1/2, GBCP and CCCP1/2. It gives a clear picture in assisting the circuit designer to choose the most suitable charge pump structure for flash memory applications under the system, performance, and process constraints. For example, considering the NOR flash memory module shown in Fig. 2, the cross-coupled structure charge pump (CCCP1/2) circuit would be a good option for implementing the \((\pm) 6–9\) V charge pump for the program and erase operations and the \(5–8\) V charge pump for the erase operation under a loading current of a few \(\mu\)A. This option has the highest pumping and power efficiencies and area-efficient among the others under the low loading current condition. Moreover, it is also more robust because of low potential drop. However, this structure is not viable if a triple-well process is not available. In addition, if the system supply voltage is low, it is also unfavorable because of its low pumping and power efficiency as discussed before. To implement a high-power \(3–5\) V charge pump, DBCP1/2 and GBCP structures can be a good option as they possess high current driving capability, especially at low supply voltage although they may require a larger silicon area. On the other hand, if a very high output voltage is required, the cascading capability of the charge pump structures
would be the major consideration. For example, to provide the W/E voltage as high as 17 V in the NAND type flash memory cells, DBCP1/2 cannot be a good candidate as the cascading capability is lower than the others and would require more cells to be cascaded which is not area-efficient.

4. Negative charge pump and other charge pump structures

Most of the published papers concerned about positive charge pump circuits and only a few of them were about negative charge pumps. Among the proposed negative charge pump circuits, most of them are based on the gate boosting structure \[31,40–43\]. A cross-coupled structure negative charge pump circuit is also proposed \[58\], but the P-type CTSs in the charge pump suffer from the body-effect. These negative charge pumps in fact are similar to the positive ones. Special attention should be paid on how to avoid the P–N junctions in the circuit being forward biased which would lead to unwanted substrate leakage current. Considering the body-effect, these negative charge pumps in fact are similar to the positive ones. Special attention should be paid on how to avoid the P–N junctions in the circuit being forward biased which would lead to unwanted substrate leakage current. Considering the body-effect. These negative charge pumps in fact are similar to the positive ones. Special attention should be paid on how to avoid the P–N junctions in the circuit being forward biased which would lead to unwanted substrate leakage current.

Some recently proposed charge pump circuits tend to use more than one techniques as given in Section 2. For example, some all PMOS cross-coupled charge pump structures, which use both gate-boosting and cross-coupled techniques, are proposed \[59–62\]. These circuits can be implemented in a standard N-well process without suffering from the body effect. Some authors proposed to use both the gate-boosting and cross-coupled techniques \[63,64\], or even with dynamic biasing technique \[65\]. These circuits result in a better current driving capability. Moreover, a mixed structure charge pump, which uses dynamic biasing technique with a cross-coupled unit cell at the last stage, has also been proposed \[66\]. This scheme effectively removes the threshold voltage drop in a conventional charge pump.

As both positive and negative voltages are required in some flash memories, some polarity switchable charge pump circuits, in which the polarity of the output voltage is switchable, are also developed recently \[67,68\]. Instead of using two separate charge pump circuits, only one charge pump circuit is constructed to provide both positive and negative operation voltages for the flash memory cells. It is an area-efficient solution for the flash memory systems.

5. Conclusion

Various charge pumping structures are reviewed. The important characteristics such as the voltage gain, the power efficiency, the area occupation, the process requirement, the gate-oxide reliability and the cascading capability of these charge pumps are compared in detail. In addition, the three commonly used efficient boosting schemes, namely the dynamic biasing, the gate boosting and the cross-coupled structures are critically discussed with the aid of computer simulations. The results provide a useful reference for the design of charge pump structures under the given technological and operational constraints.

Acknowledgment

The work described in this paper was partially supported the Strategic Research Grant of City University of Hong Kong (Project No. 7008103).

References