A 4-Bit 8GS/s Flash ADC in 0.18μm CMOS Technology

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Abstract
A 4-bit 8GS/s flash Analog-to-Digital Converter is designed and simulated in a 0.18μm CMOS technology. To enhance the speed, both of analog (comparators) and digital (encoder) parts of the ADC are designed fully pipelined using CML gates and latches. Using inductors in comparators extends the sampling rate without an increase in power consumption. Simulation results shows that the power consumption is 300mW, static DNL and INL errors are 0.1 LSB and 0.16 LSB respectively, and the ENOB is 3.2 Bits in Nyquist frequency.

Keywords
Analog-to-Digital Converter, Flash ADC, Current-Mode Logic, pipelined
1. Introduction

The continued speed improvement of serial links and appearance of new communication technologies such as Ultra-Wideband (UWB) have introduced increasing demands on the speed and power specifications of high-speed low/medium resolution analog-to-digital converters (ADCs). While multi-channel ADCs can achieve high speeds, they often require extensive and costly post-fabrication calibration. On the other hand, Flash ADC Architecture is a good candidate to meet the requirements of speed and resolution. They are the key building blocks in many applications like optical data storage systems, high-speed data rate digital communications, high-speed devices, optical communications, wideband radars and etc. These applications require 4 to 6 bits of resolution at conversion rates of several gigahertzes. In the proposed structure, a speed of 8GS/S is achieved based on low-swing operation in the complete ADC by using of a preamplifier and three latch stages. Inductors in comparator and first latch stage enhance the time constant and in consequence the overall speed is increased. [1-4].

This paper is organized as follows. Section 2 reviews the overall flash ADC architecture. The comparator circuits include preamplifier and latch stages is discussed in section 3. Finally, Simulation results are presented in section 4.

2. ADC Architecture

The architecture of the proposed flash ADC is shown in Figure 1. The input signal of the ADC is compared with evenly-spaced reference voltages generated by resistor ladder. Comparators are includes several amplification and latching stages, and amplify the differences between the input signal and reference voltage. The comparison results as an array of digital bits, they are thermometer code and they convert to gray code then binary code by current-mode-logic (CML) encoder [3].

![Figure 1. 4-Bit flash ADC Architecture [3]](image-url)
3. Circuit Implementation

3.1. Comparator core with inductor

As shown in Figure 2, the comparator is comprised of 4 stages. The first stage is a low gain and high speed preamplifier with inductors. The second stage operates in two modes: tracking and latch. When the clock is high, outputs follow the inputs and when the clock is Low the amplified difference is latched by a regenerative cross-coupled latch. In order to have higher swing, this stage has not a current sink in its tail. As a result, the dynamic power consumption of this stage is directly depended on the size of the clock transistors and must be considered in design. Actually, high speed is achieved by preamplifier and latch. Two additional latches also pipelines with these stages to enhance the latch operation [3].

![Figure 2](image1.png)

Figure 2. (a) Preamplifier , (b) The 1st Latch (also acts as a T/H), and (c) 2nd , 3rd Latches

Decreasing the tracking time constant ($\tau_t$) and regeneration time constant ($\tau_r$) is the effective solution for increasing the speed of comparator [5]. Using inductor in preamplifier and T/H we achieved good operation at 8 Gs/s sampling rate. Inductors reduce the effective time constant and signal transition time in the desired node, and let the comparator to be used at higher frequencies. Figure 3 shows the RLC circuits at the output node, and its equivalent RC circuit.

![Figure 3](image2.png)

Figure 3. (a) RLC circuit at output node (b) RC equivalent circuit

It can be proved that two circuits are equivalent if [5]:

$$R_{\text{eff}} = R + \frac{\omega^2 L^2}{R}, \quad C_{\text{eff}} = C - \frac{L}{R^2 + \omega^2 L^2}$$

(1)
Therefore, the regeneration time constant is reduced:

$$\tau_r = \frac{C_{\text{eff}}}{g_m - \left(\frac{1}{L/R_{\text{eff}}}\right)}$$  \hspace{1cm} (2)

It seems that increasing the inductance is possible to achieve a higher speed, but it may cause second order effects in system and lead to oscillation. Total capacitance of the node is equal to $C_{d1} + C_{d4} + C_{g3}$. Simulation of Comparator with the device sizes shown in figure 2 shows that the total capacitance is about 80fF. So, according to equation (2), regeneration time constant is approximately equal to 30 ps. If we suppose that the output reaches to its final value at the four time constants, with 8GHz sampling rate (the period of the clock frequency is 125ps) it can be concluded the core of comparator will operate successfully in this frequency. In the absence of 5nH inductors, regeneration time constant is about 70ps and output not settles even if the sampling frequency is 4Gs/s. Therefore, by using inductors an increase in the sampling frequency up to 8 GHz can be achieved. It should be noted that the calculation of the inductors are fully expressed in reference [5].

Since the inductors occupy large area on chip, it is possible to reduce this active area using some techniques. For example, differential inductor can be used [5]. In this work, the active area occupied by a differential inductor is calculated about 40μm×40μm.

### 3.2. Encoder

In flash ADC, outputs of comparators array compose a thermometer code. Therefore, an encoder should be designed in order to convert this thermometer code to corresponding binary code. Figure 4 shows the logic circuits encoder: first converts the thermometer code to an intermediate gray code and then produce binary code. Generally, the encoder is a combinational logic circuit, but latches are placed between stages to increase the speed. This results a sequential circuit, using 4-stage pipeline architecture.

We use Current-Mode Logic (CML) for implementation of logic gates (NAND, AND, XOR). CML blocks ensure the high-speed and low-power operation on signals with low-swing. Conversion to gray code reduces the effect of bubble errors in the thermometer code [6,7]. In order to synchronization, delay elements are used. The fully-differential CML logic gates and latch are shown in Figure 5.

![Figure 4. Encoder logic architecture](image-url)
Figure 5. CML Blocks: (a) AND/NAND gate, (b) XOR gate, and (c) CML Latch

4. Simulation Results

In this section, we present the HSPICE and Cadence simulation results to verify the operation of designed ADC. The sizes of MOS devices are shown in figures.

The static specifications of overall ADC are shown in Figure 6. a slow ramp is applied as input, which results a Differential Non-Linearity (DNL) of 0.1 LSB and a Integral Non-Linearity (INL) of 0.16 LSB.

Figure 6. Static Specifications (DNL and INL)

Figure 7 shows the variations in the Effective Number Of Bits (ENOB) for several sinusoidal inputs with different frequencies. The output signals of the ADC for 15.625 MHz and 3.984 GHz (Near Nyquist) and their corresponding 512-point DFT are shown in Figure 8. The ENOB achieved by simulation are 3.94 and 3.28 Bits for 15.625 MHz and 3.984 GHz input signals, respectively.
Since the CML circuits are used in all blocks, the average power consumption is independent to clock frequency. In this design, the total power consumption of 300mW is obtained for 1.8V power supply. Comparators, resistor ladder and encoder consume 160, 110 and 30 mW, respectively.

Table 1 compares the presented ADC with two single channel high-speed Flash ADC published in recent years.
Table 1. Comparison of the performance

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<td>Technology</td>
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<td>Resolution</td>
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<td>Sampling Rate (GS/s)</td>
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<td>3.3 @ Nyquist</td>
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<td>INL (LSB)</td>
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<td>0.16</td>
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5. Conclusion

In this paper, a 4-bit 8 GS/s Flash ADC in 0.18um CMOS technology is presented. Low-swing operation, pipelining latches and using inductors allows achieving the speed of 8GS/s with a single non-time-interleaved ADC. Thus, with no digital calibration technique the proposed 4-bit ADC achieves an ENOB of 3.3 Bits at Nyquist frequency (about 4 GHz). Simulation results also show that the power consumption is 300 mW, static INL and DNL errors are 0.1 LSB and 0.16 LSB respectively. For future designs, by Time-Interleaving and adding digital calibration techniques, an ultra-high-speed ADC can be designed.

References


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