Stability Analysis of Two-Stage PFC Power Supplies

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***Abstract*— Power-factor-correction (PFC) power supplies are required to provide high input power factor and tight output voltage regulation. The usual configuration takes a two-stage cascade structure, consisting of a PFC preregulator and a dc/dc converter. Previous studies of the dynamical behaviour mainly focused on the boost PFC preregulator, assuming that it is being terminated by a resistive load. However, in practice, as the PFC preregulator is terminated by a dc/dc converter whose characteristics differ from resistive load's, the assumption of resistive load termination gives rather inaccurate information about the stability of the system. In this paper we study the complete two-stage PFC power supply and show that the interaction between the PFC stage and the dc/dc converter stage plays an important role in determining the stability of the system.**

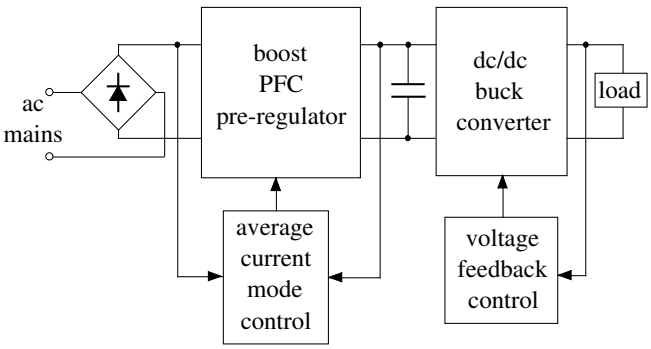

Fig. 1. Two-stage PFC power supply

I. Introduction

A power supply with input power factor correction (PFC) typically consists of a preregulator for PFC, cascaded with a dc/dc converter stage for output regulation [1], [2], [3]. The two stages can be separately controlled to achieve PFC and tight output regulation. Moreover, for ease of controller integration, the control of the two stages can be merged in a combo integrated circuitry, e.g., Fairchild ML8424 [4]. Such combo control, characterized by a shared frequency and possible synchronization of the switching period, causes stability problem which is not predicted with the usual analysis that assumes the cascading dc-dc converter being a resistive load [5], [6].

Previous studies have mainly focused on the dynamical behaviour and stability boundaries of the boost PFC pre-regulator operating in continuous conduction mode (CCM) and revealed both slow-scale [5], [6] and fast-scale [7], [8] instabilities. In this paper, we show however that extending the results concerning the stability of the boost PFC preregulator with a resistive load to the practical two-stage circuit can be misleading, particularly with the combo control. Specifically, we will show by computer simulations that it is possible for the complete two-stage PFC power supply, with both the boost PFC preregulator and the buck output regulator designated to operate in CCM, to suffer from slow-scale instability even when the control parameters assure the individual stability of each of the two constituent stages. The results point to the necessity of investigating thoroughly the detailed dynamical behaviour and the stability boundaries of the two-stage PFC power supply and the importance of treating it as a whole in doing so.

II. Two-Stage PFC Power Supplies

A block diagram of the two-stage PFC power supply is depicted in Fig. 1. The objective of active PFC is to make the input to the power supply look like a simple resistor and the PFC preregulator does this by programming the input current in response to the input voltage. In practice, a boost converter has been a favorable and popular choice for the PFC preregulator. Although the discontinuous conduction mode (DCM) has the obvious advantage of simplicity since no additional control is required, it is limited to relatively lower power ranges. The CCM considered in the present study is more suited for applications in higher power ranges. For CCM, moreover, feedback is necessary to program the input current to follow the input voltage waveform. Typically a peak current mode control or average current mode control may be used. Peak current mode control gives rise to problems such as poor noise immunity, need for slope compensation, poor factor correction due to significant errors between the programming signal and the input current. Average current mode (ACM) control eliminates these problems, is commonly available on monolithic control ICs and is therefore the control method considered here.

The boost PFC preregulator typically gives a high output voltage which is greater than the highest expected peak input voltage and provides very crude regulation. Consequently, a buck converter (in the form of a transformer-isolated forward converter) is needed to step this voltage down to a useable level and to provide tight output regulation. The buck converter may operate in either modes, and is controlled via a voltage feedback loop. The CCM case is considered in this study, since this operation mode, at the expense of a larger inductor,

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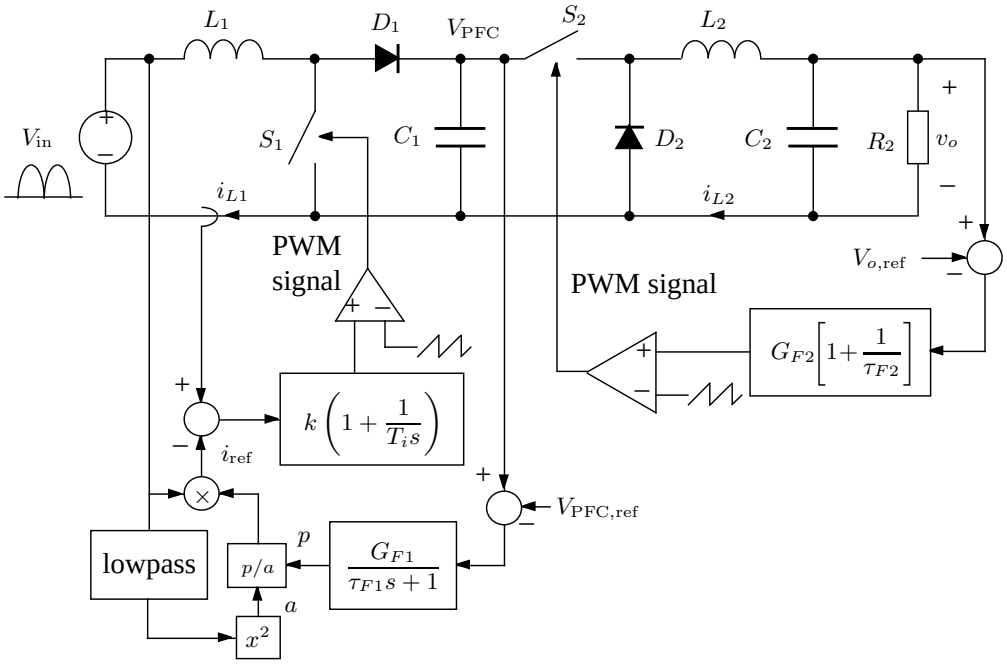


Fig. 2. Schematic of a two-stage PFC power supply, with CCM boost preregulator under ACM control and a CCM buck converter under voltage feedback control.

TABLE I

CIRCUIT PARAMETERS USED IN SIMULATIONS.

Parameters	Values
Rectified line voltage $v_{\rm in}$	70 Vrms, 50 Hz
Boost stage inductance L_1	1 mH
Boost stage capacitance C_1	60 μF
Boost switching period T_{s1}	10 μs
Reference PFC output voltage $V_{\rm PFC,ref}$	240 V
PI current controller gain k	5.12
PI current controller time constant T_i	0.12 ms
Boost stage gain G_{F1} (nominal)	8.0
Boost stage feedback time constant τ_{F1} (nominal)	8.6 ms
Buck stage inductance L_2	1 mH
Buck stage capacitance C_2	60 μF
Buck switching period T_{s2}	5 μs
Reference output voltage $V_{o,\rm ref}$	24 V

is usually more efficient and the current stress on the active switch is lower.

The circuit schematic of the two-stage PFC power supply under study is shown in Fig. 2. Here, we omit the isolation transformer for simplicity. The power circuit of the boost PFC stage is the same as that of a boost converter. Its control circuitry must control both the input current i_{L1} and the PFC output voltage $v_{\rm PFC}$. Accordingly, the average current mode (ACM) control used is a two-loop system [9]. The current loop, employing a PI controller and generating the switching signal through a pulse-width modulation (PWM) scheme, is programmed by the rectified line voltage $v_{\rm in}$ so that the input to the converter will appear to be resistive. The PFC output voltage is controlled by changing the average amplitude of the current programming signal $i_{\rm ref}$. In this voltage loop the

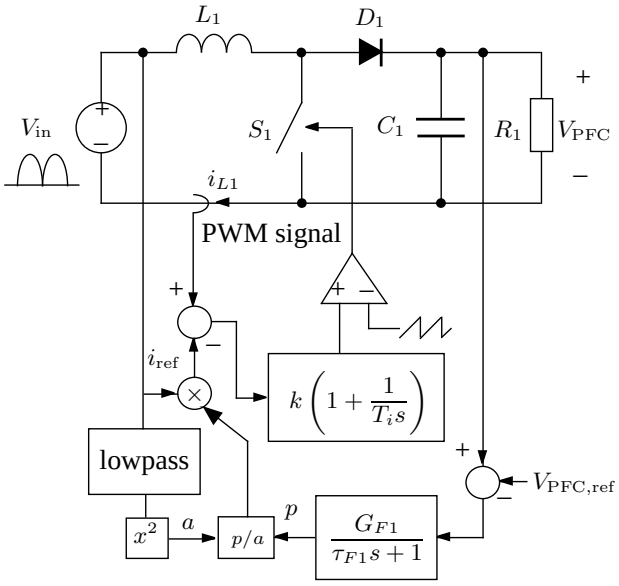


Fig. 3. Circuit schematic used in previous studies assuming the PFC stage being terminated by an equivalent resistive load.

output p of the voltage error amplifier is divided by the square of the RMS value of the input voltage before it is multiplied by the rectified line voltage. The output of the multiplier is the current programming signal, which hereby has the shape of the input voltage and an average amplitude which controls the PFC output voltage. The squarer and divider circuits keep the gain of the voltage loop constant; without it the gain of the voltage loop would change as the square of the RMS value of the input voltage. The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control, since it actually controls the power delivered to the output

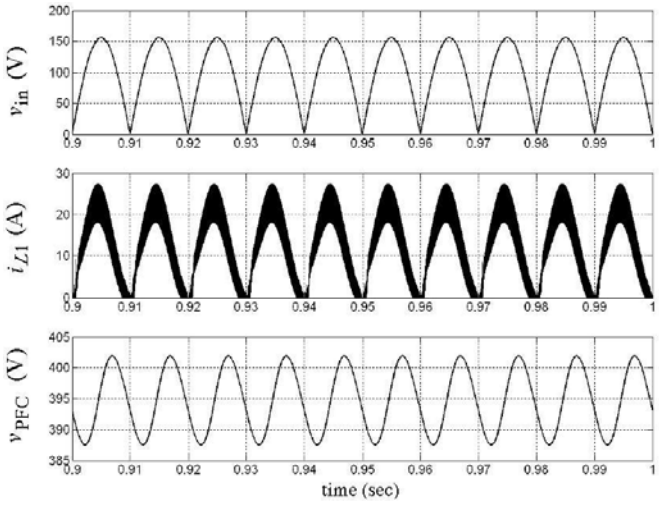


Fig. 4. Simulated waveforms from boost PFC stage with resistive termination in stable operation. Upper: input voltage; middle: inductor current; lower: capacitor voltage.

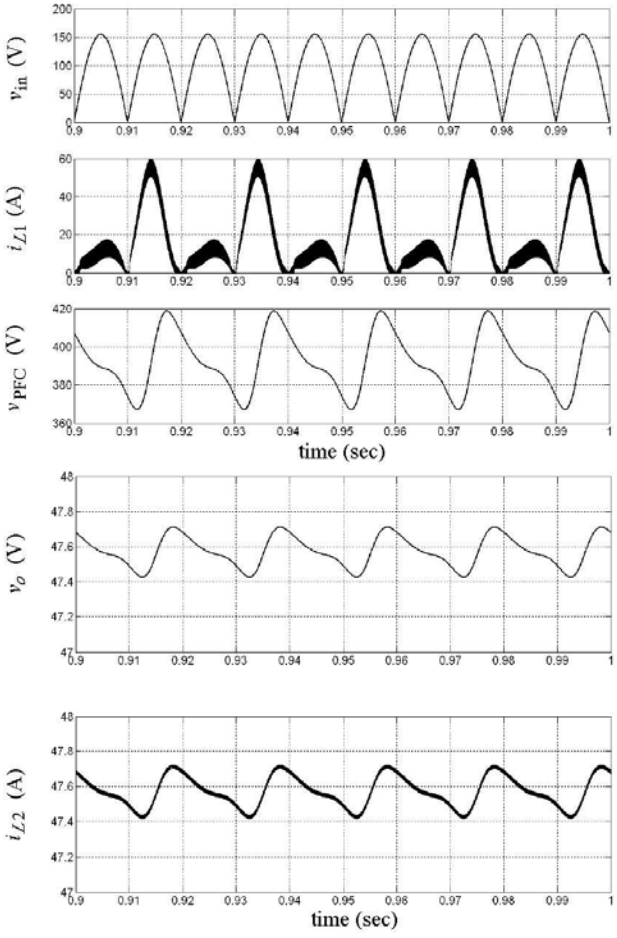


Fig. 5. Simulated waveforms from the two-stage PFC power supply showing "unstable" slow-scale period-doubling phenomenon. From top to bottom: Input voltage, boost stage inductor current, storage capacitor voltage, output voltage, buck stage inductor current.

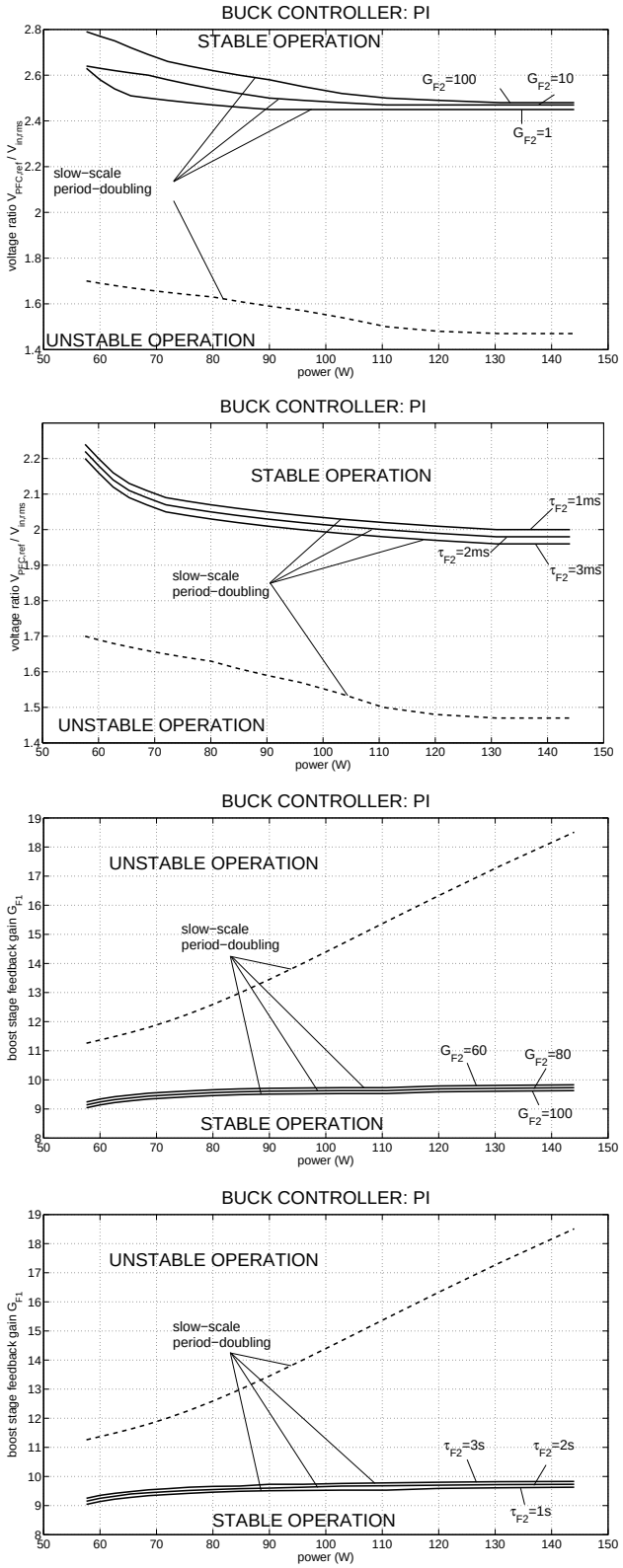


Fig. 6. Stability boundaries for boost PFC converter assuming resistive termination (dashed line) and terminated by buck converter under PI control (solid line). Each figure corresponds to different parameter variations.

of the boost PFC converter. In practice, a low-pass type of feedback is applied, with parameters G_{F1} and $1/\tau_{F1}$ in Fig. 2 denoting the dc gain and cut-off frequency of the feedback circuit, respectively.

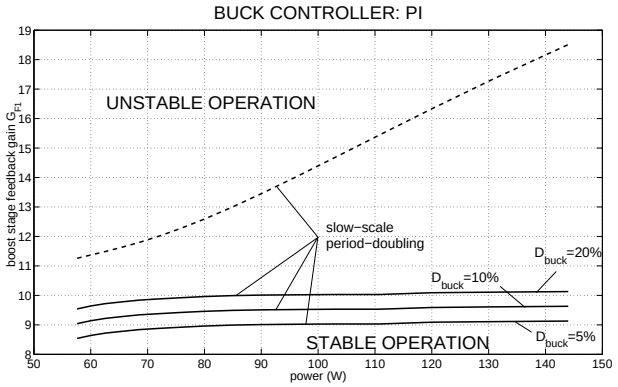


Fig. 7. Stability boundaries for boost PFC converter assuming resistive termination (dashed line) and terminated by buck converter under PI control (solid line) for different steady-state duty cycles.

The same parameters are indicated for the feedback circuit of the buck converter, whose output voltage v_o is regulated at its desired value $V_{o,\mathrm{ref}}$ by voltage-mode PWM control. Table I lists the operating parameters used in the present study. Both the boost PFC preregulator and the buck regulator are designed to operate in CCM.

III. Stability Analysis by Simulations

The detailed investigation of the dynamical behaviour of the practical two-stage PFC power supply can be challenging due to the complex interaction between the two stages. A way of reducing complexity is to replace the tightly regulated dc/dc buck converter by a resistive load with same power dissipation. Most previous studies analysed the phenomena in the boost PFC converter feeding a purely resistive load and operating in CCM, as depicted in Fig. 3. Consequently, some results are available for this circuit [5], [6]. The main objective of the present study is to investigate to what extent can these results be considered still valid when applied to the actual two-stage circuit.

Fig. 4 shows the simulated waveforms for a stable operation with $G_{F1} = 225$ and $\tau_1 = 8.5$ ms for the boost PFC converter (Fig. 3) with the resistive load $R_1 = 100\ \Omega$ at the same power level. The CCM input current (middle waveform) is programmed by the input voltage (upper waveform) to be a half sine wave, achieving a near unity power factor. The PFC output voltage (lower waveform) is a sine wave at twice the AC line voltage, as expected.

In order to verify whether the two-stage circuit exhibits the same stable operation, the buck converter is reinstated in the second stage, achieving a tight output regulation for gain $G_{F2} = 10$ and bandwith 1.6 kHz ($\tau_{F2} = 0.1$ ms). However, the simulation results in Fig. 5 show a slow-scale period-doubling phenomenon in the dynamics of the boost PFC preregulator (upper three waveforms), the period of the waveforms becomes equal to the mains period, which can also be detected in the waveforms of the buck output regulator (lower two waveforms).

The stability operation of the actual circuit is more restricted than that deduced previously in [5], [6] for the PFC stage terminated with resistive load. This is more readily seen from Fig. 6, which compares the stability boundaries of the boost PFC assuming resistive termination and the two-stage circuit in the parameter space defined by various parameters and the output power, for a few sets of feedback parameters of the buck converter. Also, Fig. 7 shows the stability boundaries for different steady-state duty cycles in the parameter space of G_{F1} versus output power.

IV. Experimental Verifications

An experimental circuit has been constructed for verification purposes. The PFC stage is a boost converter under average current-mode control, which is then cascaded with a forward converter. The PFC control of the boost stage is accomplished by UC3854A and the forward converter is controlled by a standard UC3825N PWM controller with a simple PI compensator. The circuit is thus exactly as the one analyzed in the previous section. The experimental PFC power supply is shown in Fig. 8.

For comparison, we show here the measured stability boundary curves corresponding to variation of the PFC stage feedback gain and the $V_{\mathrm{PFC}}/V_{\mathrm{in}}$ conversion ratio. The input voltage is 70 V rms, the output of the PFC stage is set at 240 V DC, and the output voltage is 9 V. Figure 9 (a) compares the boundary curves of the resistor terminated PFC stage and the complete two-stage power supply in the parameter space of G_{F1} versus output power, and Fig. 9 (b) compares the boundary curves of the complete two-stage power supply for different values of the duty cycles. Figure 10 compares the the boundary curves of the resistor terminated PFC stage and the complete two-stage power supply in the parameter space of $V_{\mathrm{PFC}}/V_{\mathrm{in}}$ versus output power. Here, the value of V_{in} actually changes in order to vary $V_{\mathrm{PFC}}/V_{\mathrm{in}}$. All results verify the basic phenomenon that the PFC stage loaded by a forward stage is less stable.

V. Conclusions

In analysing PFC power supplies, previous studies have assumed a resistive load termination for the PFC boost stage. However, in practice, the PFC boost preregulator is almost always cascaded with a voltage regulator. In this paper, a comparative study has been performed for the two circuit models, allowing the identification of the effects of the interaction between the two stages on the stability findings. It has been shown that the assumption of resistive load termination for the PFC stage produces inaccurate stability information. The actual two-stage PFC power supply is more prone to instability. Intuitively such a result is expected since the dc/dc converter stage represents a constant power load when its output is perfectly regulated. This is equivalent to a negative resistance presented to the PFC stage in the small-signal sense, which jeopardizes the overall system stability.

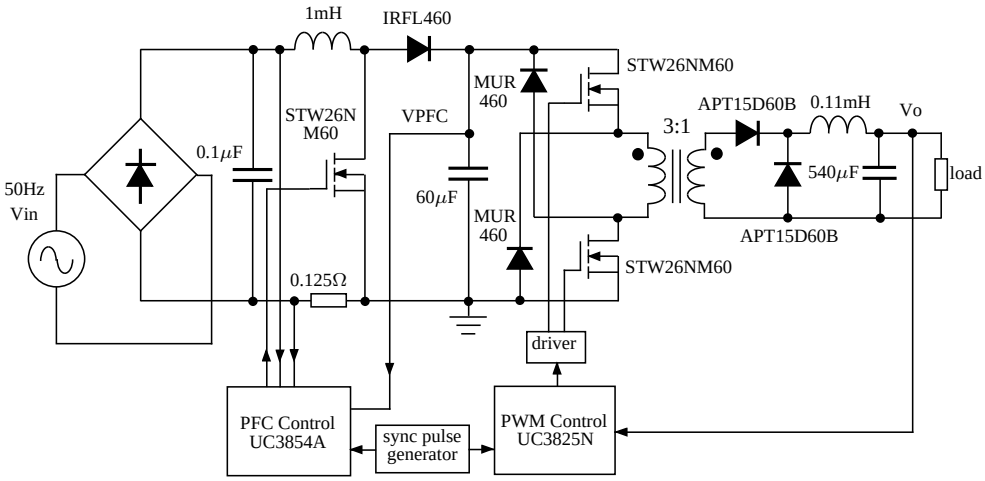
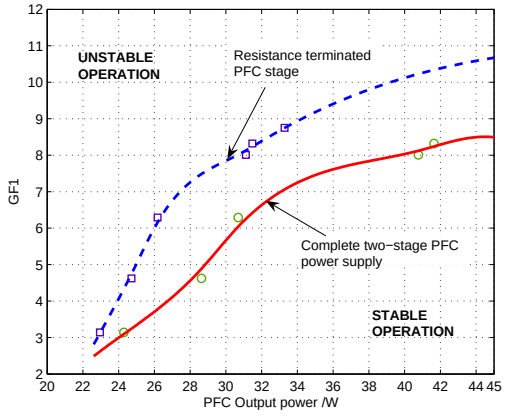
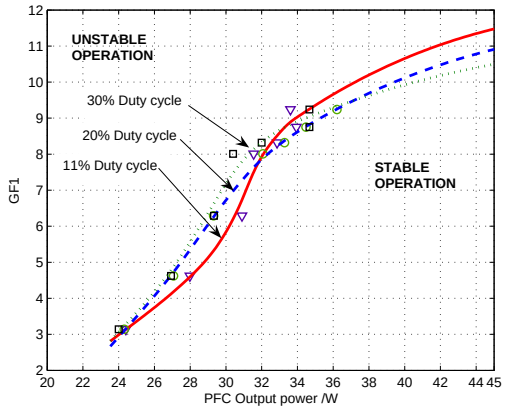


Fig. 8. Experimental circuit of the resistor terminated PFC boost stage. For the complete power supply, resistor R is removed and the PFC stage is connected to a standard forward converter.



(a)



(b)

Fig. 9. Measured stability boundaries in the space of G_{F1} vs power. (a) Comparison of resistor terminated PFC stage and 2-stage power supply; (b) comparison of 2-stage power supply for various duty cycles.

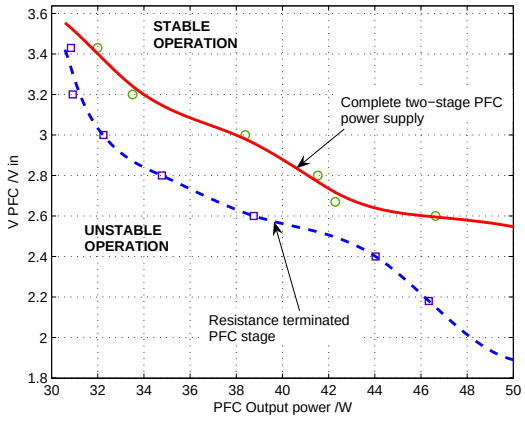


Fig. 10. Measured stability boundaries in the space of $V_{\rm PFC}/V_{\rm in}$ vs power.

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