Defect Level Evaluation in an IC Design Environment

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Abstract

The purpose of this paper is to present a methodology for the evaluation of the Defect Level in an IC design environment. The methodology is based on the extension of Williams-Brown formula to non equiprobable faults, which are collected from the IC layout, using the information on a typical IC process line defect statistics. The concept of weighted fault coverage is introduced, and the Defect Level (DL) evaluated for the Poisson and the negative binomial yield models. It is shown that DL depends on the critical areas associated with undetected faults, and their correspondent defect densities. Simulation results are presented, which highlight that the classic single Line Stuck-At (LSA) fault coverage is a unreliable metric of test quality. Moreover, results show that the efficiency of a given set of test patterns strongly depends on the physical design and defect statistics.

0.1 Introduction

In order to achieve the high standards of electronic products quality, it is mandatory to evaluate test quality. The zero defects strategy leads, in practice, to the definition of *Defect Levels (DL)* (or escape rates) as low as 100 ppm (parts per million) or less. We refer to Defect Level [1, 2] as the percentage of defective chips that successfully pass the production test and, thus, are marketed as good. Hence, at the production stage, DL should be viewed as the *indicator of test quality*.

Test preparation is carried out in the design phase of the product development. However, test quality, in the digital IC design environment, is usually assessed by the *fault coverage*. In industry, the fault coverage is estimated as the percentage of *single Line Stuck-at (LSA)* faults which are detectable by a set of test patterns, and is evaluated by gate-level fault simulation (this could also be expanded to model other types of faults, such as delay faults). The Defect Level, DL, may be estimated using Williams-Brown equation [1], relating DL with the yield, Y, and the fault coverage, T, as

$$DL = 1 - Y^{(1-T)} \tag{1}$$

This equation was derived under the assumption of equiprobable faults, and it can be used by the chip manufacturer to estimate DL after a production test of defined coverage. However, the IC designer has not sufficient data to predict DL, and thus to evaluate the test quality.

Moreover, it has been proved, especially for CMOS designs, that single LSA fault coverage is not synonimous with *defect coverage* [3,4]. In fact, physical defects, induced or enhanced during IC manufacturing, are the real cause of circuit faults; those which modify the DC connectivity of adjacent conducting or semiconducting regions [17] (or the device characteristics) are referred as *critical defects*. Under this perspective, test quality should evaluate the ability of the test patterns to cover critical defects.

Unfortunately, the common practice is that the fault list is compiled on the basis of a purely *topological* description of the circuit (usually, gate level), without any reference to its layout, or its *physical structure*. Hence, some faults which actually affect the circuit are disregarded, whereas other faults which cannot physically occur are included in the fault list. In view of such abstract fault model, equiprobable faults are assumed, which strongly deviates from the reality. As a consequence, single LSA fault coverage, T, can be a misleading metric for test quality [5-7], and both Y and T may loose validity and meaning, as confirmed also by observation on production chips [8].

The purpose of this paper is to present a methodology for the evaluation of the Defect Level in an IC design environment. The methodology is based on the extension of the Williams-Brown formula to non equiprobable faults [9,10], which are collected from the IC layout, by exploiting the concept of critical area, and using the information on a typical IC process line defect statistics [11]. Section 2 introduces the extension of equation (1), the concept of a *weighting factor*, associated with the probability of occurrence of each fault, and the definition of a *weighted fault coverage*. The evaluation of the faults probabilitites, for different yield models, is presented in section 3, in which a physical significance to the weighted fault coverage is given. Section 4 reviews the software package used to extract the realistic fault list and to

compute Y, DL and the weighted fault coverage, Ω, and presents some illustrative simulation examples. A final discussion is included in section 5.

0.2 Defect Level for Non-Equiprobable Faults

Let us define the event A as the real fault-free case, i.e., the case in which none of the n faults, assumed possible to occur (and thus included in the fault set) is present on the chip. Moreover, let B represent the event which refers to successful testing for m out of the n assumed faults ($m \leq n$)

Assuming equiprobable faults, with p as the probability of a fault occurring, $P(A) = (1-p)^n$ is the probability of a good chip and, by definition, is equal to the yield (referred to the chosen fault model). $P(B) = (1-p)^m$ is the probability of having a chip not affected by m out of n faults. $P(A|B)$ is the probability of having a good chip after a test whose fault coverage is $T = m/n$. This, by definition, coincides with $1 - DL$. By application of Bayes rule [12],

$$P(A|B) = P(B|A)\ P(A)/P(B) \tag{2}$$

and, since $P(B|A) = 1$,

$$P(A|B) = P(A)/P(B) = (1-p)^{n-m} = (1-p)^{(1-m/n)n} = (1-p)^{n(1-T)} = Y^{(1-T)} \tag{3}$$

As a consequence,

$$DL = 1 - Y^{(1-T)} \tag{4}$$

which is the well known formula presently employed for equiprobable faults.

0.2.1 Generalization of Williams-Brown Formula

Assuming now that nonequiprobable independent faults may occur, denoting p_j the probability of occurrence of fault j, and reordering the fault list in such a way that the first m are the m out of n detected faults, we have

$$P(A) = Y = \prod_{j=1}^{n}(1-p_j) \tag{5}$$

$$P(B) = \prod_{i=1}^{m}(1-p_i) \tag{6}$$

$$P(A|B) = \frac{\prod_{i=1}^{n}(1-p_i)}{\prod_{j=1}^{m}(1-p_j)} = \prod_{i=m+1}^{n}(1-p_i) = 1 - DL \tag{7}$$

The last equation clearly shows that the Defect Level only depends on the probability of occurrence of the *undetected faults*. In other words, $(1 - DL)$ is the partial yield associated with the undetected faults. Given the identity $x = e^{ln(x)}$, or, in general, $x = \alpha^{log_\alpha(x)}$ where $x > 0$, equation (7) can also be written as

$$P(A|B) = \frac{Y}{\prod_{j=1}^{m}(1-p_j)} = Y^{1-log_Y(\prod_{j=1}^{m}(1-p_j))} \tag{8}$$

By using the change of basis from Y to e, equation (8) can now be written as

$$P(A|B) = Y^{(1-\frac{log_e(\prod_{j=1}^{m}(1-p_j))}{log_e Y})} \tag{9}$$

or

$$P(A|B) = Y^{(1-\frac{ln(\prod_{j=1}^{m}(1-p_j))}{lnY})} \tag{10}$$

and finally

$$P(A|B) = Y^{(1-\frac{ln(\prod_{j=1}^{m}(1-p_j))}{ln(\prod_{i=1}^{n}(1-p_i))})} = 1 - DL \tag{11}$$

As a consequence, we may define a new parameter, the *weighted fault coverage*, Ω, as

$$\Omega = \frac{ln\prod_{j=1}^{m}(1-p_j)}{ln\prod_{i=1}^{n}(1-p_i)} \tag{12}$$

and conclude that

$$DL = 1 - Y^{(1-\Omega)} \tag{13}$$

i.e., we can retain equation (1) for nonequiprobable faults, if the concept of *weighted fault coverage* is introduced, rather than the one associated with the equal probability assumption. This parameter is still a fault coverage, in the sense that it compares detected faults with the entire fault set; however, it takes into account the probabilities of non occurrence $(1 - p_j)$ of detected faults, as compared to the probabilities of non occurrence of all likely faults. Of course, for equiprobable faults, Ω reduces to T.

At this stage, and for reasons that will become apparent in the following, a *weighting factor of a fault*, w_j, is introduced as [9]

$$w_j = -ln(1 - p_j) \tag{14}$$

The above equations can thus be written as

$$Y = exp(-\sum_{j=1}^{n} w_j) \tag{15}$$

$$\Omega = \frac{\sum_{j=1}^{m} w_j}{\sum_{i=1}^{n} w_i} \tag{16}$$

$$DL = 1 - exp(- \sum_{i=m+1}^{n} w_i) \quad (17)$$

These equations are general, since Y, Ω and DL are dependent on the fault probabilities of occurrence, which can be computed for different yield models. As it will be seen in section 3.1, for the Poisson yield model, a physical significance can be attributed to w_j and Ω.

0.2.2 Weighted Fault Incidence and Coverage

As shown above, the computation of DL deals with the evaluation of the relevance of the probabilities of occurrence (or of the weighting factors) of the undetected faults, as compared to the entire fault set. Such relevance can be highlighted by tedious (and computer expensive) fault simulation; however, it would be rewarding to devise a strategy to identify hard to detect fault subsets, without fault simulation. Moreover, from the manufacturer's point of view, and for a given design style (e.g., a standard cell style) and a set of design rules, it is important to identify the sensitivity of the layout to the different physical failure mechanisms, in order to improve either the cells layout and routing, or the process design rules.

Therefore, the partitioning of the fault set, extracted from the layout, for a given defects statistics, may be useful from two points of view:

1. *according to the expected fault detectability* - the identification of the faults nature (such as shorts, or opens) and topology, allows the identification of subsets of faults which systematically exhibit high or low fault coverage [13]. For instance, nonfeedback bridging faults *within* reconvergent fanout areas are more difficult to detect than those occurring outside such areas, and open faults causing floating gates disconnecting *one* MOS transistor gate terminal are harder to detect than those, in a full CMOS design, which disconnect both complementary transistors. Such partitioning of the fault set, according to the expected faults detectability, can guide the designer in evaluating DL, and in identifying poor testability areas [14];
2. *according to different physical failure mechanisms* - the evaluation of the sensitivity of the layout to different failure mechanisms, e.g., metal_1 shorts, or poly opens, may lead to cell library [15] or design rules refinements.

Assuming that the fault set (n faults) is partitioned into k subsets, each one with n_k faults, it is possible to define, for each subset (or *fault class*), a *class fault incidence*, FI_k, as

$$FI_k = \frac{\sum_{j=1}^{n_k} w_j}{\sum_{i=1}^{n} w_i} \quad (18)$$

and a correspondent *class fault coverage*, Ω_k, as

$$\Omega_k = \frac{\sum_{j=1}^{m_k} w_j}{\sum_{i=1}^{n_k} w_i} \tag{19}$$

where m_k are the detected faults of class k. After some manipulation, the weighted, global fault coverage, Ω, can be written as

$$\Omega = \sum_{k=1}^{c} FI_k \; \Omega_k \tag{20}$$

where c is the total number of fault classes.

Therefore, the weighted fault coverage can be viewed as the sum of the class fault incidences, weighted by the class fault coverages. As a consequence, classes with low fault incidences have little impact on Ω, regardless of their weighted fault coverage; on the contrary, classes with high fault incidences have a dominant role in Ω. As an example, it has been shown, for a particular case of a digital, 2_metal CMOS process, and a standard cell design style, that typically 45% of extracted faults are bridging (BRI) faults [7]; however, their *incidence* is as high as 95%, due to the greater density of defects associated with bridging mechanisms, in a positive photoresist process. Note that *class fault incidences* can be computed from the circuit netlist and the fault set, without simulation. This implies that the sensitivities can be calculated with low cost computation.

0.3 Evaluating Individual Fault Probabilities

In order to compute Y, Ω and DL, we need to evaluate the probabilities of occurrence of the faults, p_j, in the fault set. We assume that a circuit fault is a consequence of a *critical* defect present on the chip. The physical defects under consideration are spot defects, which can be related in some way to the lithographic masks of the process [16,17].

0.3.1 Uniform Distribution of Defects (Poisson Yield Model)

Assume a spot defect of a given diameter Ψ. In general, the number of spot defects landing on a chip is a random variable R for which a Poisson distribution function is hypotized. Therefore, the probability of having exactly r defects is given by

$$P(R = r) = \frac{exp(-\overline{R})\overline{R}^r}{r!} \tag{21}$$

where $\overline{R} = A\overline{D}$ is the product of the chip area, A, times the average number of defects per unit area, $\overline{D}$ (defect density). Assuming the defects are independent of each other, a Bernoulli trials model can be applied to calculate the probability that k out of r of these defects will result in faults (i.e., defect landing in the critical area):

$$P(K = k|R = r) = \frac{r!}{k!(r-k)!}\theta^k(1-\theta)^{r-k} \tag{22}$$

where K is the random variable "number of faults" and θ is the probability that a randomly selected defect will result in a fault.

The probability of a given electrical fault is the probability of having at least one defect landing in the critical area defined for that fault:

$$P(fault) = P(K = 1|R = 1)P(R = 1) + [P(K = 1|R = 2) + P(K = 2|R = 2)]P(R = 2) + ... \tag{23}$$

or

$$P(fault) = \sum_{r=1}^{\infty}\sum_{k=1}^{r} P(K = k|R = r)P(R = r) \tag{24}$$

$$P(fault) = \sum_{r=1}^{\infty}\sum_{k=1}^{r} \frac{r!}{k!(r-k)!}\theta^k(1-\theta)^{r-k}\frac{exp(-\overline{R})\overline{R}^r}{r!} \tag{25}$$

$$P(fault) = exp(-\overline{R})\sum_{r=1}^{\infty}\frac{\overline{R}^r}{r!}\sum_{k=1}^{r}\frac{r!}{k!(r-k)!}\theta^k(1-\theta)^{r-k} \tag{26}$$

$$P(fault) = exp(-\overline{R})\sum_{r=1}^{\infty}\frac{\overline{R}^r}{r!}[1-(1-\theta)^r] = 1 - exp(-\overline{R}\theta) \tag{27}$$

Now, in the joint probability expression, $P(fault, defect) = P(fault|defect)P(defect)$, we may evaluate the conditional probability from (22) for $k = 1$ and $r = 1$, yielding

$$P(fault|defect) = P(K = 1|R = 1) = \theta = A_c/A \tag{28}$$

where A_c is the critical area [18], given by

$$A_c = \int_0^{\infty} A(\Psi)f_{\Psi}(\Psi)d\Psi \tag{29}$$

and $f_{\Psi}(\Psi)$ is the defect size distribution function. Hence, θ has a simple geometrical interpretation: it is the ratio A_c/A in the hypothesis of uniformly distributed defects. By substituting in equation (27), we finally obtain

$$P(fault) = 1 - exp(A_c\overline{D}) \tag{30}$$

which shows that to evaluate the probability of a given fault, it is required to know the average defect density and the critical area for that fault.

Clearly, a fault may result from the union of a set of disjoint events. For instance, a short between two electrical nodes may result from shorts between different wires, of different layers (such as shorts between two metal_1 lines, and between two poly lines). In this case, the *effective* critical area is the sum of the elementary critical areas, each weighted by its defect density, corresponding to the elementary faults [17]. We refer to *elementary faults* as those associated with a single circuit topology (e.g., short between nodes x_1 and x_2), and a single *Physical Failure Mode (PhFM)*; examples of *PhFMs* are shorts between poly lines, or open Al/diffusion contacts. On the contrary, we may whish to analyse separately each elementary fault, to assume for each *PhFM* a defect density, D_j, and then to define for each of these faults a critical area, A_j. At present, there are tools available for critical areas evaluation [9,19,20]. In the software package described in section 4 [9], such approach is followed.

Under the Poisson yield model, and assuming elementary faults, we can thus write for the weighting factor of fault j

$$w_j = -ln(1 - p_j) = A_j D_j \tag{31}$$

and, hence,

$$Y = exp(-\sum_{j=1}^{n} A_j D_j) \tag{32}$$

$$\Omega = \frac{\sum_{j=1}^{m} A_j D_j}{\sum_{i=1}^{n} A_i D_i} \tag{33}$$

$$DL = 1 - exp(-\sum_{i=m+1}^{n} A_i D_i) \tag{34}$$

$$FI_k = \frac{\sum_{j=1}^{n_k} A_j D_j}{\sum_{i=1}^{n} A_i D_i} \tag{35}$$

As a consequence, for this yield model, a physical significance can be attributed to w_j, Ω, and FI_k:

- w_j - represents the average number of critical defects associated with fault j;
- Ω - describes the percentage of *tested* critical area (i.e., associated with detected faults), weighted by the *relative* defects densities. In fact, due to equation (33), where ratios of $A_j D_j$ occur, only the *relative* defect density of each individual *PhFM* influences the weighted fault coverage. Of course, if only one *PhFM* is considered as likely, Ω represents simply the ratio of two critical areas, the tested area, divided by the total critical area. In our work, we take the defect density of shorts between metal_1 lines, D_o, as reference.

- FI_k - represents the percentage of critical area associated with fault class k, weighted by the *relative* densities of the defects causing the faults.

The important point from all these equations is that, if all the defect densities were to increase by a factor β, the yield will decrease (equation (32)); however, the weighted fault coverage will remain the same (equation (33)). Finally, DL will increase, as expected. This work establishes a mathematical basis in order to quantify a good layout for a given set of defect densities.

0.3.2 Defect Clustering (Negative Binomial Yield Model)

The generalized negative binomial model is commonly employed to account for defect clustering [21] and is characterized by

$$1 - p_j = (1 + \frac{A_j D_j}{\alpha_j})^{-\alpha_j} \tag{36}$$

where α_j is the clustering parameter. The smaller the α_j value, the stronger the clustering. In this case, although the faults are no longer independent, the general yield expression, (5), still holds [21]. As a consequence, we may still use the general equations (12) and (13). Under the assumption of this yield model, the weighting factor has a more complex dependence on the critical areas and defect densities, since

$$w_j = -ln(1 - p_j) = \alpha_j ln(1 + \frac{A_j D_j}{\alpha_j}) \tag{37}$$

However, equations (15)-(17) still apply, provided that equation (37) is used for the evaluation of w_j. As a general conclusion, we may point out that the influence of the yield model on DL can be computed from equations (15)-(17), where the weighting factors are evaluated in accordance to the specific yield model, which may include clustering.

0.4 Simulation Examples

0.4.1 Software System

In order to evaluate, in the IC design environment, the Defect Level, and to estimate the influence of the defect statistics and layout style, the software package depicted in Fig. 1 has been used.

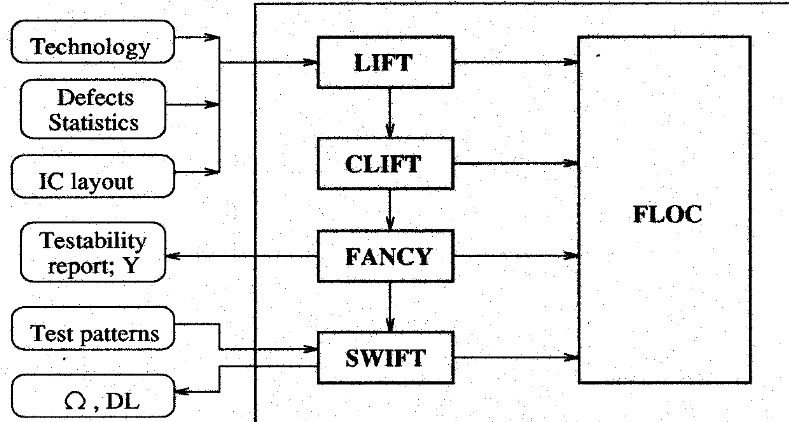

Figura 1: Software package for Defect Level evaluation.

Here, `LIFT` is the circuit and realistic fault extractor. Together with the circuit netlist (at transistor level), `LIFT` outputs a realistic fault list. Each fault has assigned to it a set of attributes, namely, the fault type, the physical failure mode (*PhFM*) originating it, and the weighting factor, w_j, evaluated as described above from the critical areas evaluation and from the process line defect statistics. At present, in `LIFT`, two basic types of faults are defined, BRI (bridging) and LOP (Line OPen) faults. *PhFMs* are user's defined, being usually, for a digital CMOS process, interconnection failures and device failures, as described in Table 1. In this Table, MOS transistor drain to source shorts are taken into account, as poly opens occuring in channel areas. Other failures can be considered, as, for instance, gate oxide shorts (due to thin oxide pinholes), or metal_1 opens due to metal_1/poly step coverage problems. However, as no defect statistics for these failure mechanisms are available to the authors, these failure modes were not included.

Fault collapsing is performed by `CLIFT`, for which different collapsing rules can be applied; here, faults topologically equivalent but caused by different *PhFMs* are not collapsed, in order to allow the identification of the elementary faults. An additional advantage of defining the weighting factors as in equation (14) can be seen by the fact that, when fault collapsing is performed, the weighting factor of the remaining faults can be easily computed. In fact, when eliminating faults from the fault set, without distorting the representativeness of the faults, the weighting factor of each remaining fault (representative of itself and of the collapsed faults) is evaluated by simply adding the w_j of remaining fault to the w_j of the collapsed faults; for the Poisson yield model, this corresponds to adding the critical areas of the equivalent faults.

Layer(s)	Failure Nature	Relative Density
Diffusion	open	α_d
	short	β_d
Polysilicon	open	α_p
	short	β_p
Metal_1	open	α_{m1}
	short	1.0
Metal_2	open	α_{m2}
	short	β_{m2}
Al/diff. contacts	open	α_{cd}
m1/poly contacts	open	α_{cp}
vias	open	α_{cv}

Tabela 1: Likely Physical Failure Modes (*PhFM*) in a digital CMOS process.

Fault classification is carried out by `FANCY`, which also computes FI_k and Y, and estimates Ω and DL. `FANCY` further descriminates TSOP (Transistor Stuck-OPen) faults, since this type of faults has received considerable attention in the literature, in the last decade. TSOP faults are a subtype of LOP faults which disconnect single channel terminals (source or drain) from the broken nodes. Moreover, a refined classification of BRI and LOP faults has been proposed, to descriminate hard from easy to detect fault subsets [7]. Extensive fault simulation allowed us to estimate Ω_k for the different fault classes, and thus to estimate DL. However, a switch-level fault simulator, `SWIFT`, can be used (and was used for the following examples, for improved accuracy), to compute Ω_k and Ω. For layout and fault inspection, an additional tool, `FLOC`, is available. `FLOC` is a graphics display program, which allows the visualization of the layout and the faults location and attributes, as well as bar or pye charts of the fault incidences, according to different fault classes or *PhFMs*.

0.4.2 Simulation Results

The results reported in this paper deal with:

- *two CMOS physical designs* of the same logic network (i.e., the `c432`, an ISCAS benchmark circuit [22]), which show the influence of the layout style and of the cell library on Ω and DL; the two physical designs are referred as `c432a` and `b`.
- *two defect statistics*, one from an european IC manufacturer's data (dominated by bridging defects, and referred as `R1`), and a more balanced defects statistics

(R2) (balanced in terms of opens and shorts), to show how defects statistics modulates w_j, FI_k, Y, Ω and DL. In R2, equal relative defect densities are assumed. Both statistics include the full spectrum of likely *PhFMs* depicted in Table 1. Numerical results have been computed for the Poisson yield model.

- *two defect densities* of metal_1, namely D_o=2 and 0.8 defects/cm^2 (and the same *relative* defect densities for the different *PhFMs*), to highlight the effect on Y but not on Ω.

Comparison, of course, is also made with the equiprobable approach ($T = m/n$), and with the DL values, computed from realistic Y, and gate-level, single line stuck-at fault coverages (referred as FL, or *fault level*).

Fig. 2 shows the influence of the defects statistics on the non equiprobability of the extracted faults. The 45° line corresponds to the equiprobable case. It can be seen that the real process line defects statistics (R1) leads to less than 50% of the extracted BRI faults accounting for more than 90% of the fault incidence. This fact must be taken into account when test preparation costs, namely test generation and fault simulation costs, are being defined. Furthermore, if BRI faults are very likely to occur (as in this example), one should include them in the fault model as target faults, to obtain low Defect Levels.

In the past, a number of papers and considerable energy has been directed at research to develop automatic test pattern generation tools for TSOP faults. Also, a large effort was undertaken to find such physical examples, with limited results. The work reported in this paper shows that, in fact, the TSOP faults give a negligible contribution to the weighted fault coverage, Ω, even for processes where open faults are significant (R2), and provides a physical explanation for it. At most, for such processes, effort such be directed at more general LOP faults (splitting the branches converging to the broken node in unique subsets, physically possible), not at TSOP faults.

In order to further highlight the influence of the fault's non equiprobability, Fig. 3 depicts the fault weights (closely related to their probability of occurrence) of metal_2, metal_1 and poly shorts, in one of the examples. It can be seen that a significant number of extracted faults are associated with limited critical areas, and thus only weakly influence the weighted fault coverage. Also, shorts between long interconnection lines (especially, metal lines) dominate this standard cell layout. Hence, routing can play an important role in the Defect Level of digital ICs.

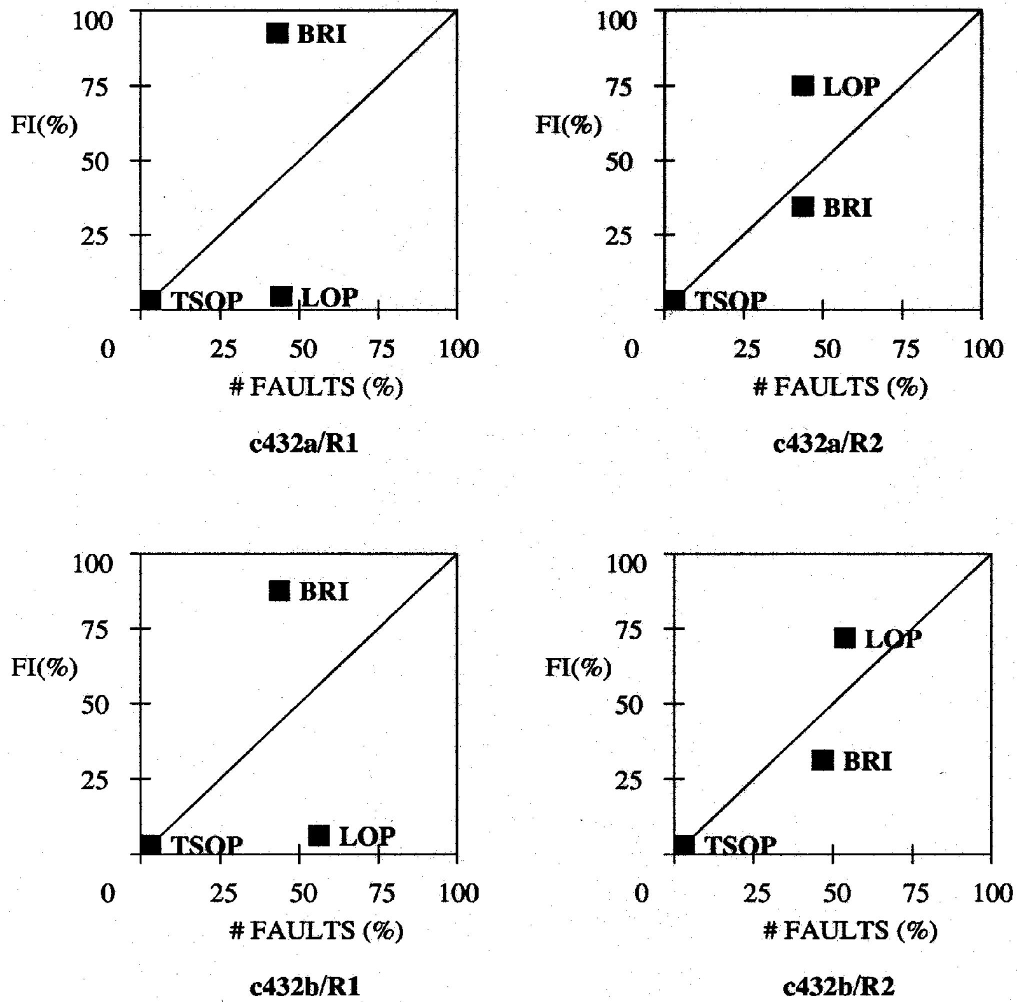

Figura 2: Fault incidences versus the percentage of faults, for different physical designs (`c432a, b`) and defect statistics (`R1, R2`).

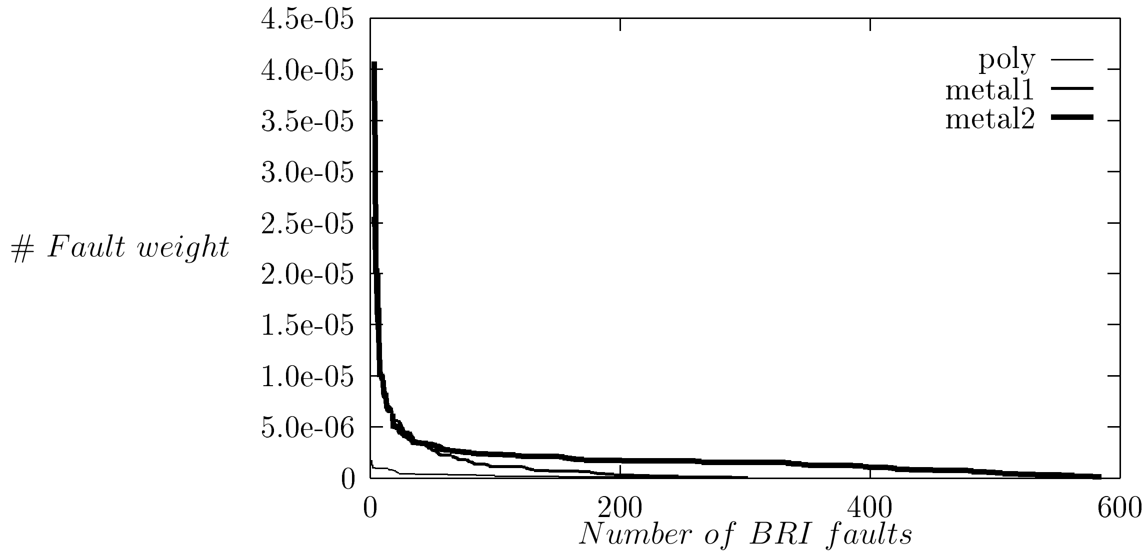

Fig. 3 - Weighting factors of ranked metal_2, metal_1 and poly shorts associated with `c432a/R1/2`: (a) linear scale.

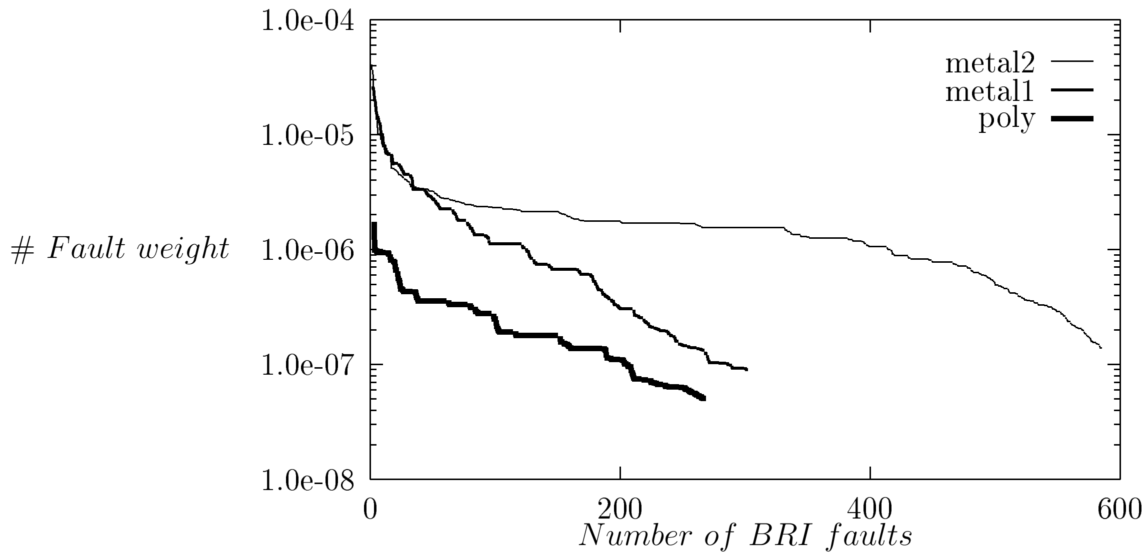

Fig. 3 (cont.) - Weighting factors of ranked metal_2, metal_1 and poly shorts associated with `c432a/R1/2`: (b) log scale.

Finally, in Table 2, a comparison is made among the different physical designs, defect statistics and defect densities. The deterministic set of test patterns used

was a stuck-at test set, i.e., it was derived for Line Stuck-At (LSA) fault detection, leading to T = 91.4%. However, the *weighted* fault coverage can be significantly different from T. In fact, for `R1`, dominated by BRI faults, Ω is consistently higher than T, which shows that the stuck-at test sets are efficient in covering well bridging faults, although these are non target faults. Considerable study of non target faults has been done by Mercer et al. [23].

Example	T (%)	Ω (%)	Y (%)	DL (ppm)	FL (ppm)
`c432a/R1/2`	91.4	98.6	99.91	12.5	77.4
`c432a/R2/2`	91.4	79.1	99.61	813.6	356.0
`c432b/R1/2`	91.4	97.7	99.88	26.7	103.3
`c432b/R2/2`	91.4	76.6	99.54	1089.7	396.4
`c432b/R1/.8`	91.4	97.7	99.95	11.5	43.0

Tabela 2: Fault coverage, weighted fault coverage, yield, defect and fault level.

One conclusion that can also be drawn from Table 2 is that it is very difficult, for the circuit designer, to evaluate DL using only the classical approach, where T and an estimated yield are used. Here, we used for Y the computed values from the realistic fault list, and, as a consequence, the estimated value (FL) can vary from 43 to 396 ppm. This variability is caused by different values of Y. The high values obtained for Y in this example are due to the small layout area (less than 1 mm ^{2}). The classical fault coverage, T, is thus a unreliable metric for test quality.

Moving to the weighted fault coverage, it can be seen that open faults are more difficult to detect by this test pattern, as Ω is around 98% for `R1`, but only around 78% for `R2`. Such a difference produces a very significant change on DL; for instance, for the `c432a` circuit, for `R1`, DL=12.5 ppm, while for `R2`, DL=813.6 ppm. These results put into evidence that the product Defect Level strongly depends on the defect statistics.

Another important conclusion is that the physical design can significantly decrease DL. In fact, for the `R1` and D_o=2 defects/cm^2 on the metal_1 lines, DL can vary from 26.7 down to 12.5 ppm (almost half the value) moving from the `c432b` to the `c432a` physical implementation. This improvement not only enhances the test efficiency (measured by the Ω increase) but also improves the design, increasing product quality.

Finally, by improving the process control, and thus reducing the defect density (as shown, by moving from D_o=2 to 0.8 defects/cm^2 on the metal_1 lines), an almost linear dependence of DL on D_o (due to the high values of Y and Ω) can be observed.

0.5 Conclusions

In conclusion, a methodology for the evaluation of the Defect Level in an IC design environment has been proposed. The methodology uses an automatic translation from physical defects to circuit faults on the basis of experimental information from the process line. This is a rather different approach as compared to the original Inductive Fault Analysis (IFA) approach [16], leading to a computationally much more affordable solution, as it can be seen from the estimates of the number of Monte Carlo trials reported in [17].

The methodology is based on an extension of the Williams-Brown model for the Defect Level to non equiprobable faults. The probability of occurrence of each individual faults is evaluated, provided that a critical area can be defined for it, either without or with defect clustering (Poisson and negative binomial yield models). A weighting factor, w_j, has been introduced, which, for the normal distribution, describes the average number of critical defects associated with fault j. The concepts of weighted fault *incidences* (FI_k) and *coverage* (Ω) were also introduced, providing quantitative measures of the relative importance of non equiprobable faults, and of the efficiency of a given set of test patterns to cover the likely faults, respectively. Ω assumes the meaning of a more general fault coverage figure.

It was shown that, to obtain DL, only the critical areas associated with the undetected faults need to be evaluated. In fact, the minimization of DL implies the minimization of the untested critical area, especially the part of it associated with large defect density failure mechanisms. This may have an interesting implication on the test strategy to adopt for a given product, since the undetected faults may be any kind of faults the ATPG is not able to detect. In particular, they can be either hard to detect faults whose fault models can be handled by the ATPG, or faults belonging to other categories (non target faults) that cannot be represented by the fault primitives of the given ATPG tool.

Furthermore, it was demonstrated, for a digital CMOS process, that the fault's non equiprobability strongly modulates the fault list, the weighted fault coverage and the Defect Level. Bridging faults have been found as dominant faults, for which the stuck-at test sets are quite efficient in covering these non target faults. Transistor stuck-open faults exhibit a negligible influence, which points out that researchers may have overemphasized their importance. However, a more general class of open faults (the LOP faults) are difficult to be detected by stuck-at test sets. When the classical LSA fault model was considered, is was verified that it constitutes a unreliable metric for DL evaluation, and thus for test quality evaluation.

Finally, it was shown in this paper that DL depends on the layout style, namely on the cell library and the routing pattern; this leads us to the conclusion that layout

level design for testability may be rewarding, especially to achieve extremely low values of DL, provided it may be automatable. Moreover, DL strongly depends on the defect statistics (defect size, distribution and densities); hence, layout sensitivity to different *PhFMs* should be analysed, to improve IC quality. The proposed methodology provides a mathematical basis to carry out such analysis.

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Main Abbreviations

BRI - bridging fault
DL - defect level
FL - fault level, DL evaluated by LSA fault coverage
LOP - line open fault
LSA - gate level line stuck-at fault
PhFM - physical failure mode
TSOP - transistor stuck-open

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