# Design and Evaluation of High Speed Parallel Multiplier Using Low Power Data Compressors

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*Abstract*— A Parallel multiplier using approximate compressors are proposed in this paper. The two new approximate 4-2 compressors are proposes that the simplified compressors have better power consumption than the optimized 4-2 compressor existing designs. These approximate compressors are then used in the restoration module of a Parallel multiplier. Four different schemes for utilizing the proposed approximate compressors are proposed and analyzed for a Parallel multiplier.

***Key words:*** Parallel multiplier, Compressor, low power, high speed

## I. INTRODUCTION

The multiplier is one of the vital hardware blocks in most of the digital and high performance systems such as digital signal processors and microprocessors. Addition and multiplication are extensively used operations in computer arithmetic .Multiplication can be thought as the repeated sum of partial products. During the past few decades ,a gathering of various multiplier architectures have been published in the literature. With the recent progress in technology, many researchers have worked on the design of increasingly more effective multipliers. Their purpose at offering higher speed and lower power consumption even while occupying reduced silicon area. This makes them well-suited for various complex and portable VLSI circuit implementations. However, the truth remains that the area and speed are two incompatible performance constraints. Hence, innovating increased speed always grades in larger area. The Parallel multiplier basically multiplies two unsigned integers. In the proposed architecture, AND array for computing the partial products generation and the partial product reduction is accomplished by the use of approximate compressor structures. The approximate compressors designs have been proposed. However, these designs is a target for multiplication. It must be noted that the attitude improves over by utilizing a simplified multiplier block that is agreeable to approximate multiplication. Initially in this paper, two innovative approximate 4-2 compressors are analyzed.

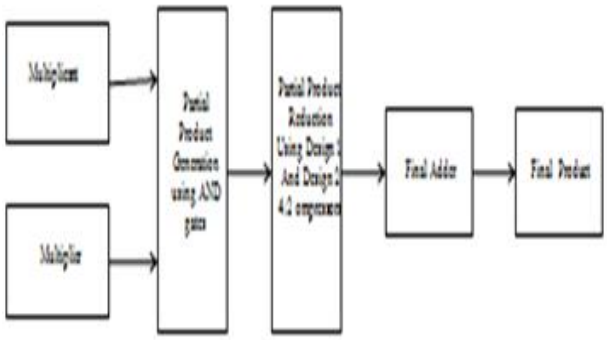



Fig. 1: Proposed Architecture of Parallel Multiplier Using Approximate Compressors.

## II. EXISTING DADA MULTIPLIER

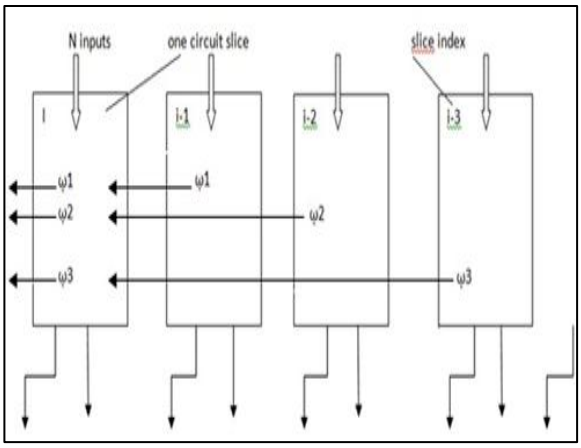



Fig. 2: N:2 compressor circuit

The main objective of parallel multiplication is to reduce n numbers to two numbers .Therefore n:2 compressors have been extensively used in computer arithmetic. A n:2 compressor is usually a section of a circuit that reduces n numbers to two numbers when properly simulated. The n number of inputs which is given to the each circuit slice .The cin which comes from the previous compressor block and the cout goes to the next compressor block. Correspondingly, the two output bits are also referred to as the sum and carry. For the correct operation of the circuit , the following discrimination must be satisfied.

$$n + \omega 1 + \omega 2 + \omega 3 + \ldots \leq 3 + 2\omega_1 + 4\omega_2 + 8\omega_3 + \ldots,$$

In general, 4:2 compressor consists of two full adder cells The approximate compressors of both design 1 and design 2 compressors have number of incorrect results and thus producing the number of error rate. The equations governing the existing 4-2 compressor outputs are shown below

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin$$

$$Cout = (x1 \oplus x2)\, x3 + \overline{(x1 \oplus x2)}\, x1$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)\, Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}\, x4$$

In this section, two designs of an approximate 4:2 design 1 and design 2 compressor used in an Dadda multiplier .In the design of a dadda multiplier, the second component plays a fundamental role in terms of delay, power consumption and circuit complexity. The existing dadda multiplier uses AND gates to generate all partial products. In the second part, the approximate compressors of both design 1 and design 2 compressors which is used for

partial product reduction. In the last part, carry propagation adder which is used for final adder. There are four different stages of approximate compressor dadda multiplier. In the first stage ,the reduction part requires 2 half-adder, 2 full-adder and 8 compressors. In the second stage, reduction part requires 4 half-adder, 1 full-adder and 7 compressors. In the third stage ,the requires 1 half-adder, 1 full-adder and 10 compressors. In the last stage , the reduction part requires 2 half-adder and 10 compressors. The objectives of the approximate compressors of both design 1 and design 2 compressors are to reduce the delay and power consumption compared with an exact multipliers. power consumption, the error distances in the third and fourth stages of multiplier designs are expected In these designs , the delay is determined by the exact compressors . As a result, there is no improvement in delay for these dada multiplier using an approximate designs compared with an exact multipliers. However, approximate compressors of both design 1 and design 2 compressors decrease the power consumption and area. Despite the fact that the multipliers have better performance in terms of delay and to be drastically lower .

## III. PROPOSED PARALLEL MULTIPLIER

In this section, two designs of an approximate compressor are proposed in a Parallel multiplier. Two different designs are proposed next to reduce the power consumption in a parallel multiplier. These compressor designs present extensive performance improvement compared to an accurate compressor with respect to delay, area and power consumption.

### *A. Design 1:*

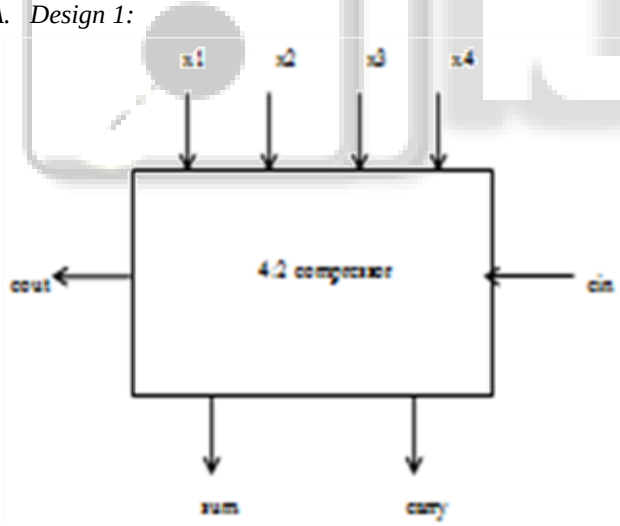



Fig. 3: 4:2 compressor

The 4:2 design 1 compressor consists of four inputs x1, x2, x3, x4 , two outputs sum and carry with cin and cout. But the carry is simplified to cin . The overall delay is reduced due to the critical path. The simplifications of carry and sum which is used to reduce the power consumption . The equations governing the 4:2 design 1 compressor outputs are shown below

$$Sum' = \overline{Cin}\ \overline{(x1 \oplus x2 + x3 \oplus x4)}$$

$$Cout' = \overline{(x1\ x2 + x3\ x4)}$$

$$Carry' = Cin$$

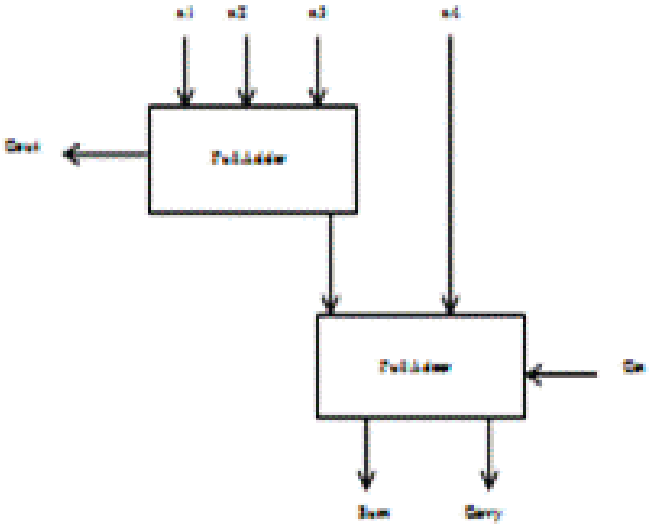


Fig. 4: Implementation of 4:2 compressor

The 4:2 design 1 compressor gate level implementation as shown in the fig.5.The critical path of this 4:2 compressor has a static delay of 3Δ as compared to an existing compressors. Nevertheless, the propagation delay through the gates of this compressor design is lower than the one for the existing compressor.

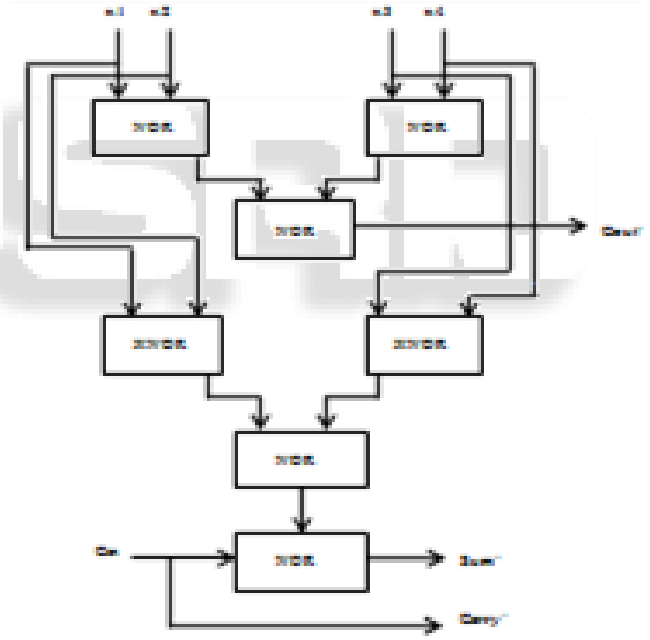


Fig. 5: Gate Level Implementation of Design 1 Compressor

The XOR and XNOR signals are generated by the XOR*. The XOR* gate propagation delay is higher than the delay through a XNOR gate. Therefore, the critical path delay in the proposed compressor design is lower than in the existing compressor design. Furthermore, the total number of gates in the proposed design is extensively less than that in the optimized existing compressor designs.

### *B. Design 2:*

A second design of an approximate compressor is proposed to further increase performance as well as reducing the power consumption compared to an previous proposed compressor design. The modified 4:2 design 2 compressor conists of four inputs x1,x2,x3,x4 and two outputs sum and carry eliminating cin and cout. In view of the fact that the

carry and cout outputs have the similar weight, the proposed equations for the approximate carry and cout in the preceding part can be interchanged. In this new modified compressor design, carry uses the right hand side of the equation and cout is constantly equal to cin. While , cin is zero in the first stage, cout and cin will be zero in all the stages. As a result , cin and cout can be neglected in the hardware design. Fig. 6 shows the block diagram of the modified 4:2 compressor . The equations governing the 4:2 design 2 compressor outputs are shown below

$$Sum' = \overline{(x1 \oplus x2 + x3 \oplus x4)}$$

$$Carry' = \overline{(x1\ x2 + x3\ x4)}$$

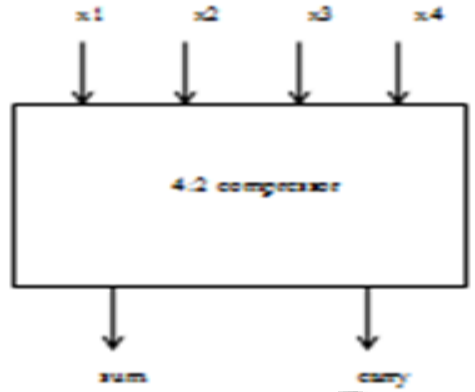



Fig. 6: Modified 4:2 Compressor

Fig. 7 shows the gate level implementation of the modified 4:2 compressor proposed design. The critical path delay of the modified 4:2 compressor design is 2Δ. Accordingly, it is 1Δ less than the earlier compressor designs. Likewise, a supplementary reduction in the number of gates is proficient.

## IV. MULTIPLICATION

In this section, the bang of using the proposed compressors for parallel multiplication is scrutinized. A expeditious parallel multiplier is frequently tranquil of three parts_ partial product generation, partial product reduction and the final adder.

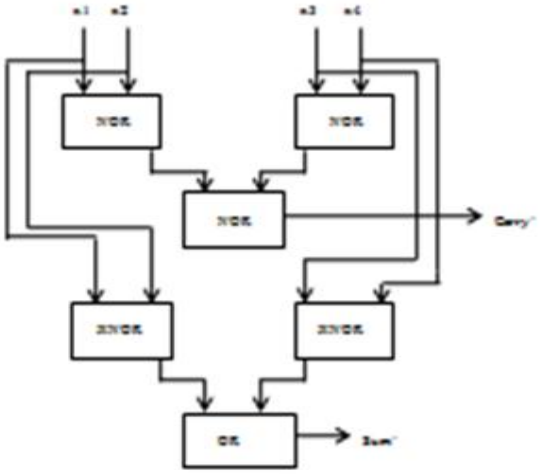
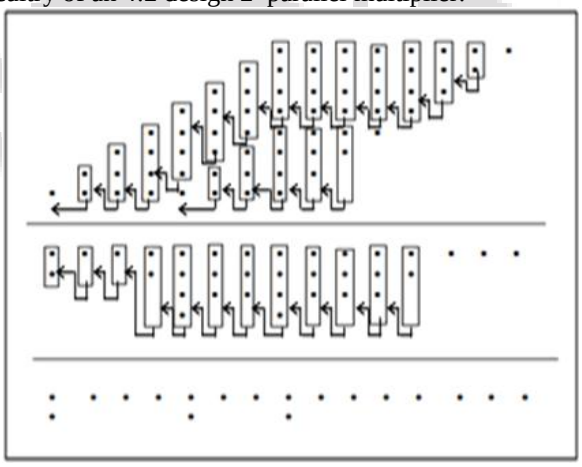
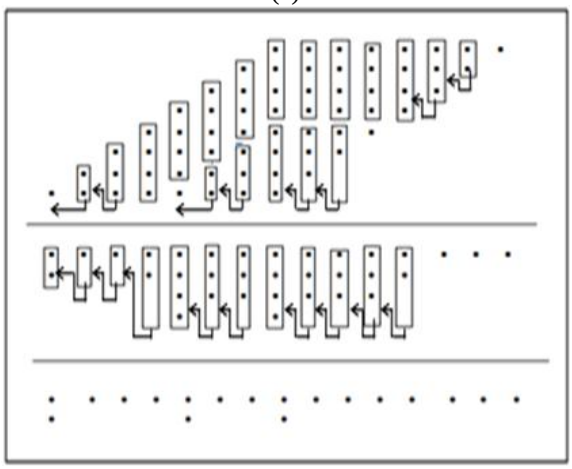



Fig. 7: Gate Level Implementation of Design 2 Compressor

In the design of a parallel multiplier using 4:2 design 1 and design 2 compressors, the second building block plays a deep-seated role in terms of delay, power consumption and circuit complexity. The use of 4:2 design 1 and design 2 compressors in the partial product reduction of a parallel multiplier results in an reliable multiplier. A 8 _ 8 mysterious Parallel tree multiplier is considered to weigh up the brunt of using the proposed compressors in reliable multipliers. The proposed parallel multiplier uses in the first part AND gates to produce all partial products. In the second part, the 4:2 design 1 and design 2 compressors proposed to reduce the partial products. The last part is the final adder. Fig. 8a shows the cutback circuitry of an reliable parallel multiplier for n = 8. In this diagram, each partial product bit is symbolize by a dot. There are four different schemes of 4:2 design 1 and design 2 compressors for a parallel multiplier. In the first scheme ,the reduction part requires 4 half-adder, 4 full-adder and 10 compressors are applied to reduce the partial products into atmost four rows.In the second scheme or last scheme, the reduction part requires 4 half-adder, 6 full-adder and 2 compressors are used to calculate the two final rows of partial products. In the third scheme ,the requires 4 half-adder, 4 full-adder and 10 compressors are applied to reduce the partial products into atmost four rows. In the last stage ,the reduction part requires 3 half-adder ,5 full adder and 2 compressors are used to calculate the two final rows of partial products. Therefore, two stages of cutback and eight half-adders, ten full-adders and twelve compressors are indispensable in the cutback circuitry of an 4:2 design 1 parallel multiplier and seven half-adders, nine full-adders and twelve compressors are indispensable in the cutback circuitry of an 4:2 design 2 parallel multiplier.



(a)



(b)

Fig. 8: Cutback Circuitry Of An 8 _ 8 Parallel Multiplier, (A) Using Design 1 Compressors, (B) Using Design 2 Compressors.

In this paper, four methods are considered for designing an 4:2 design 1 and design 2 compressor for parallel multiplier.

- In the first method (Multiplier 1), 4:2 Design 1 compressor is used in Fig. 8a.
- In the second method (Multiplier 2), 4:2 Design 2 compressor is used in Fig. 8b. In view of the fact that the Design 2 does not have cin and cout, the cutback circuitry of the parallel multiplier requires a lower number of compressors .
- In the third method (Multiplier 3), 4:2 Design 1 compressor is used in the n - 1 least significant columns. The other most significant columns n in the cutback circuitry use reliable 4-2 compressors.
- In the fourth method (Multiplier 4), 4:2 Design 2 compressor are used in the n _ 1 least significant columns and the n most significant columns in the cutback circuitry respectively.

The objectives of the first two reliable multiplier designs are used to reduce the power consumption compared with an existing multiplier. But there is no improvement in area and delay for the 4:2 design 1 and design 2 compressor designs using a parallel multiplier compared with an existing multiplier. On the other hand, it is acknowledged that the exploitation reliable compressors in the least significant columns will decrease the power consumption.

## V. RESULT AND ANALYSIS

8 Bit Parallel Multiplier using Design 1 compressor:

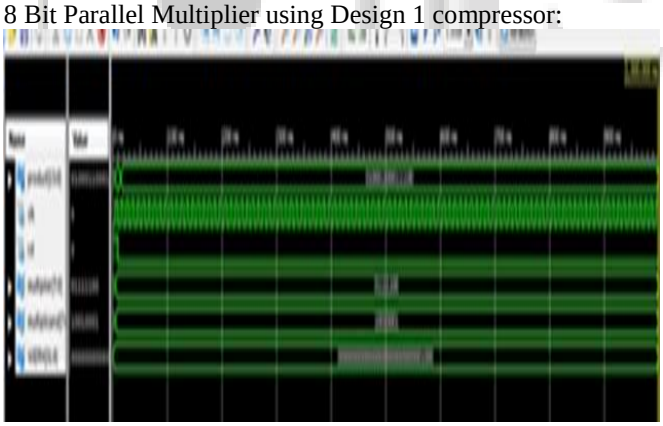


Fig. 9:

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 89 | 5472 | 1% |
| Number of 4 input LUTs | 156 | 10944 | 1% |
| Number of bonded IOBs | 34 | 240 | 14% |
| Number of GCLKs | 1 | 32 | 3% |

Fig. 10:

8 Bit Parallel Multiplier using Design 2 compressor:

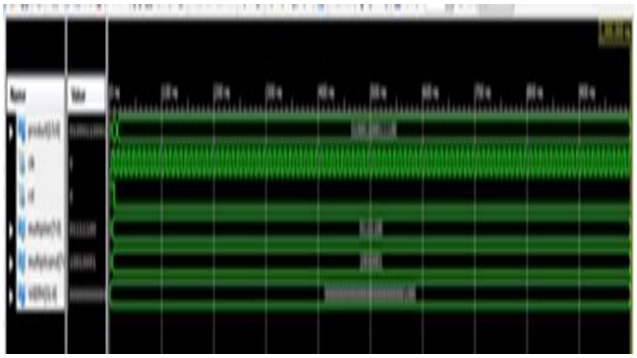


Fig. 11:

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 88 | 5472 | 1% |
| Number of 4 input LUTs | 155 | 10944 | 1% |
| Number of bonded IOBs | 34 | 240 | 14% |
| Number of GCLKs | 1 | 32 | 3% |

Fig. 12:

Table of Comparision:

**POWER:**

| Design | Total thermal power dissipation | Core dynamic thermal power dissipation | Core static thermal power dissipation | IO thermal power dissipation |
|---|---|---|---|---|
| Compressor 1 | 102.74mw | 20.66mw | 46.18mw | 35.90mw |
| Compressor 2 | 60.07mw | 1.59mw | 46.13mw | 12.34mw |

Fig. 13:

**AREA:**

| Design | 16bit register | Flipflop | Total pins | Total combinational functions |
|---|---|---|---|---|
| Compressor 1 | 1 | 16 | 34/183(19%) | 150/5.136(3%) |
| Compressor 2 | 1 | 16 | 34/183(19%) | 150/5.136(3%) |

Fig. 14:

**DELAY:**

| Design | Before clock | After clock |
|---|---|---|
| Compressor 1 | 16.721ns | 3.597 ns |
| Compressor 2 | 16.721ns | 3.597 ns |

Fig. 15:

## CONCLUSION

In this paper, the design and analysis of a parallel multiplier using approximate compressors are proposed. .The comparison result also shows that a significant reduction of power and area is achieved The results prove that the proposed architecture is more efficient than the conservative one in terms of power consumption and area. The simulation and synthesis of a parallel multiplier is done in Xilinx ISM 13.2i and Quartus 9.0. The analysis is followed using design 1 and design 2 compressors. This progress may be well-matched for multiplication of numbers with in excess of 16 bit size for high speed applications. The power of the proposed multiplier can be discover to implement high performance multiplier in VLSI applications .Because the parallel multiplier using two different compressors are providing low power as compared to an existing multiplier. Further the work can be comprehensive for optimization of parallel multiplier to recover the delay.

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