A Universal-Input Single-Stage High-Power-Factor Power Supply for HB-LEDs Based on Integrated Buck-Flyback Converter

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Abstract- Due to the high rise in luminous efficiency that HB-LEDs have experienced in the last recent years, many new applications have been researched. In this paper, a streetlight LED application will be covered, using the Integrated Buck-Flyback Converter developed in previous works, which performs power factor correction (PFC) from a universal ac source, as well as a control loop using the LM3524 IC, which allows PWM dimming operation mode.

Firstly, the LED load will be linearized and modeled in order to calculate the IBFC topology properly. Afterwards, the converter will be calculated, presenting the one built in the lab.

Secondly, the converter will be modeled in order to build the closed loop system, modeling the current sensor as well in order to develop an adequate controller.

Finally, experimental results obtained from the lab tests will be presented.

I. INTRODUCTION

Due to the high increase in performance that High Brightness Light Emitting Diodes (HB-LEDs) have been developing in the recent years, they have become an interesting and overcoming choice in most cases for general lighting solutions. In addition to their inherent high efficiency, there is no mercury inside the devices and they perform an extremely long operating life. The main purpose of this paper consists of presenting a topology for running LED streetlights from an Ac source.

Although HB white LEDs are not the most efficient lighting systems in terms of lumens per watt for streetlight applications (indeed, they achieve a lower efficiency than low-pressure sodium vapor lamps), they are quite interesting compared to traditional solutions due to their longer operating life (which reduces the maintenance costs to the minimum) and their more pleasant light spectrum (sodium lights emit only in yellow color, thus providing a very poor Color Rendering Index, CRI). What is more, HB-LEDs do not need neither warm up nor restart period, which do imply the use of specific circuitry.

Since streetlights are powered from an ac source, they must comply with European IEC 61000-3-2:2000 mandatory regulations in terms of harmonic content and power factor correction (PFC). In addition, the electronic ballast must be energy efficient and it has to be capable of working with a wide range of input Ac voltages providing an accurate current control and allowing pulse width modulation (PWM) dimming operation. These features yield the requirements that the ballast must meet: firstly, the input ac voltage must range between 90 Vrms and 265 Vrms, so it can work worldwide properly. Secondly, a power factor of at least 0.9 is generally required, and the total harmonic content must comply with Class C equipment, which refers to lighting systems [1].

There are two different ways to comply with regulations. One consists of using passive devices such as inductors and capacitors plus non-controlled rectifiers, which offers an attractive trade-off between efficiency and cost and do not generate electro-magnetic interferences (EMI). Anyway, these topologies are only good solutions for low power levels. However, the input current harmonic content is very close to the limit and some have many drawbacks with the universal input voltage range. The other consists of using switching converters, reaching high efficiency and PFC, but these circuits are complex, expensive and generate EMI. Anyway, these topologies are considered the best solution for higher power levels and for operating within the universal input voltage range [2], [3].

The simplest active PFC circuits are implemented with a single-stage that makes the power factor correction. The most common single-stage topology used is the flyback converter [3], [4] working in Discontinuous Conduction Mode (DCM), being called DCM flyback PFC converter. The main drawbacks of these pre-regulators are, by one hand, the high peak current stresses caused by the DCM and serious EMI problem [3] and, by the other, the poor dynamics that these converters perform due to the low-pass filter (10 Hz-20 Hz) needed to reduce the input line current total harmonic distortion (THD). Therefore, if dimming operation is required, which must be done at frequencies above 200 Hz, these single stage solutions are not feasible [1].

Attending to the reasons exposed above, a two-stage is needed so the Power Factor Correction can be done properly and a fast enough output dynamics is obtained. The way for implementing this system consists of a PFC pre-regulator in DCM working as an input current shaper (ICS) followed by a Dc converter in cascade, usually a boost converter for the first stage and forward or flyback converters for the second one [1], [5], although buck-boost and even buck converters may be used for the former. These topologies are a very good solution,
being capable of reaching unity power factor, and providing fast output dynamics, but they increase the size of the device and therefore, the costs.

A good solution is to implement the so-called Integrated Single-Stage (ISS), which implies the integration of the PFC stage with the dc converter, usually eliminating one transistor and making the two stages to share the remaining device. These topologies represent a good solution when unity power factor is not needed, and perform a fast output dynamics equivalent to that of two-stages PFC converters, but reducing the size of the whole converter and therefore, the cost. In addition, the efficiency is usually very high when operating under narrow input voltage range conditions, because most of the power is switched only once or just a small part is switched twice within a switching period [2].

The topology proposed in this paper is the Integrated Buck-Flyback Converter (IBFC) [6] developed in a previous work, which is composed by a buck converter working in DCM for the PFC stage integrated with a DCM flyback dc converter which supplies the power to the LED lamp. The operation in DCM is fundamental so the PFC can be carried out and the flyback converter is able to work as a current source, as will be stated later in the paper [7].

Further lines of development will take in account the implementation of a digital control system that will regulate the output current, will perform a LED temperature acquisition and will allow PWM dimming operation mode.

II. HB-LEDs AND LOAD DESIGN

HB-LEDs are usually low power devices, ranging from 1 W to 5 W at currents from 350 mA up to 2000 mA in the latest devices, while performing luminous efficiencies around 100 lm/W at 350 mA [8], [9]. The fact that they are low power devices means that many of them will be necessary for wide area lighting applications such as streetlights.

The devices chosen for the first prototypes were the DragonTape from Osram [10], composed of six Golden Dragon LEDs in series attached to a flexible self-adhesive tape, achieving a luminous efficiency of 21 lm/W at 350 mA (this means 7.2 W of power dissipation by tape). Since as forward current rises the luminous flux decreases, and lifetime decreases too, the design is focused on providing the nominal current of 350 mA.

The nominal power requirement for most LED streetlights ranges from 60 W to 150 W [1]. The load finally chosen is made of 10 DragonTapes run at 350 mA, composing a 60 LEDs load emitting 1500 lumens at a nominal power of 72 W.

The second step in the load design consists of its modeling. In a first step, the data obtained from the datasheet [11] are used. The simplest linear model takes in account only the equivalent resistance of the device at the nominal operating point. This is a valid method only if the load is going to work in a narrow range around the nominal point.

Otherwise, this approximation yields to unacceptable errors due to the great difference between the equivalent resistance at the operating point and the dynamic resistance, much higher the former than the latter. Therefore, the most accurate approximation is the one consisting of a threshold voltage and a dynamic resistance in series, as shown in Fig. 1.

Then, the LED load I-V model would be the following:

\[ V_D = R_D \cdot I_D + V_{th} \]  

(1)

Where \( V_{th} \) is the forward voltage drop of the LED, \( R_D \) is the dynamic resistance, \( I_D \) is the LED current and \( V_{th} \) is the threshold voltage. Considering the whole string in series, the expression for the output voltage is the same, but multiplied by the number of LEDs in series:

\[ V_D = N \cdot (R_D \cdot I_D + V_{th}) = R_D \cdot I_D + V_{th} \]  

(2)

Where \( V_D \) is the entire string output voltage, and \( N \) is the number of LEDs in series. For a theoretical design, the large number of LEDs used make no need for considering the whole forward voltage range that features unbinned LEDs. The variation of forward voltage drops are assumed to be a random variable, so placing a large number of devices in series will cause the random variables to sum together, and this has the effect of lowering the standard deviation of the forward voltage drop across the whole LED load. Therefore, a statistical approach can be done instead of designing the load in worst-case conditions [12][13].

The LED modeling process done in the lab consisted in obtaining the forward voltage for several current values, taking steps of approximately 50 mA during few seconds and letting the devices to cool down again, so the heating effects on the threshold voltage were negligible. The results extracted from the test, as well as the load threshold voltage and dynamic resistance obtained from a linear interpolation, are shown in Table I, as well as in Fig. 2.

III. PROPOSED TOPOLOGY

The converter proposed in this paper takes, as a starting point, the topology of the IBFC for High Power Factor (HPF) presented in [6], which consisted in the integrated buck-flyback converter for HPF off-line power supplies, having been adapted for Metal-Halide lamps in previous works [7]. The purpose of this work is to investigate and evaluate the feasibility of this converter for driving a LED load.

![Fig. 1. Equivalent circuit of a diode: linear model.](image)
In this way, the inverter stage has been eliminated, keeping the buck converter for the PFC and the flyback for regulating the output power. As shown in [6], when the IBFC is being operated in DCM in both inductors, the bulk capacitor voltage or bus voltage (VB) does not depend on the load, duty cycle and switching frequency, depending only on the ratio between buck and flyback inductances (LB and LF respectively). This is an important feature, since it provides PFC and fast output voltage regulation, that is, fast output dynamics, which is extremely important if PWM dimming operation is going to be performed. The topology proposed is shown in Fig. 3. Its operation is equivalent to two converters in cascade. The buck converter is only capable to work while the bulk capacitor voltage is lower than that of the rectified line, thus driving an averaged sinusoidal current. For complying with IEC 61000-3-2 regulations, the bulk capacitor must be low enough, so that a target conduction angle of 130º is achieved [6].

The first step calculating the topology consists of obtaining the ratio between the bulk capacitor and the line voltages. This relation depends on the conduction angle and can be specified as follows:

\[
m = \sin \left( \frac{\pi - \theta}{2} \right) = \frac{V_B}{V_g}
\]

(3)

![Graph](image)

**TABLE I**

<table>
<thead>
<tr>
<th>(I_D(A))</th>
<th>(V_D(V))</th>
<th>(R_{D}(\Omega))</th>
<th>(V_f(V))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.102</td>
<td>177.2</td>
<td>87.2</td>
<td>170.1</td>
</tr>
<tr>
<td>0.150</td>
<td>182.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.208</td>
<td>189.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.249</td>
<td>192.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.301</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>0.352</td>
<td>201.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.403</td>
<td>205.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.453</td>
<td>208.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.492</td>
<td>211.8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Where \(m\) is the relation between bulk capacitor and peak line voltage, \(\theta\) is the conduction angle, \(V_B\) is the bulk capacitor voltage and \(V_g\) is dc peak line voltage. It is remarkable that the maximum buck duty cycle equals that ratio between those voltages for working in the boundary between DCM and CCM.

The second step consists of determining the inductance ratio (\(\alpha\)), which is the ratio between buck and flyback inductances. This relation is related to the voltage ratio \(m\) as stated in the following expression [6]:

\[
m - \frac{1}{2} \cdot \frac{m}{\alpha} \cdot \left( 1 - \frac{2}{\pi} \cdot \sin^{-1} m \right) + \frac{1}{\pi \cdot \alpha} \cdot \sqrt{1 - m^2} = 0
\]

(4)

As can be noticed from (4), the voltage ratio between the bulk capacitor and the input power line depends only on the inductance ratio \(\alpha\). This expression can be plotted, as shown in Fig. 4. After having calculated the inductance ratio, the flyback inductance, \(L_F\), can be obtained as follows:

\[
L_F = \frac{V_B^2}{2 \cdot P_o \cdot f_S}
\]

(5)

Where \(D\) is the duty cycle, \(P_o\) is the output power in nominal operation conditions, and \(f_S\) is the switching frequency. The buck inductor is derived from the flyback using the inductor ratio \(\alpha\).

The flyback transformer ratio is obtained from making the maximum buck converter duty cycle the same as that of the flyback converter. From this, the expression derived is (6), where \(V_o\) is the output voltage and \(n\) is the transformer ratio.

\[
m = \frac{V_o}{n \cdot m \cdot V_B + V_0}
\]

(6)

![Graph](image)

Fig. 2. Forward current \(I_D\) and forward voltage \(V_D\) values obtained from the LED lamp built and tested in the laboratory (dotted line) and linear model (dashed line).

Fig. 3. HPF Integrated buck-flyback ac-dc converter

Fig. 4. Voltage ratio \(m\) as a function of inductance ratio \(\alpha\)
Finally, the secondary stage of the DCM flyback converter behaves as a current source, as shown in Fig. 5. The output current follows the law stated below:

\[ I_0 = \frac{V_P^2 \cdot D^2}{2 \cdot L_F \cdot f_s \cdot V_O} \]  

(7)

Where \( I_0 \) is the output current. Once the output voltage is obtained -see expression (2)-, the expression (7) can be rewritten as shown:

\[ I_0 = \frac{V_p}{2 \cdot R_D} + \sqrt{\frac{V_p^2}{2 \cdot R_D} + \frac{4 \cdot V_B^2}{R_D} \cdot \frac{D^2}{2 \cdot L_F \cdot f_s}} \]  

(8)

Finally, rearranging the expression (8), the relation between duty cycle, bulk capacitor voltage and LED forward voltage for a given output current can be obtained:

\[ D = \frac{\sqrt{2 \cdot L_F \cdot f_s \cdot I_0 \cdot (I_0 \cdot R_D + V_p)}}{V_B} \]  

(9)

Which is depicted in Fig. 6 for an output current of 350mA.

**IV. DESIGN EXAMPLE**

A universal input (90-265 Vrms), 350 mA output, 72 W at nominal operating point, 100 kHz switching frequency ac-dc converter was designed to build and test a preliminary prototype. The conduction angle was set to 130° in order to meet all the European requirements for Class C devices.

Therefore, the obtained voltage ratio from (3) is \( m = 0.423 \), which is the maximum duty cycle for the converter to operate in DCM. Additionally, with this voltage ratio, the minimum bulk capacitor voltage is 53 V whereas the maximum rises up to 158 V. The flyback inductor was built using the interleaving technique in order to minimize the leakage inductance, obtaining a value of only 0.75 µH and using Litz wire so that the losses in the wires were reduced too, employing 25x0.2 mm diameter wires in the primary and 15x0.2 mm in the secondary. The devices used are stated in Table II.

**V. REGULATION AND DIMMING**

Since HB-LEDs are current-controlled devices, a current control should be implemented rather than a voltage control. Otherwise, slight changes in the string forward voltage would lead to huge changes in forward current, being capable even to cause the complete destruction of the LED string. Moreover, the flyback secondary, operating in DCM works as a current source, so a current control could be easily implemented.

The regulation loop is based on the one developed for the IBFC in Off-Line applications [6], using a LM3524 IC which contains an Operational Transconductance Amplifier (OTA).

Based on the circuit shown in Fig. 5 the converter can be modeled in order to obtain the transfer function of the output current versus duty cycle, as follows:

\[ G(s) = \frac{i_d(s)}{d(s)} \]  

(10)

Assuming the output capacitor from Fig. 5 large enough for filtering the whole ac current component, the current flowing from the secondary stage would be the sum of the dc current through both the output capacitor (during the transient period) and through the LED load. This is represented in Fig. 7.
In this case, $I_{DC}(t)$ is the output current, $I_0$, obtained in expression (7), and therefore, the differential equation shown below is yielded:

$$i_c(t) + i_0(t) = i_{DC}(t)$$

(11)

Substituting in the equation above:

$$C_o \frac{dV_o(t)}{dt} + \frac{V_o(t) - V_v}{R_o} = \frac{V_o^2 \cdot d(t)^2}{2 \cdot L_F \cdot f_2 \cdot V_o(t)}$$

(12)

Where $C_o$ is the output capacitor, and $V_o(t)$ is the output voltage, $V_v$ the threshold voltage, and $R_o$ the dynamic resistance of the entire LED string.

Rearranging and linearizing expression (12) at the nominal operation point, the following transfer function is yielded:

$$G(s) = \frac{i_o(s)}{i_o(s)} = \frac{2 \cdot \frac{I_o}{D \cdot C_o \cdot R_o}}{s + \frac{V_o}{V_o} + \frac{I_o}{R_o} \cdot \frac{R_o}{C_o}} = \frac{4.5 \cdot 10^4}{s + 8813}$$

(13)

In some operation conditions it could be interesting to perform a PWM dimming in order to adapt the luminous flux to the ambient light, to work as a signaling light point or even to save power and allow the lamp to cool down in case of overheating. If the dimming frequency is above 200Hz, the human eye perceives a loss in the luminous intensity instead of flickering. In this way, the regulation loop was developed in order to achieve at least 1 kHz of bandwidth, so dimming can be easily carried out at frequencies over the previously commented. Moreover, for avoiding electrical stresses in the LED load, a first-order behavior was looked for.

The regulator was designed using the Sisotool toolbox from Matlab, obtaining the following PI controller, with an additional pole added in order to get rid of a high frequency oscillation noticed during the lab tests:

$$C(s) = C_p \cdot \frac{s + s_2}{s \cdot (s + s_p)} = \frac{6.06 \cdot 10^5}{s + 8792}$$

(14)

Where $C_p = g_m/C_2$, $s_2 = 1/C_1 \cdot R$ and $s_p = C_1 + C_2/C_1 \cdot C_2 \cdot R$

This regulator was built using the OTA included in LM3524 IC, using the topology shown in Fig. 8. The 517 nF capacitor was obtained by connecting a 470 nF capacitor in parallel to another 47 nF one.

In order to close the loop measuring the current through the LED load, a 1 Ω resistor was placed in series for sensing the voltage drop across it, which is directly proportional to the current. This value was chosen as a trade-off between low power dissipation in the measuring system and voltage values high enough to avoid sensible high frequency noise. Anyway, the voltage signal measured coming from the output had to be conditioned and amplified, since there was some high frequency noise and the voltage value obtained from the output was too low for the OTA controller common mode input. In this way, a first order low-pass filter was implemented using the rail-to-rail LM358 IC. Since the minimum value of the ramp generated in the LM 3524 IC goes down to 0.6 V and the maximum rises up to 3.2 V whereas the minimum common mode input voltage is 1.5 V, the reference voltage value was set to around 2.5 V, so a gain of 7 should be set. Using a non-inverter first order Butterworth topology, a gain of 6.6 was achieved, so the reference voltage value was finally set to 2.31 V for keeping the output value in 350 mA, and the chosen cut-off frequency was around 20 kHz. The final open loop Bode diagram, considering the current sensor and the controller, is shown in Fig. 9.

Finally, PWM dimming can be carried out in three main ways, which will be dealt with in future development of this topology. The first, called “Enable Dimming” consists in turning on and off the whole converter like an Enable/Disable action. If this action is taken at a frequency above 200 Hz, the eye will notice a loss in the luminous intensity. The second, called “Series Dimming” consists in displacing a switch in
series to the load, and applying a dimming signal to it, the load is set to be an open circuit during the time it should not be lit on. The main drawback of this solution is the high-electrical stresses that appear in the switch used for dimming the light.

The last, called “Shunt Dimming” consists in displacing a switch in parallel to the load, and applying a dimming signal to it, the load is shunted during the time it should not light [13]. The main drawback of this solution is the dissipation of the energy stored in the output capacitor, done through the transistor, which could be easily destroyed.

VI. SIMULATION AND EXPERIMENTAL RESULTS

Simulations were carried out using PSIM 6.0. The converter was simulated first in open loop, in order to test whether the topology was adequate for the LED load. Only the most interesting simulations were taken in account: ac input current and output current for both minimum and maximum input voltages, since those are the worst-case operating conditions, and the nominal operation input voltage, 230 Vrms.

The prototype was tested with an EMI filter at the lowest input voltage (90 Vrms), maximum input voltage (265 Vrms) and at an intermediate input voltage (150 Vrms), as well as at the nominal input voltage for Europe (230 Vrms). The experimental results obtained are summarized in Table IV, where $V_g$ is the input voltage, $I_o$ is the output current, $V_o$ is the output voltage, $P_o$ is the output power, $P_i$ is the input power, $PF$ is the power factor, $\eta$ is the efficiency, and $THDi$ is the input current total harmonic distortion. In Fig. 10 both line current and voltage are shown for the different line voltage levels tested. The conduction angle of the input current is similar to that obtained from the theoretical design and simulations. Fig. 11 shows the detailed waveforms of the drain-source MOSFET voltages as well as the gate signal for two different operating points. Fig. 12 illustrates the line voltage and bus voltage in order to verify the ripple voltage obtained.

Closed loop tests were performed as well, setting a variable reference that consisted in a 1.3 V dc level and a 0.3 Vp-p square wave superimposed at a frequency of 400 Hz. The input voltage was set to 150 Vrms and a 530 $\Omega$ resistor was used to simulate the LED lamp. The results obtained are shown in Fig. 13 whereas in Fig. 14 the whole circuit is shown.

Finally, Fig. 15 represents the obtained efficiency as a function of the input voltage. A maximum of about 80% is obtained for 150 Vrms.

Table IV.

<table>
<thead>
<tr>
<th>$V_g$(Vrms)</th>
<th>90</th>
<th>150</th>
<th>230</th>
<th>265</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_o$(A)</td>
<td>0.351</td>
<td>0.353</td>
<td>0.353</td>
<td>0.354</td>
</tr>
<tr>
<td>$V_o$(V)</td>
<td>202.6</td>
<td>202.2</td>
<td>203.9</td>
<td>202.4</td>
</tr>
<tr>
<td>$P_o$(W)</td>
<td>71.2</td>
<td>71.5</td>
<td>72.1</td>
<td>71.7</td>
</tr>
<tr>
<td>$P_i$(W)</td>
<td>91.1</td>
<td>89.6</td>
<td>92.6</td>
<td>93.8</td>
</tr>
<tr>
<td>$PF$</td>
<td>0.948</td>
<td>0.950</td>
<td>0.97</td>
<td>0.953</td>
</tr>
<tr>
<td>$\eta$ (%)</td>
<td>78.2</td>
<td>79.8</td>
<td>78.2</td>
<td>76.5</td>
</tr>
<tr>
<td>$THDi$ (%)</td>
<td>32.5</td>
<td>31.0</td>
<td>27.5</td>
<td>29.3</td>
</tr>
</tbody>
</table>

Fig. 10. Line current and voltage at different line voltages. Top: 90Vrms, 50V/div, 2.5A/div; middle: 150V rms, 100V/div, 1A/div; bottom: 265Vrms, 100V/div, 0.5A/div. Horizontal scales: 5ms/div.

Fig. 11. Upper side of the pictures: MOSFET drain-source (top), 200V/div and gate signal (bottom), 10V/div at 150Vrms input voltage, horizon. scale: 1ms/div . Bottom side of the pictures: zoom of the signals above, 5µs/div. Left: maximum input voltage point. Right: input voltage below bus voltage.

Fig. 12. Ripple voltage at the bulk capacitor and line voltage. Left: 90Vrms input, 50V/div for both traces. Right: 265Vrms input, 100V/div for both traces. Horiz. scale: 5 ms/div.
REFERENCES


[8] Luxeon K2 with TFFC, datasheet DS60 (June 2008).


