On-Chip Detector for Single-Event Noise Sensing with Voltage Scaling Function

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SUMMARY In this paper we present an on-chip noise detection circuit. In contrast with the previous works concerning on-chip noise measurement, this detector does not assume specific noise properties such as periodicity. The detector is able to continuously capture 10 nano-second time window from the measured signal with a resolution equal to 100 pico-second. The requested bandwidth of the output channel can be adjusted freely, therefore, the user can avoid the effect of on-chip parasites and the need to off-chip sophisticated monitoring tools. The detector is equipped with an on-chip programmable voltage divider, which enables measuring the high and low swing fluctuations accurately. Therefore, the detector is suitable to measure the non-periodic/single event noise for the purpose of reliability evaluation and performance modeling. The detector is implemented in a test chip using Hitachi 0.18 μm technology.

key words: on-chip detector, non-periodic noise, high-swing noise

1. Introduction

The continuous progress and scaling of semiconductor technology put the noise issue among the major concerns of VLSI designers. The power supply/ground fluctuations and inductive/capacitive crosstalk can cause severe problems to the system performance and/or reliability. These problems can be ranged from decreasing the system throughput to causing glitches on wires, which may result in function failure. No doubt that familiarity with the nature of on-chip noise will be helpful to the VLSI designer in taking these phenomena into account during the design phase of the subsequent system generation and/or precisely predicting the performance of the off-the-shelf product. CAD tools are using more and more sophisticated models of the distribution network in order to give chip-designers the ability to find potential problems in simulation [1]. However, an on-chip noise detector is necessary after fabrication to keep an eye on-chip to observe the abnormal events, which helps to evaluate the system reliability and performance.

Although there are analog methods to measure noise waveform [2], it is difficult to directly probe the noise signal. That is, the inductive response of interconnects and bonding wires limit the bandwidth of the signal that would be directed off-chip. Instead, some on-chip measurement circuits have been designed to sense specific properties of noise that can be extracted without the need for high-speed interface [3]. Assuming particular noise characteristics such as periodicity, some researchers have used the sub-sampling technique and built an on-chip oscilloscope [4]–[6]. By sampling the high bandwidth (periodic) signal once per period (or more) and drive the sampled signal off-chip, the bandwidth of output signal can be significantly made lower than that of the signal being measured. In [7], they proposed a circuit to detect the peaks and droops events over a window of time. By performing repeated measurement at different threshold level, the circuit can provide information about the distribution of supply noise. It can be noticed that those works had assumed periodic noise signal to be able to use the sub-sampling technique in order to overcome the large bandwidth of the signal being measured. However, it is difficult to apply any of the above works as a single-event detector where the signal is not periodic, for example, when the chips under test communicate with other systems using the spread spectrum clocking system.

In this work we developed an on-chip noise sensing circuit, which is not assuming a periodic signal. This design differs from those in previous works in the following features:

1. It does not assume the signal periodicity, which means that it is capable to detect the single-event or the non-periodic signals within the measurement time window.
2. The requested bandwidth of the output channel can be adjusted freely, therefore, the user can avoid the effect of on-chip parasites and the need to off-chip sophisticated monitoring tools.
3. The design is equipped with an on-chip programmable voltage divider and hence it can be used to detect the low and high-swing signals having double the magnitude of $V_{DD}$ in 0.18 μm technology where $V_{DD}$ is 1.8 V.

Previously in [8] we have presented a methodology to evaluate the performance of the different CMOS low-power design schemes in presence of noise. In that work, the noise has been assumed to have a non-periodic random distribution. To complete the model, we need a circuit, which is suitable to measure either the supply voltage/ground fluctuation or cross-talk noise regardless the signal periodicity. In addition to the above-mentioned features of the proposed circuit, it is also suitable for this purpose.

2. Detector Architecture and Operation

The proposed detector has been designed to measure the...
noise waveforms in an LSI design. Figure 1 shows the block diagram of the detector. The detector is equipped with a programmable capacitive voltage divider having three tabs in order to be able to measure large and small signal fluctuations accurately. Each tab consists of two capacitors and a selection switch. The desired tab is connected to the input buffer by closing the corresponding switch and opening the others. The dividing ratios of the tabs are $6/7$, $2/5$ and $1/7$ respectively. The measured signal is coupled to the sampling node by capacitor and leveled by the input buffer.

The detector is designed such that it samples the input signal over around 10 ns time window with a resolution of 100 ps. The signal is sampled during the capturing time window and stored by sample and hold array. The stored signals are multiplexed to produce the output signal. The multiplexing rate can be controlled by choosing the clock frequency such that the bandwidth of output signal fits within the frequency band of the monitoring tools off-chip and also to make it less than the cut-off frequency of parasitic low pass filter, which is resulted from the capacitive and inductive response of on-chip interconnects and bonding wires.

The sampling and multiplexing processes can significantly lower the bandwidth of the measured signal by the ratio $T_m/T_s$. Where $T_s$ is the sampling interval and $T_m$ is the multiplexing time interval. Figure 2 explains the theory of operation of the detector. It is clear that the output signal is a time-expanded version of the measured signal. For better immunity, the signal produced by the analog MUX is fed to a voltage to current converter and then driven off-chip. For convenient control of the output channel bandwidth, the clock is fed from off-chip.

2.1 Input Buffer

Figure 3 shows the schematic diagram of the input buffer. The role of the input buffer can be summarized in three points. First, it isolates DC voltage of the probed node.

![Fig. 1 Block diagram of the detector.](image1)

![Fig. 2 Example of the input and output signals.](image2)

![Fig. 3 Schematic diagram of the input buffer.](image3)
from the sample and hold (S&H) array, so that the sampling pulses do not disturb the probed node. Second, it supplies an adequate current to charge the holding capacitor within the sampling time. Third, it helps adjusting the signal being sampled to a suitable range such that it can be sampled by S&H circuit. The transistor M1 is biased by applying a short pulse (biasing pulse) on the gate of M3 before starting the sampling process. Therefore the voltage of N1 is charged to \( V_{DD} - V_{th3} \), where \( V_{th3} \) is the threshold voltage of M3. M4 is added to prevent N1 from clamping to \( V_{DD} \) by the effect of leakage current through M3. To ensure the quiescent voltage of N1, M4 is turned on (by applying a discharging pulse to its gate) for a short time after applying the biasing pulse. The timing of biasing and discharging pulses is also shown in Fig. 3. The bias level of the divider output (N1) is \( V_{DD} - V_{th3} \). Then, the threshold voltage of M1 lowers the bias level further so that simple S&H circuit can capture the signal. This configuration is referred to as detector I. M3 and M4 can be replaced by R1 and R2 respectively as shown by dotted lines in Fig. 3. This guarantees fixed biasing voltage at N1. However, it costs area overhead, increases power consumption and raises the minimum frequency that can be sensed by the circuit. The configuration in this case will be referred to as detector II. Both cases are investigated in this work. The buffer is designed such that the bandwidth is larger than 10 GHz. The frequency response of the buffer is shown in Fig. 4.

2.2 Sample and Hold Array

The sample and hold circuit is built by using NMOS sampling switch and capacitor as shown in Fig. 5. The sampling speed and accuracy are important parameters in this circuit. To maximize the sampling speed, first; the swing of input signal is made low such that the driving voltage \( (V_G - V_A) \) of the switch \( M_S \) is high enough to ensure low \( r_{SD} \). Second; the NMOS width and the holding capacitor size are optimized to minimize the circuit time constant and clock feedthrough. The input range to the sampler is set to \((0.1–0.8\text{ V})\) by the divider and the input buffer. The feedthrough is checked by simulation and it is found that the feedthrough is ranged from 23 mV to 25 mV over the mentioned input range. Since the clock feedthrough is almost unique over the S&H array, it can be processed as a DC offset voltage and taken into account during calibration. Therefore, it is not a vital problem in this design. Each S&H cell is followed by PMOS buffer, shown in Fig. 5, to isolate the corresponding sample from the multiplexing capacitor to ensure that the multiplexed samples are independent of each other. The buffer also raises the sample to a level suitable to drive the input stage of the voltage to current converter. The PMOS buffer consists of two PMOS transistors. One is a driver and is connected to the holding capacitor and the other serves as active load with current mirror.

2.3 Analog Multiplexer

The role of analog MUX is to construct the low bandwidth signal from the buffered samples. It consists of an array of switches. Each switch in the array is an NMOS transistor and is connected to a buffered output of S&H circuit as shown in Fig. 5. The switches are turned on sequentially at a given frequency to compose a signal that has lower bandwidth than that of the measured signal. For better immunity, the output voltage is then converted to current and driven off-chip. The voltage to current converter circuit is similar to that used in [4]. The feedthrough due to the multiplexing process has been studied by simulation. The results have shown that the feedthrough difference between the lowest and highest values of the input range is 15 mV, which is considered within the accuracy of the detector.

2.4 Sampling and Multiplexing Controls

The sampling and multiplexing control block comprises digital logic to generate the sampling and multiplexing pulses. As shown in Fig. 6, the block starts with pulse generator.
The pulse is fed to a delay line to generate the sampling pulses. To increase the sampling pulse width without decreasing the sampling frequency, we designed the sampling pulses generator such that three sampling pulses are overlapped. In this way, we realized enough sampling time more than the time-constant of the sampler in order to avoid the hysteresis effect of the sampler. The sampling pulse generator has been built as shown in Fig. 7. The generated pulses are positive going pulses, which are suitable to control a simple S&H circuit. However, the sampling interval is limited to the delay of two successive inverters, which is 100 Pico-seconds in this case. Note that the sampling pulse width is independent of the clock frequency. The generated pulse and the clock are fed to a shift register to generate the multiplexing (MUX) pulses. The MUX pulse width is equal to the clock period, which means that the multiplexing time is controlled by the clock frequency and hence the user can flexibly adjust the bandwidth of the output channel. It is important to note that the MUX time is limited by the retention time of the holding capacitor.

### 3. Test Chip Configuration

To examine the noise detector, a test chip has been designed using Hitachi 0.18 μm technology. The detector is used to measure the power supply noise of a noise generation circuit. The noise generation circuit comprises 5K gates CMOS inverter. It consists of four blocks as shown in Fig. 8. To obtain various noise levels, the activation of any of the four blocks is controlled from off-chip. The power supply voltages are supplied separately to the detector circuit and noise generation circuit. The detector circuit is also isolated from the noise generation circuit by using a guard ring. The detector has been replicated to check the effect of using biasing resistance instead of biasing transistor with and without the voltage divider. An on-chip decoupling capacitor (150 pf) is used to guarantee the integrity of the detector supply voltage line.

#### 3.1 Simulation Results

The designed test chip has been extracted and simulated using HSPICE. The detector and noise generation circuit are fed by clock signal having frequency 100 MHz and fully activated. To test the accuracy of the detector, the noise generation circuit is disabled by setting the inputs of the four blocks to ground. Then, the supply voltage of noise generation circuit is measured. Figure 9(a) shows the input buffer’s output (upper graph) and the detector’s output (lower graph). The results show that the output contains a small fluctuation (<30 mV) due to the difference in parasitic capacitance of the wiring among the samplers. Figure 9(b) shows the input and output of the detector when the noise generation circuit is fully activated. The noise peaks are generated at the clock edges. The amplification/attenuation factor of the input/output ratio can be measured during the calibration and hence the original signal level can be recorded as it will be explained in the next subsection. The sampling speed in this design is adjusted to 10G sample/sec and is confirmed by simulation. The measured sampling rate is 8G sample/sec at 1.8 V. By increasing the supply voltage to 2.2 V, the sampling rate reaches 10G sample/sec. The captured time-window is ~10 nsec. It can be made wider/narrower by changing the number of samplers. The clock frequency is chosen such that the bandwidth of the output channel is two orders of magnitude less than that of the input signal.
3.2 Measurement Results

Figure 10 shows the micrograph of the fabricated detector. The detector size is $640 \times 270 \, \mu m$. The detector area, $A$, can be expressed by the following equation:

$$A = \alpha + \eta \beta$$

Where $\alpha$ is the fixed (basic) area, $\beta$ is the area of one segment of Fig. 5 including the area of digital part needed for generation of the sampling and multiplexing controls and $\eta$ is the number of samplers. In our design, $\alpha$ and $\beta$ are equal to 12460 and 1160 $\mu m^2$ respectively. The detector consumes average current about 20 mA at 2 V operating voltage. The fabricated chip is tested by HP93000 logic tester and the output is monitored by a conventional oscilloscope. The input-output transfer characteristic is measured by operating the detector as an on-chip sampling oscilloscope and applying a low frequency sine wave (6.5 MHz). The input is plotted versus the output as shown in Fig. 11. Note that it is difficult to apply a high frequency signal from off-chip because the effect of parasites. The noise generation circuit is fully activated by connecting all inverter chains to a clock signal having frequency 100 MHz. The power supply of the noise generation circuit is measured by the detector. The detector captures time-windows triggered at specific points every time. Hence, within the capturing time-window, the detector is capable to report the events, which need not to periodically happen during systems operation. The original signal can be known from the monitored signal and the calibration graph shown in Fig. 11 in addition to the ratio $T_m/T_s$. To obtain the original signal, the time axis of the monitored signal is divided by the ratio $T_m/T_s$ and the value axis (vertical axis) is multiplied by the amplification/division ratio extracted from the calibration graph. In this work, $T_m$ and $T_s$ are set to 10 nano-second and 0.1 nano-second respectively. The original detected noise signal is shown in Fig. 12. It is clear that the parasitic elements (inductance and resistance) are under-estimated during the simulation.

At zero input (noise circuit is quite), the output shows some fixed pattern noise (FPN) as shown in Fig. 13. The major reason for the fixed pattern noise is due to the fluctuations of the threshold voltage of PFETs in the S&H outputs and sampling and multiplexing switches. The effect of area variations of the sampling switches has been investigated by simulation and it is concluded that those variations have a negligible effects on the accuracy of the detector. Furthermore, the detector layout is done such that the switching events in the digital part do not affect the operation of the
analog part. The clock, which controls the detector operation, has a possibility to share in generating such fixed pattern noise. However, to alleviate such effect, the power lines are made wide enough to ensure low parasitic resistance and inductance and hence the effects of the input clock and the control pulses generations on the detector accuracy are negligibly small. To check the periodicity of the noise pattern shown in Fig. 13, the autocorrelation of the signal has been calculated as shown in Fig. 14. The autocorrelation result shows that more than 80% of the noise pattern is periodic and can be removed as it is discussed later in this section and less than 20% is random, which is difficult to remove and is considered as the accuracy limit of the detector. In order to overcome the fixed pattern noise, there are two solutions.

1. Remove the PMOS buffers from the design. However in such case, the holding capacitor should big compared with multiplexing capacitor in order to make the multiplexed pulse independent of each other.

2. Modify the detector circuit according to Fig. 15. Using this modification, the FPN is removed by a way similar to the correlated double sampling method [9] where the output is independent of $V_{thP}$. $T_P$ is the active part of the measurement cycle where the sampled signals are being multiplexed. The switch $S^{out}$ is controlled by a clock signal (CK) during the time $T_P$. CK should be synchronized with the MUX pulses M2, M4, M6, etc. Since both MUX pulses and CK are generated from the input clock, it is easy to make such synchronization.

4. Conclusion

An on-chip noise detector has been designed and fabricated using 0.18 $\mu$m technology. The detector can detect the single-event or the non-periodic signals within the measurement time window. It is equipped with programmable voltage divider to be able to detect high-swing signals having maximum theoretical frequency 5 GHz. The bandwidth of the output signal can be controlled by the user to fit the monitoring tools off-chip and to avoid the effects of the on-chip parasitic elements and hence conventional equipments can be used to measure the signal off-chip. A test chip is fabricated and tested successfully.

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References

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