Low Power/Low Voltage High Speed CMOS Differential Track and Latch Comparator with Rail-to-Rail Input

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ABSTRACT

A new CMOS differential latched comparator suitable for low voltage, low-power application is presented. The circuit consists of a constant-gm rail-to-rail common-mode operational transconductance amplifier followed by a regenerative latch in a track and latch configuration to achieve a relatively constant delay. The use of a track and latch minimizes the total number of gain stages required for a given resolution. Potential offset from the constant-gm differential input stage, estimated as the main source of offset, can be minimized by proper choice of transistors sizes. Simulation results show that the circuit requires less than 86 µA with a supply voltage of 1.65 V in a standard CMOS 0.18 µm digital process. The average delay is less than 1 ns and is approximately independent of the common-mode input voltage.

1. INTRODUCTION

Differential circuit techniques have become common in many areas of analog circuit design. They are especially useful in rejecting common mode noise in integrated circuits that perform both analog and digital signal processing. In such circuits, comparators often provide a link between the analog and digital domains. At the same time, designing analog circuits that can operate from a low-voltage supply is important in today’s VLSI systems. The demand for low-voltage systems stems from three different sources. First, the rapid advent of battery operated portable systems require low power dissipation in order to prolong battery life, and a minimum number of battery cells to reduce the volume and weight of the system. The second and third reasons are due to the smaller feature sizes offered by today’s VLSI technology. Reduced device dimensions require low voltage power supplies in order to reduce internal electric fields and improve device long-term reliability. This is further driven by the need for reduced power dissipation, as a greater number of transistors are integrated on a single die. According to the SIA roadmap [1], power supply levels in the range of 1-1.65 V will be needed to keep pace with the reduction in transistor dimensions corresponding to line widths below 0.18 µm. Nevertheless, reduced power supply levels do not necessarily lead to lower power dissipation for analog circuits. Current biasing levels must also be reduced.

A consequence of the lowered power supply is the need for rail-to-rail input stages in order to compensate for the reduced input common-mode and dynamic range. Such efforts have been underway for several years now [2]. In CMOS op amp circuits, improved input range operation has been achieved by connecting complementary (NMOS and PMOS) differential amplifiers in parallel. Such circuits are referred to as having rail-to-rail operation. Similar methods have been also used in comparator designs [3]. Most of them use a switched-capacitor circuit design approach [4], [5] or an inverter-based chopper type amplification approach [6]. In [7] a continuous-time CMOS comparator with a rail-to-rail input stage has been reported. The circuit is based on a single ended design configuration. It consists of two operational transconductance amplifiers (NMOS and PMOS in parallel) in a type II active load enhancement configuration [8].

In this paper we will present a new approach to the design of a CMOS differential latched comparator suitable for low voltage, low-power applications. The new approach makes use of the well-known constant-gm rail-to-rail input stage used in amplifiers. The circuit consists of a constant-gm rail-to-rail common-mode OTA (compared to previous work [4]-[7]) followed by a regenerative latch. The circuit dissipates less than 86 µA with a supply voltage of 1.65 V in a standard CMOS 0.18µm digital process. At the heart of the design is a track-and-latch circuit. This circuit reduces the number of gain stages normally required in an asynchronous or multi-stage comparator [9] thereby reducing the power and silicon area requirements, as well as decreasing the comparator settling time. The net result is a more power efficient comparator.

We begin this paper in section 2 by introducing an overview of the architecture of the proposed comparator, followed by an evaluation of its performance in section 3. Finally, conclusions are drawn in section 4.

2. Comparator Circuit

![Figure 1:Comparator Circuit block diagram](image-url)

To optimize the performance of a comparator, one has to consider the resolution, speed and power dissipation trade-off (in a situation of reasonable devices size, i.e. offset considerations). To achieve high resolution, large gain structures are necessary. Attempting to achieve this with one power-efficient gain stage results in reduced
bandwidth due to amplifier gain-bandwidth trade-off. Conversely, medium-speed operation can be obtained by cascading several lower-gain stages at the expense of higher power dissipation. Although individual stages can be made fast, signals require time to propagate through all stages. Possibly the most power-efficient high-speed design method involves combining a low-gain (high-bandwidth) stage with a positive feedback track-and-latch circuit. In essence, this achieves a large nonlinear gain with a high-speed and low power design. Such an approach is illustrated in Figure 1. It consists of three main stages: a biasing circuit, a constant-gm rail-to-rail low-gain amplifier stage and a summing-regenerative latch circuit. The input differential voltage is converted into a differential current using the constant-gm stage. This differential current is then summed and fed to the latch circuit for a decision. Details of each stage are described below. The bulk of all pMOS (nMOS) devices in those circuits are connected to the positive (ground) supply voltage $V_{DDA}$ ($V_{SSA}$) unless otherwise stated.

2.1. Biasing Circuit

![Biasing Circuit](image)

The biasing circuit is shown in Fig. 2. It is a high swing cascode version of the $\beta$-multiplier reference of [10]. This circuit utilizes positive feedback and is stable as long as the loop gain is less than unity, which is the case when $k > 1$ (with $k$ defined as the aspect ratio of transistor MN2 over the aspect ratio of transistor MN1). The biasing current $I$ is defined by the resistance value $R$ and the aspect ratio $k$, using the first-order approximation relation described in [9].

Unfortunately this circuit has a second stable operating point where all the currents are zero. To guarantee that doesn’t happen, we have added a start-up circuit that only affects the operation if all the currents are zero at start-up. The biasing current $I$ is affected by the value of the resistance $R$. A variation of about ±20% in the resistance value leads to an approximately ±25% in the biasing current. This induced variation in the biasing current has a direct influence of the comparator resolution by means of the differential input stage gain. A typical loss of 3 bits of resolution has been observed.

2.2. Constant-gm rail-to-rail input stage

![Constant-gm rail-to-rail input stage](image)

Figure 3 shows the constant-gm rail-to-rail input stage in a high-swing cascode configuration. When a single differential pair is used as an input stage for a comparator, a small input common-mode range is obtained. A well-known technique to realize a rail-to-rail input stage is to place two complementary pairs in parallel. When the common mode input signal is close to the rails, only one of the pairs turns on while the other one is cut off. At the mid range, both the n- and p-type pairs operate. Because of this the total transconductance is not constant across the input common mode range and the delay of the comparator may vary as seen in [7]. The transconductance has twice the $g_m$ value of a single pair, assuming both pairs have the same $g_{mns}$. This is an undesirable situation because it gives delay and performance evaluation problems. An easy way to measure and control the transconductance is to tune the biasing currents of the n- and p-type pairs. The complementary input stage with three to one current mirror proposed in [11] has been used. The relation describing the way the current is distributed in the differential constant-gm input pair is well described in [11] and will not be reported here. Offset on this constant-gm differential operational transconductance amplifier will lead to an offset in the comparator circuit. This offset is mainly due to mismatch and threshold variation in the input drivers (n and p-type). At the mid-range, when both n-and p-type pairs operate, total offset is the average value of the induced offset from each pair. When the common mode input signal is close to the rails, offset contribution would be the maximum contribution coming from both input pairs. Equations describing those offsets are given below in section 3.

2.3. Regenerative latch

The regenerative output latch is based on an approach proposed in [12] and is shown in Fig. 4, together with the current summing circuit. The latch consists of discharge transistors (M6-M7), an n-channel flip-flop (M1Y-M2Y) with a pair of n-channel transmission gates for strobing (MSI-MS2), p-channel flip-flop (M2X-M3X), and p-channel pre-charge transistors (M1X-M4X). The flip-flop output is taken at the drain terminals of MSI-MS2 instead of the corresponding source nodes. This is done to increase the regeneration speed and reduce the offset [13]. In addition, the strobing transistors isolate the flip-flop from the comparator output nodes, reducing the load on the flip-flop to the gate capacitance of the flip-flop itself. Offsets caused by the channel length fluctuation (during manufacturing), estimated as the main source of offset voltage, is much lower at zero volt substrate bias [14]. Such an
effect is estimated to be the main source of offset voltage in the latch. Thus, transistors channel length can be reduced and the flip-flop speed can be made faster.

![Summing Circuit](image)

Figure 4: Summing circuit with regenerative latch

3. CIRCUIT PERFORMANCE

Our goal is to design a comparator that has high accuracy, low power consumption and high speed with a reasonable transistor size (offsets consideration). Before sizing the circuit, we investigate the main source of offset and what limits the circuit performance. There are two mains source of offset in the circuit and they can be expressed as

\[
V_{\text{offset}} = V_{\text{offset,diapair}} + V_{\text{offset,latch}}
\]

where \( V_{\text{offset,diapair}} \) and \( V_{\text{offset,latch}} \) are the offset contribution form the constant-gm differential input pair and the regenerative latch, respectively. The offset voltage in the latch circuit is systematically minimized by the latch topology [14]. Also, since the offset voltage in the latch circuit is divided by the differential amplifier gain, which is about 44 V/V in our case, most of the offset sources are in the differential stage. There are two kinds of offset sources in a MOS differential pair. They are charge density fluctuation, such as surface states and impurity concentration, and dimension fluctuation.

Offset associated with the constant gm-input pair consists of contribution from the p- and n-type differential input pairs. Offset contribution of the p-type input pair with n-type load transistor is given by:

\[
V_{\text{offset},p} = D_p \left( \frac{1}{L_n} + \frac{1}{L_p} \right) \left[ \frac{I_{bp}}{2k_p} + \Delta V T + \frac{k_n}{k_p} \Delta V T_n \right]
\]

while the one from the n-type input pair with p-type load is

\[
V_{\text{offset},n} = D_n \left( \frac{1}{L_p} + \frac{1}{L_n} \right) \left[ \frac{I_{bn}}{2k_n} + \Delta V T + \frac{k_p}{k_n} \Delta V T_p \right]
\]

where \( D_p \) and \( D_n \) denotes the channel-length imbalance between transistors pairs, for both p-channel and n-channel devices; \( I_{bp}, I_{bn}, \Delta V T_p \) (respectively \( I_{bp}, I_{bn}, \Delta V T_n \)) are respectively the channel length, biasing current of the p-type input pair and threshold variation in the p-type devices (respectively the channel length, biasing current of the n-type input pair and threshold variation of the n-type devices). The first term comes from dimension fluctuation in the differential input pair and the load transistors. Using layout techniques, such as common centroid configurations, the transistor mismatch caused by gradients can be greatly reduced. The second and third come from charge fluctuation. Since surface state density and impurity concentration can be well controlled and since the last two terms are proportional to gate oxide thickness (which is small in our case here) these terms are insignificant compared to the first. The first term is increased in inverse proportion to channel length, therefore this term was assumed dominant for the comparator offset consideration.

Numerous works has been performed on offset contribution due to mismatch problems. An useful offset estimation has been reported by Steyaert [16] and is given by:

\[
\sigma^2(V_{\text{off}}) = \frac{k_p}{g_m} (V_{GS} - V_i) \left[ A_{p} + \frac{A_{n}}{4} (V_{GS} - V_i)^2 \right]
\]

where the constants \( A_p \) and \( A_n \) are dependent technology. Table 1 in [16] summarized the value of those constants for several industrial CMOS technologies. We observe a decrease in those constants with the decrease of the minimum devices sizes. This is mainly due to the decrease in oxide thickness as has been measured in [17]. The variance reduces with increasing gate area (W/L) and with decreasing oxide thickness.

Offset voltage dependence on channel fluctuation has been reported in [12], [13]. Based on those results we choose two times the minimum length for p-channel and n-channel input driver transistors and four times the minimum length for the p-channel and n-channel load transistor. In order to achieve high comparison speed the minimum channel has been used in the latch circuit.

3.1. Simulation Results

The proposed implementation has been simulated with HSPICE using BSIMv3 0.18 μm technology. In this technology, the threshold voltage levels are approximately 0.52 V and –0.48 V for nMOS and pMOS transistors, respectively. Figure 5 shows the sum of the square roots of the tails currents of the complementary differential amplifiers used in the amplifier stage as a function of the input common mode voltage. Although the appropriate transistor scale factor is not included, it serves as a useful measure of how the amplifier \( g_m \) varies with the input common-mode voltage. In particular, here we see that the sum of the square root of currents varies between 4 and 4.7 mA \( \sqrt{2} \). A peak occurs at each end of the input common-mode voltage range, corresponding to the condition when one differential pair is partially on, while the other pair is fully on. For the device sizes chosen in our design, this corresponds to a 14% change in \( g_m \) over the full range of common-mode input voltage, as predicted by the formula provided in [11]. The simulated comparator performance using \( V_{DD} = 1.65 \) V, a switching voltage overdrive of \( \pm 0.2014 \) mV (which corresponds to a \( \pm 0.5 \) LSB of a 12 bit precision) and an inverter a load (which is the case in our application) is summarized in Table 1. The propagation delay shows little variation, and the delay in all cases remains smaller than 1ns. The propagation delay when the common mode input voltage is near one of the power supply voltage is only slightly increased above this value.
The propagation delay in Table 1, which has been simulated under static condition (Vp and VN are set to a DC input level with an overdrive of ± 0.2014 mV), is less than 1ns. An additional simulation has been performed under dynamic conditions using the worst-case driving condition waveform of a comparator described in and displayed in Figure 6. Results show an average propagation delay of about 15 ns. This is due to the speed limitation of both the NMOS and PMOS current differentiator (highlighted in figure 3). This can be improved at the price of increasing the current level.

4. CONCLUSION

In this paper a new rail-to-rail track-and-latch comparator has been presented. An important attribute of the design is that the transconductance of the preamplifier, and therefore the propagation delay, is nearly constant. The circuit operates at 1.65V and draws about 86µA of current, resulting in a power dissipation of 141µW. The propagation delay, in all cases, remains smaller than 1ns. Under dynamic conditions using the worst case waveform, results show an average propagation delay of about 15ns due mainly the differentiator circuit. The layout is in progress and some experimental results will follow soon. The rail-to-rail input range capability enables the circuit to be used in high-speed resolution applications such as flash, successive approximation and pipelined ADCs, to name just a few examples.

REFERENCES