A Two-Stage Ring Oscillator in 0.13-μm CMOS for UWB Impulse Radio

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Abstract—We present a two-stage digitally controlled ring oscillator designed mainly for impulse-radio ultra-wideband (UWB) applications. Each basic stage utilizes a local positive feedback, allowing to achieve steady oscillation at low current consumption levels, and to extend the frequency tuning over an ultra-wide range. The frequency tuning is achieved via the control of the tail resistor in each stage. The circuit is fabricated in a 0.13-μm CMOS technology. It features full UWB coverage at slightly higher than 1.3-V supply voltage, –121.7-dBc/Hz phase noise at a 5.6-GHz carrier, and 10-MHz offset, and less than 5-mW power consumption for the digitally controlled oscillator core alone at 10.18-GHz maximum frequency under 1.3-V supply voltage.

Index Terms—CMOS, digitally controlled oscillator (DCO), impulse radio (IR), low power, ring oscillator, ultra-wideband (UWB).

I. INTRODUCTION

ULTRA-WIDEBAND (UWB) systems are pushing forward circuit design techniques in submicrometer CMOS to their limits in order to achieve optimum performances in terms of high speed, low noise, ultra-wide tunability, and low power consumption. The oscillator is one of the examples being at the same time a key block in a UWB system and a challenging design since it has to accommodate the defined constraints above. In addition, using a two-stage oscillator topology looks attractive from a high-frequency and phase noise point of view, but it presents a hard tradeoff for the power consumption since the power savings with no additional quadrature-generation circuit or other stages may be lost with the high current consumption level needed to ensure steady oscillation. Therefore, the two-stage oscillator topology cannot be considered as highly attractive unless it features low-power implementation as well. From previous work in the literature addressing high-frequency ring oscillator design, De Heyn in [2] presented a three-stage ultra-wide tuning range with very low power consumption, but did not provide measured phase noise figures, allowing fair comparison with state-of-the-art results. Rezayee in [3] and [4] presented a two-stage ultra-wide tuning range (114%) oscillator with reasonable phase noise performance at the cost of relatively high power consumption. In [5], Van der Tang demonstrated a two-stage bipolar-based phase noise-optimized oscillator, but with a very short tuning range (16%) and relatively high power consumption. In [14]–[17], examples of ring oscillators balancing a relatively low noise and an ultra-wide tuning range (148%) are provided; however, they all feature a very low oscillation frequency (below 1.3 GHz) and sometimes high-power figures, which places them out of the scope of the intended application.

The emphasis on low-power high-frequency operation and wide tunability aspects with a two-stage differential oscillator implementation, for impulse-radio UWB (IR-UWB) applications, was the main drive behind this work.

IR-UWB system considerations are treated in Section II. In Section III, we briefly present a block-level small-signal analysis of the proposed two-stage oscillator topology. Section IV describes the digitally controlled oscillator (DCO) circuit design. Measurement results are presented in Section V. A comparison with the state-of-the-art performance is shown in Section VI. Finally, a conclusion is given in Section VII.

II. SYSTEM CONSIDERATIONS

The UWB spectrum allocated by the Federal Communications Commission (FCC), Washington, DC, covers the 3.168–10.56-GHz frequency range. A UWB radio is defined as any wireless transmission system that occupies at (–10 dB) a fractional bandwidth W/fc ≥ 20% (where W is the bandwidth and fc is the band central frequency), or more than 500 MHz of absolute bandwidth. UWB regulations do not specify technology, but rather rules to access the UWB spectrum. Therefore, the following two main impulse-radio (IR)-based implementations can be given [1].

• Direct sequence spread spectrum (DS-SS) (see Fig. 1): the UWB spectrum in this case is divided into two main bands, which can be used individually or together: the low-band direct sequence (LB-DS) with a 1.5-GHz bandwidth and a frequency extension from 3.1 to 5.15 GHz, and the high-band direct sequence (HB-DS) with a 3.6-GHz bandwidth and a frequency extension from 5.825 to 10.6 GHz.

• Time-division/frequency-division multiple access (TD/FDMA) (see Fig. 1): the spectrum is divided into many sub-bands, each having at least 500-MHz bandwidth. The time-domain signal consists of pulses transmitted on dynamically switched frequency channels at different given time slots.

Local oscillator (LO) generation requirements are fundamentally different between IR-UWB and orthogonal frequency division ultra-wideband (OFDM-UWB). In fact, IR-UWB allows frequency wrapping since the transmitted signals are pulses that
carry simple information depending on the digital modulation (on–off keying (OOK), binary phase-shift keying (BPSK), etc.). Even if the LO carrier drifts a bit from the band center, this drift has to be put into perspective with at least 500-MHz bandwidth. The integrated power lost or leaked into an adjacent channel, over a 500-MHz bandwidth might be relatively small and might not disturb the integrity of the transmitted data, depending on the data modulation complexity. The receiver will still be able to a certain extent to demodulate and extract the transmitted data. The added filtering at the transmitter output helps further in attenuating the LO drift effects on adjacent channels. Moreover, in the DS mode, a dead zone of 5.1–5.8 GHz is planned between low-DS and high-DS bands [see Figs. 1(a) and 2(a)] to further minimize inter-bands power leakage. Besides, the oscillator can be designed to have digitally switchable bands, with a certain resolution, and a soft-calibration performed via the digital baseband, in order to optimize the receiver signal-to-noise ratio (SNR) within a given channel. This calibration can also be done to accommodate process variations and slow drifts over temperature. All these considerations lead to the fact that no accurate oscillator locking, and therefore, no phase-locked loop (PLL), is required in the IR-UWB case. For the OFDM case, frequency wrapping is not allowed since it implies direct SNR degradation, and therefore, PLL-based frequency synthesis becomes mandatory.

In this study, we propose a DCO, with the main following specifications.

- Low power consumption, as it will be designed principally for IR-UWB applications.
- Full coverage of the UWB spectrum (Fig. 2)
  \[ F_{DCO_{\text{min}}} = 3168 \text{ MHz} + \left( \frac{500 \text{ MHz}}{2} \right) \]
  \[ = 3418 \text{ MHz} \]
  \[ F_{DCO_{\text{max}}} = 10560 \text{ MHz} - \left( \frac{500 \text{ MHz}}{2} \right) \]
  \[ = 10310 \text{ MHz} \]
- Direct in-phase/quadrature (I/Q) signals generation.

The oscillator phase noise is targeted to be competitive with state-of-the-art performance. The phase noise is normally not specified for IR-UWB since, at more than 500-MHz offset, the phase noise effect is negligible.

### III. BLOCK-LEVEL ANALYSIS

#### A. Basic Two-Stage Ring Oscillator

We begin our analysis with the linearized model of a basic two-stage ring oscillator (Fig. 3), where each basic cell is modeled with a transconductance stage \( G_m \) and an \( RC \) circuit. The open-loop transfer function can be calculated as

\[
H(j\omega) = -\left( \frac{-G_m \cdot R}{1 + jRC\omega} \right)^2.
\]  

(1)

Assuming that the phase shift introduced by \( G_m \) is small in the frequency range up to 10 GHz, and by applying the steady oscillation criteria—\( H(j\omega) = 1 \)—to (1), the oscillation condition occurs then for

\[
RC\omega \gg 1
\]

(2)

which is equivalent to

\[
G_m \cdot R \gg 1
\]

(3)

with the oscillation frequency expressed as

\[
\omega = \frac{G_m}{C}.
\]

(4)

The condition (3) implies that for a certain loss \( R \), an extremely high \( G_m \) is required in order to ensure a steady oscillation state. Consequently, this requires high current consumption level and large size components with increased parasitics, which makes this condition difficult to obtain, mainly for high-frequency operation.
B. Two-Stage Ring Oscillator Using Negative Resistance

The proposed approach in this paper consists of using an additional active positive \((Gm')\) feedback in each basic cell. This will be equivalent to a negative resistance \(Rn = -1/Gm'\) that compensates the resistive losses and makes the oscillation condition achievable at much lower power consumption. The linearized model is presented in Fig. 4. The new equivalent resistance \(Rq\) can be written as

\[
Rq = \frac{R \cdot Rn}{R + Rn} = \frac{R}{1 - Gm' \cdot R},
\]

and the new open-loop transfer function is given as

\[
H(j\omega) = \left(\frac{-Gm \cdot Rq}{1 + jRqC\omega}\right)^2.
\]

(6)

By calculating the modulus and the phase expressions of this transfer function, we get

\[
|H(j\omega)| = \frac{(Gm \cdot Rq)^2}{1 + Rq^2C^2\omega^2},
\]

\[
\tan(\phi(j\omega)) = \frac{-2RqC\omega}{1 - Rq^2C^2\omega^2}.
\]

(8)

The extraction of the oscillation condition from (7) and (8) leads to

\[
Gm > \frac{1}{|Rq|} \quad \text{and the oscillation frequency is given as}
\]

\[
\omega = \frac{Gm}{C}.
\]

The oscillation frequency in (10) is the same as the expression for a simple two-stage oscillator (4) (assuming \(Gm'\) is ideal), while the oscillation condition (9) is now dependent on a new factor. This factor facilitates steady oscillation at lower power consumption compared to the simple two-stage ring oscillator previously presented in Section III-A. This becomes particularly true around the ideal case of \(Gm' = 1/R\), which means a compensation for all losses and almost an oscillation condition satisfied for any \(Gm' > 0\).

Furthermore, we will assume through our analysis that both \(Gm\) and \(Gm'\) are a function of the same bias current \((I)\)—which is actually the case in our proposal, as it will be shown in Section IV—and that \(A = Gm/Gm'\) is the proportionality ratio between them. The following analysis provides insights on the optimum setting of \(A\). The left and right terms of (9) are plotted in Fig. 5 versus \(Gm\), to ease analysis, and because \(Gm(I)\) is the main design parameter directly linked to the bias current \((I)\).

For \(0 < Gm' < 1/R\), i.e., \(0 < Gm < A/R\) (see Fig. 5), the new factor in (9) is smaller than \((1/R)\), which helps to shift the oscillation condition downward to lower \(Gm\) values, and thus lower power consumption compared to a simple two-stage oscillator.

For the region where \(Gm' > 1/R\), i.e., \(Gm > A/R\), and depending on \(A\) and \(1/R\) levels (Fig. 5), the \(Gm(I)\) increase with the bias current may be compensated by the \((Gm')(I) - 1/R\) increase with the same bias current, in order to keep the oscillation condition (9) true over an extremely wide range of bias current.

The factor \(A\) represents the ratio between \(Gm\) and \(|Gm' - 1/R| = |Gm/A - 1/R|\) slopes. Its setting should be optimized in order to: 1) obtain the oscillation condition for the smallest possible \(Gm\) in the region where \(Gm < A/R\), and 2) ensure the oscillation to a maximum extent over \(Gm > A/R\). Nevertheless, and as depicted in Fig. 5, these considerations behave in opposite directions versus \(A\), and lead, therefore, to a tradeoff on the optimum setting of \(A\). For \(Gm < A/R\), the oscillation condition is relaxed with decreasing \(A\) values, while it degrades for \(Gm > A/R\) with decreasing \(A\), and is compromised for \(A < 1\). The case where \(A = 1\) is dependent on \(1/R\), and the oscillation condition (9) might not be satisfied for low \(1/R\) levels. Hence, and in order to get a maximum extension for the oscillation condition, the best choice for \(A\) seems to have it reasonably set above 1.

As a conclusion to this section, we have shown that the use of a two-stage ring oscillator with local positive feedback presents
the advantage of making the oscillation condition more easily achievable at lower power consumption levels in comparison with a simple two-stage ring oscillator. In addition, this architecture maintains the small-signal relationship between frequency and $Gm$ exactly the same as that with a two-stage ring oscillator. The assumption of making $Gm$ and $Gm'$ function of the same bias current has the advantage of extending the oscillation condition over a wider bias range.

IV. DCO DESIGN

The block diagram of the designed circuit [see Fig. 6(a)] consists of a two-stage DCO core providing I/Q differential outputs. Differential to single-ended I/Q outputs are obtained through on-chip buffers, which can drive externally 50-Ω loads.

The basic amplifier cell is shown in Fig. 6(b). The $Gm$ core is designed with a simple differential NMOS pair, where the positive feedback loop ($Gm'$) is designed with a cross-coupled PMOS load. Considering the differential structure of the basic amplifier, we get

$$g_{mN} = g_mN/2 \quad \text{and} \quad g_{mP} = g_mP/2,$$

where $g_{mN}$ and $g_{mP}$ are the small signal transconductances of NMOS and PMOS transistors. The $R$-parameter, invoked in the previous paragraph, models the losses represented by $gdsN$ and $gdsP$, which are the NMOS and PMOS drain–source transconductances, in addition to the resistive parasitics due to interconnects.

A programmable tail resistors network [see Fig. 6(c)] provides the bias current, which is common for both $Gm$ and $Gm'$ cores. This satisfies the assumption made in the previous section. The tail resistor is chosen here to be digitally programmable with 3 bits for the sake of simplicity. In order to extract the small-signal relationship between the oscillation frequency and the tail resistor $R_{tail}$, we can write around $I = I_{tail}/2$

$$V_{gsN}(I) + V_{gsP}(I) + 2 \cdot R_{tail} \cdot I = V_{dd}.$$  \hspace{1cm} (11)

By developing this equation with respect to $g_{mN}$, and considering $A = (g_{mN}/g_{mP}) = (\beta_N/\beta_P)^{1/2}$, $g_{mN} = \beta_N \cdot V_{gsN} - V_{tN}$, $g_{mP} = \beta_P \cdot V_{gsP} - V_{tp}$, and $V_0 = V_{dd} - V_{tN} - V_{tp}$, we get a second-order equation

$$g_{mN}^2 + \frac{(1 + A)}{R_{tail}} \cdot g_{mN} - \frac{V_0 \beta_N}{R_{tail}} = 0 \hspace{1cm} (12)$$

for which a solution can be given as

$$g_{mN} = \frac{2 \beta_N V_0}{(1 + A)} \cdot \frac{1}{\left(1 + \sqrt{1 + \frac{4 \beta_N V_0}{(1 + A)^2} R_{tail}}\right)}.$$ \hspace{1cm} (13)

As a result, the oscillation frequency behaves as function of $1/\sqrt{R_{tail}}$. In order to get a linear programmable oscillation frequency from (10) and (13) versus an applied tuning code, $R_{tail}$ has been designed as a second-order polynomial expression as

$$\frac{1}{R_{tail}} = \frac{1}{R_1} + \frac{\text{Tuning Code}}{R_0}$$

$$= \frac{1}{R_1} + \frac{1}{R_0} \cdot \left( C_0 + 2 \cdot C_1 + 6 \cdot C_2 + C_0 \cdot C_1 + 2 \cdot C_0 \cdot C_2 + 6 \cdot C_1 \cdot C_2 \right) \hspace{1cm} (14)$$

where $R_1$ and $R_0$ are resistors determining the highest network value (i.e., the lowest frequency) and the frequency tuning slope, respectively, and $C_n$ are the tail network digital commands [see Fig. 6(c)].

By making frequency programmability achievable via the tail resistor only, and by avoiding the use of traditional techniques based on adding tunable extra loads [9], [10], [18] on top of differential pairs, the capacitive parasitics due to transistors and connections are considerably reduced, which favors a higher oscillation frequency and a larger tuning range.

The DCO differential signals are ac coupled and then driven throughout a current-mode logic (CML) buffers path, as shown in Fig. 6(d). The input common-mode level ($V_{dd}/2$) is set...
through a resistive bridge from \textit{Vdd} to \textit{Gnd}. The second CML buffer drives one internal 50-\textOmega resistor load, and a second 50-\textOmega load is connected externally. The buffers biasing is done with the \textit{R}_{in} impedance of their tail NMOS switches.

The simulated average transient supply current of the DCO core shows a quadratic behavior of the total current versus the digital tuning code (Fig. 7), which allows to further reduce the oscillator current consumption for low UWB frequencies. The oscillator core has a maximum current consumption of 3.2, 3.7, and 4.9 mA at \textit{V}_{supply} = 1.2, 1.3, and 1.5 V, respectively. The first buffer consumes 1–1.5 mA, and the second buffer consumes 10–11 mA. High current is needed in the last buffer to overcome the 3-dB power loss into the internal 50-\textOmega load, and provide relatively high output signal levels.

Although phase noise is not specified for IR-UWB, and in order to point-out the potential of the proposed implementation, it was important to avoid sacrificing the phase noise performance while achieving the other main design targets. Examples in [14]–[17] proved the ability to achieve relatively low noise with a high tuning range for low oscillation frequencies (around 1 GHz). At these frequencies, extra MOS devices, for extended frequency tuning or feedback paths can be added, to a certain limit, without a noticeable increase in losses and phase noise degradation. With increased oscillation frequency up to 5 or 10 GHz, the \textit{Q} factor of the MOS capacitances drops with frequency, and therefore, increases losses and degrades phase noise. The final phase noise degradation versus carrier frequency might be more than 20 dB/decade for a given power consumption. Thus, traditional techniques based on adding extra devices become less suitable at high frequencies for high-tuning/low-noise design; as a result, the need to simplify as much as possible the basic amplifier cell, combined with different techniques to achieve tunability (current), becomes the determining factor to attain low-noise performance, and this was the strategy used in our design.

Furthermore, by referring to the Hajimiri’s phase noise theory on differential ring oscillators [9], the single-sideband noise in the 1/f² region is directly proportional to the number of stages \(N\), which is the most favorable in our case \((N = 2)\), while the 30-dB/decade corner frequency \(f_{1/f^2}\) is inversely proportional to \(N\), which makes \(f_{1/f^2}\) higher when \(N\) is minimized. In our design, simulations showed a \(f_{1/f^2}\) corner around 1-MHz offset from the carrier, where the major noise contributors are mainly due to the up-converted 1/f-noise of the active components with small NMOS and PMOS transistors needed to push upwards the maximum oscillation frequency.

The advantage of using a negative resistance with lower global \textit{gm’s} to get oscillation tends to lower the white-noise contribution \(4kT\cdot \gamma\cdot gm\) of the MOS transistors (where \(\gamma\) is the excess noise factor for short channel devices), and also compensates some of the 1/f-noise \((\sim gm^2/\textit{W} \cdot \textit{L} f)\) increase due to lower transistors size \((\textit{W} \cdot \textit{L})\). In addition, the choice of a tail resistor to provide the bias current helps to minimize the 1/f up-conversion noise due to the bias part, compared to an active current mirror implementation. On the other hand, this tail resistor increases the sensitivity to the common mode supply noise, which may require the use of a top regulator with low-drop-output from the supply to improve the power supply rejection (\textit{not used here}).

V. MEASURED RESULTS

The chip is implemented in a 1-poly 8-metals (1P8M) 0.13 \textmu m CMOS technology from the United Microelectronics Corporation (UMC), Hsinchu, Taiwan. The chip microphotograph is shown in Fig. 8.

As shown in Fig. 9, the measured minimum and maximum oscillation frequencies at 1.3-V supply voltage are 1.82 and 10.18 GHz, respectively, with a 139% tuning range. Fig. 10 provides measured and simulated tuning ranges versus applied tuning code at different supply voltages. These results demonstrate the ability to cover the full UWB spectrum at slightly higher than a 1.3-V supply voltage. At a 1.5-V supply, the maximum oscillation frequency reaches 12.4 GHz with a 142% tuning range. Furthermore, Fig. 10 also shows a linear trend with the programmable oscillation frequency curves versus tuning code, as predicted in the design section.

The phase noise was measured with the Agilent E5052 phase noise measurement equipment. In Fig. 11, the measured free-running oscillator’s phase noise is shown. The phase noise at a 5.65-GHz carrier is \(-88.4\) and \(-121.7\) dBc/Hz at 1- and 10-MHz offsets, respectively. At minimum oscillation frequency (1.82 GHz), the measured phase noise performance is \(-90\) and \(-120.4\) dBc/Hz at 1- and 10-MHz offsets.
VI. COMPARISON WITH THE STATE-OF-THE-ART

The presented solution in this paper is compared to a number of reported ring oscillators in the literature representing the published state-of-the-art performances (Table I and Fig. 12). We use for those two figures of merit (FOMs). The first one uses a power-frequency-normalized FOM, as defined in [5]. In order to take the oscillator’s tuning range into account, a second power-frequency-tuning-normalized FOM, equivalent to the proposed definition in [19], is employed as follows:

\[
\text{FOM} = 10 \log \left( \left( \frac{F_{\text{osc}}}{F_m} \right)^2 \frac{1}{P_{\text{(min)}}} \right) - L\{F_m\} \tag{15}
\]

\[
\text{FOM}_{\text{TR}} = 10 \log \left( \left( \frac{F_{\text{max}} - F_{\text{min}}}{F_m} \right)^2 \frac{1}{P_{\text{(max)}}} \right) - L\{F_m\} \tag{16}
\]

where \( L \) is the phase noise, \( F_m \) is the frequency offset from the carrier, \( F_{\text{osc}} \), \( F_{\text{max}} \) and \( F_{\text{min}} \) are the maximum and minimum oscillation frequencies, respectively, and \( P \) is the total dissipated power.

A category-by-category comparison of the measured phase noise performance with the state-of-the-art yields the following conclusions.

- Although the oscillator is not locked, the measured phase noise at 5.65-GHz carrier and 1-MHz (Fig. 11) offset is equivalent to the reported performance in [3] and [4], at almost the same conditions, but with higher tuning range and much lower power.
- In [5], the measured phase noise is about \(-94 \text{ dBc/Hz}\) at \( 2\)-MHz offset and 11.5-GHz carrier, which yields around \(-88 \text{ dBc/Hz}\) at 1-MHz offset (assuming a \(-20\text{-dB/dec}\) slope), and this is equivalent to our measured value at half the carrier, but with much higher tuning range and lower power in our case. The same conclusions are valid for [6].
- In [9] and [18], the reported phase noise at 1-MHz offset and at almost the same carrier (\( \sim 5.5 \text{ GHz} \)) is better than our measured performance (\(-98.5 \text{ and } -99.5 \text{ dBc/Hz}\), respectively). This comparison might be unfair since our oscillator is measured unlocked, and presents carrier instability up to 4-MHz offset. If we compare the phase noise results at the same carrier, but at let us say, 10-MHz offset (assuming a \(-20\text{-dB/dec}\) slope), we see that the performances among these references and our circuit become comparable (\(-118.5 \text{ and } -119.5 \text{ dBc/Hz}\), respectively) (Fig. 13).
TABLE I
RING OSCILLATOR BENCHMARKING

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<th>$L(F_m)$</th>
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<th>$F_{min}$</th>
<th>$F_{max}$</th>
<th>Tuning Range</th>
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<th>FOM</th>
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<td>No</td>
<td>1</td>
<td>BiCMOS</td>
</tr>
<tr>
<td>Finocchiaro [13]</td>
<td>-82</td>
<td>0.1</td>
<td>1.8</td>
<td>1.3</td>
<td>2.3</td>
<td>56</td>
<td>22.5</td>
<td>153.6</td>
<td>148.5</td>
<td>Yes</td>
<td>2</td>
<td>Si Bipolar</td>
</tr>
<tr>
<td>Yan [14]</td>
<td>-106</td>
<td>0.6</td>
<td>0.9</td>
<td>0.66</td>
<td>1.27</td>
<td>63.2</td>
<td>15.5</td>
<td>157.6</td>
<td>154.2</td>
<td>Yes</td>
<td>2</td>
<td>CMOS 0.5um</td>
</tr>
<tr>
<td>Park [15]</td>
<td>-117</td>
<td>0.6</td>
<td>0.9</td>
<td>0.75</td>
<td>1.2</td>
<td>46.2</td>
<td>30</td>
<td>165.8</td>
<td>159.7</td>
<td>Yes</td>
<td>4</td>
<td>CMOS 0.6um</td>
</tr>
<tr>
<td>Jeong [16]</td>
<td>-79</td>
<td>0.6</td>
<td>1.69</td>
<td>0.25</td>
<td>1.69</td>
<td>148.5</td>
<td>96</td>
<td>128.2</td>
<td>126.8</td>
<td>Yes</td>
<td>4</td>
<td>CMOS 0.8um</td>
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<tr>
<td>Thamsirianan [17]</td>
<td>-99</td>
<td>0.6</td>
<td>0.926</td>
<td>0.32</td>
<td>0.926</td>
<td>97.3</td>
<td>7.4</td>
<td>154.1</td>
<td>150.4</td>
<td>No</td>
<td>3</td>
<td>CMOS 1.2um</td>
</tr>
<tr>
<td>Eken [18]</td>
<td>-99.5</td>
<td>1</td>
<td>5.79</td>
<td>5.16</td>
<td>5.93</td>
<td>14</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>No</td>
<td>3</td>
<td>CMOS18</td>
</tr>
</tbody>
</table>

(1) Free-running oscillator.
(2) Assuming a locked oscillator, and 20dB/decade phase noise slope from 1MHz to 10MHz.
(3) Estimated power consumption for the oscillator core alone.

![Fig. 12](image)

Fig. 12. FOM comparison with state-of-the-art ring oscillators, placed in categories as: (A) high frequency (up to 10 GHz), high tuning range ($\geq 100\%$). (B) High frequency (10 GHz), low tuning range. (C) Very high frequency (20 GHz), mid tuning range. (D): Mid frequency (5 GHz), mid/low tuning range. (E) Low frequency ($< 2$ GHz), mid/low tuning range. (F) Low frequency, high-tuning range.

- Oscillators in [14]–[17] (mainly [15]) offer low phase noise figures. However, and as we have explained in Section IV, the phase noise comparison among these oscillators and the one we propose cannot be directly made, due to the difference in carrier frequencies, and to the capacitances $Q$-factor drop and losses increase in frequency, leading to more than 20-dB/decade phase noise degradation versus carrier frequency, and making the FOM definitions (15) and (16) more penalizing for high-frequency than low-frequency oscillators. However, even if we extrapolate the best phase noise result [15] with a 20-dB/decade law from a 600-kHz offset and 900-MHz carrier, toward a 10-MHz offset and 5.5-GHz carrier, we get $-125.7$ dBc/Hz, which is 4 dB better than our result, at the same carrier and offset frequencies, at the cost of three times less tuning range, and six times more power.

![Fig. 13](image)

Fig. 13. Measured and extrapolated phase noise from state-of-the-art results, at 10-MHz offset, versus carrier frequency (assuming a 20-dB/decade slope).
the-art solutions. Now, if we look at the phase noise performance at 10-MHz offset, with the assumption of a 20-dB/decade slope between 1- and 10-MHz offsets (locked oscillator), the calculated FOM (second line of Table I) is 4 dB above the best published state-of-the-art performance [15]. The real phase noise performance should be somewhere in between those two results due to the 30-dB/decade slope, which may have its corner frequency above 1-MHz offset (see also Fig. 12, △).

FOM_{TR} calculations, based on the proposed definition in (16), achieve a state-of-the-art and record result, with either 1- or 10-MHz offsets measured phase noise results (Table I and Fig. 12, □).

VII. CONCLUSION

In this paper, we have presented the design of a two-stage quadrature ring oscillator using the concept of local positive feedback. The oscillator features an ultra-wide tuning range of 139%, with a low power consumption level (< 5 mW), which is key for building state-of-the-art low-power IR-UWB applications.

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REFERENCES


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