First-order Continuous-time Sigma-delta Modulator

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Abstract

This paper presents the design of a first-order continuous-time sigma-delta modulator. It can accept input signal bandwidth of 10 kHz with oversampling ratio of 250. The modulator operates at 1.8 V supply voltage and uses 0.18 um CMOS technology. It achieves a level of 60 dB SNR.

1. Introduction

With the fast development of the CMOS technology, the analog-to-digital converters (ADCs) go to the trend of high-resolution, wide bandwidth and low-power applications. Sigma-delta (Oversampling) analog-to-digital converter has been playing an important role and gaining more popularity in these areas. Based on the oversampling method, it uses high-frequency modulation and thus eliminates the need for abrupt cutoffs in the analog anti-aliasing filters at the input to the ADCs. Compared with other ADCs, the analog circuitry of the sigma-delta ADC is simpler and easier to be realized [1-3].

The sigma-delta modulator is the key part of the sigma-delta ADC. It samples the input analog signal with a much higher frequency than the bandwidth of the input signal, then it shapes the noise into high frequency end and lets the signal pass through. The sigma-delta modulator has two typical architectures – switched-capacitor (SC) and continuous-time (CT). Although SC modulators exhibit good accuracy and linearity, CT modulators can achieve much broader bandwidths with simple analog circuitry [4-5].

The sigma-delta modulator is based on oversampling and implements the concept of noise shaping. Oversampling reduces the quantization noise power in the signal band by spreading the fixed quantization noise power over a bandwidth much larger than the signal band. Noise shaping further attenuates this noise in the signal band and amplifies it outside the signal band. Figure 1 shows a simplified “S-domain” model of first order sigma delta modulator, which illustrates the principle of noise shaping.

Based on Figure 1, when noise $N(S) = 0$, the signal transfer function (STF) will be:

$$\frac{Y(S)}{X(S)} = \frac{1}{1 + \frac{1}{S}} = \frac{1}{1 + S}$$

which is actually a lowpass filter. The signal remains unchanged as long as its frequency content doesn’t exceed the filter’s cutoff frequency. Similarly, when the input signal $X(S) = 0$, the noise transfer function (NTF) will be:

$$\frac{Y(S)}{N(S)} = \frac{1}{1 + \frac{1}{S}} = \frac{S}{1 + S}$$

which behaves as a highpass filter, indicating that the noise has been pushed into a higher frequency band. To summarize, this process of noise shaping by the sigma-delta modulator can be viewed as pushing quantization noise power from the signal band to higher frequencies. In this paper we present the design and implement of a first-order sigma-delta modulator with TSMC 0.18um technology.

2. System level design and simulation

Figure 2 shows a system level block diagram of a continuous time sigma-delta modulator.
The continuous time sigma-delta modulator needs a continuous time loop filter with transfer function (for the first order loop filter):

\[ H(S) = \frac{b0}{S + a0}. \]

It can be realized by using the block diagram as Figure 3 shown.

Thus, the system level design for the sigma-delta modulator is focus on designing loop filter or finding the suitable noise transfer function (NTF) for the corresponding system to achieve the required signal-to-noise ratio (or dynamic range). It usually requires a large amount of calculation and application in the program (C or Matlab). To minimize the program working load and speed up the design step, this project implements the delta sigma toolbox [6-7].

The first step in the design of a sigma delta modulator is the selection of the NTF. To use the delta sigma toolbox, the loop filter structure can be represented in Figure 4.

Afterwards, a discrete-time Z-domain to continuous-time S-domain transformation should be done in order to implement a continuous-time sigma-delta modulator [9]. Two common transformations can be considered: bilinear transformation and impulse-invariant-transformation. For design simplicity, the impulse-invariant-transformation is chosen. The delta sigma toolbox also provides the tools to transform between z-domain and s-domain.

Figure 5 shows the simulation result of the designed first order sigma-delta modulator. The input sine wave is 10K Hz bandwidth. The output signal is a pulse density wave. Figure 6 shows the signal to noise ratio (SNR).

The block diagram of a first order continuous time sigma delta modulator is shown in Figure 7, which consists of an integrator, a comparator plus a DFF functioning as a one-bit ADC, and a one-bit DAC placed in the feedback loop.
The integrator consists of an op-amp, a resistor, and a feedback capacitor. The values of the resistor and the capacitor decide the time constant of the integrator. The time constant shouldn’t be too big. Otherwise, the integrator will go into the saturation status. Op-amp is the core part of the sigma-delta modulator. It provides a large open loop gain to implement the negative feedback concept as well as let the integrator integrate smoothly. In addition, it has large bandwidth to pass through at least the first two harmonics of input sine wave. In an affect to achieve better stability, the designed op-amp also has large phase margin. Figure 8 shows the structure of the implemented op-amp [8].

The feedback capacitor P3 introduces a dominant pole to expand the unit gain bandwidth while it decreases the DC gain. By carefully sizing the feedback capacitor P3, the op-amp achieved 20 MHz unit gain bandwidth, 70 dB DC gain with a phase margin of 70 degree (Figure 9).

P4 and P5 act as current source as well as voltage divider. N2 and N3 form current mirror to provide stable current for the first stage differential inputs. P0, P1, N0 and N1 are composed of differential amplifier. P2 and N4 form the second stage to amplify the signal from the first stage. Since in sigma-delta modulators the comparator is required to work at a high oversampling frequency but its resolution can be as small as 1 bit, the comparator design thus focuses more on a high-speed operation instead of
accuracy. Figure 11 shows the propagation delay of the comparator.

![Figure 11. The propagation delay of the comparator](image)

The clock frequency of the D Flip flop decides the sampling rate. Since the project requires the oversampling ratio (OSR) of 250, the D flip flop will operate at 5 MHz.

This 1-bit DAC logic is easily to be realized by a simple multiplexer circuit. The operation of this multiplexer is to select +VREF and -VREF signals depending on the 1-bit digital input signal.

4. Conclusion

The circuit design of the first order continuous time sigma delta modulator goes through the system schematic, two-stage op-amp, integrator, comparator, DFF and DAC. The whole first order sigma delta modulator system works very well under the following conditions:
- Input sine wave frequency up to 10 KHz
- Input sine wave amplitude up to 0.8 V
- Clock frequency (DFF clock) 5 MHz

The output signal of the modulator is a pulse density waveform, which uses the pulse density to represent the original input sine wave. Figure 12 shows the input signal, integrator output signal and the modulator output signal of the designed continuous time sigma-delta modulator.

![Figure 12. Simulation of the first order continuous-time sigma-delta modulator](image)

5. References