Imperial College London

Separation Logic-Assisted Code Transformations for Efficient High-Level Synthesis

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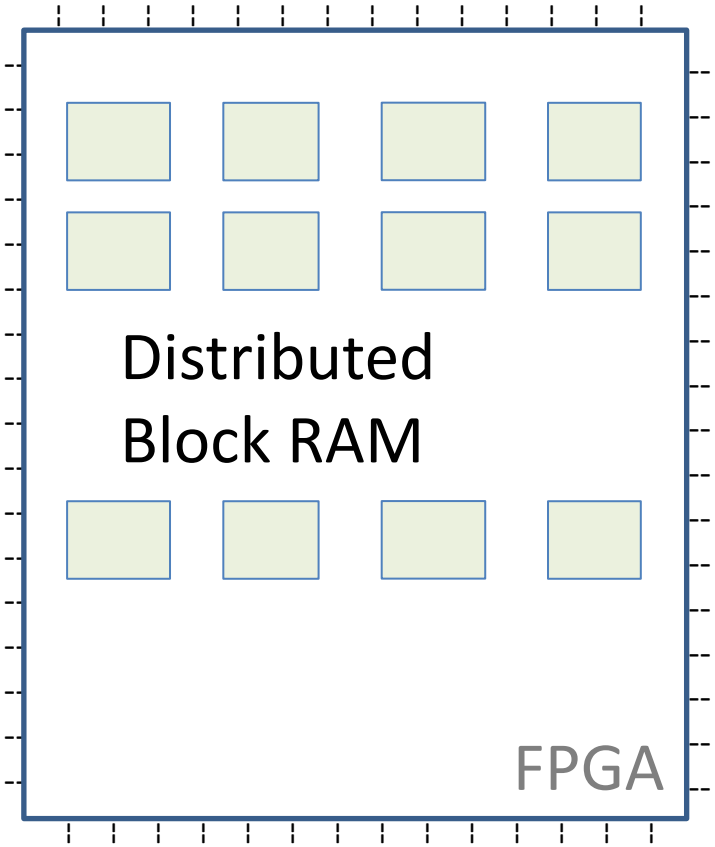
George Constantinides

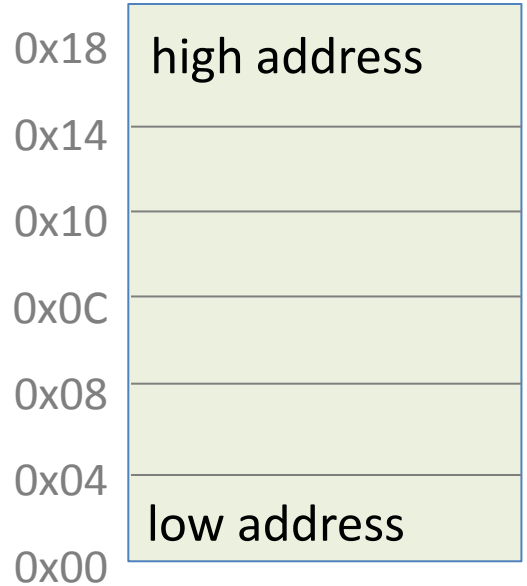
12 May 2014

esa

Background



SW memory model

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int main() {
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  p = new int;
  *p = 3;
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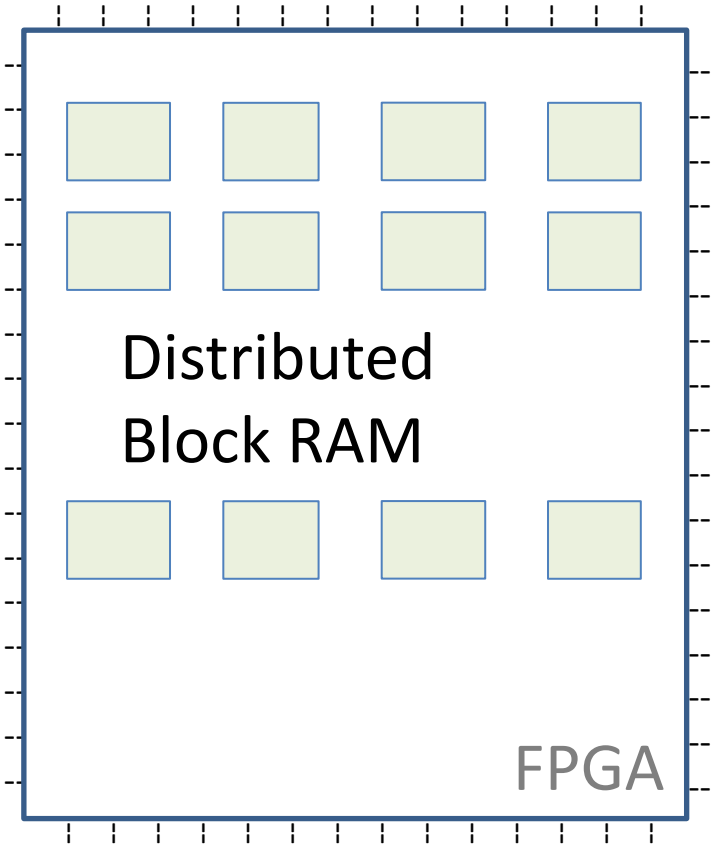

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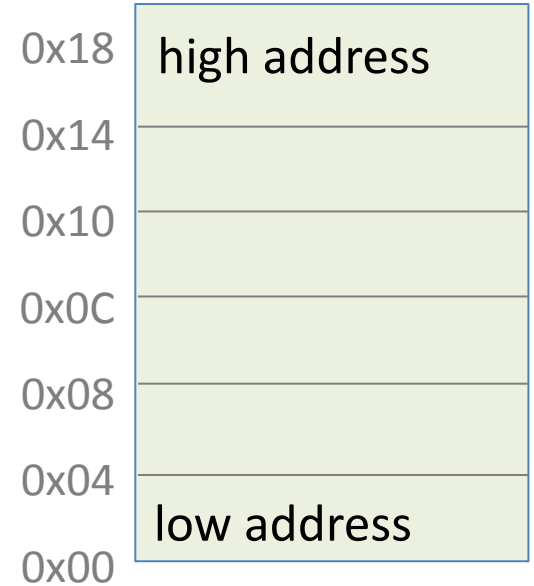


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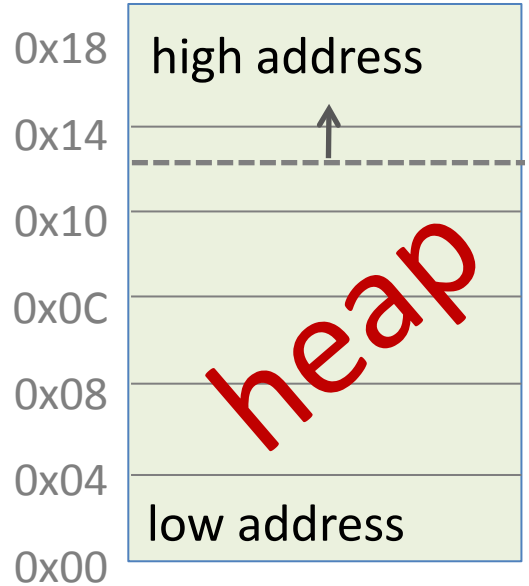
Background

Lack of automated optimizations …

- … for programs using pointers
- … because pointers are difficult to analyze
- … and memory is allocated, disposed, and reused at run-time
- Yet widely used in SW

SW memory model

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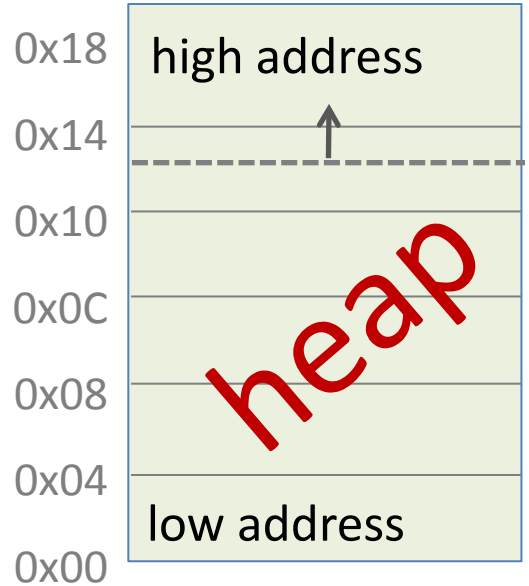
Background

Lack of automated optimizations …

- … for programs using pointers
- … because pointers are difficult to analyze
- … and memory is allocated, disposed, and reused at run-time
- Yet widely used in SW

This work takes a step towards closing this gap

SW memory model

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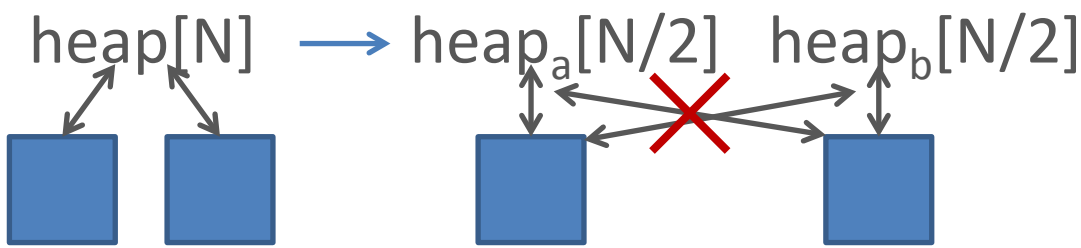
Our contribution

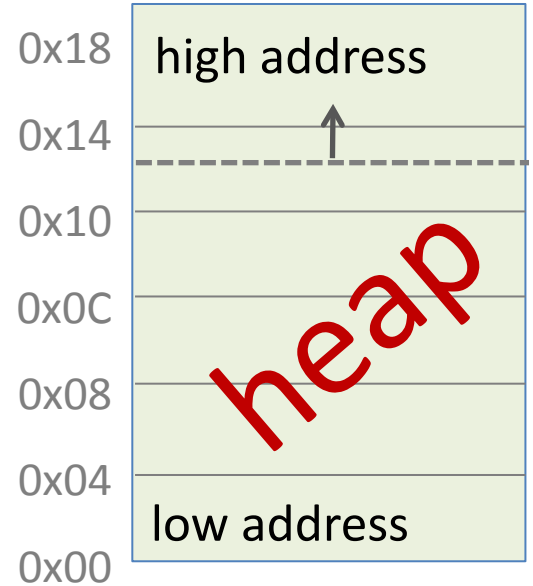
Our goal

- Partition heap-allocated data structures ('heaplets')
- Synthesize parallel memory accesses



- Ensure that heap partitions are 'private'

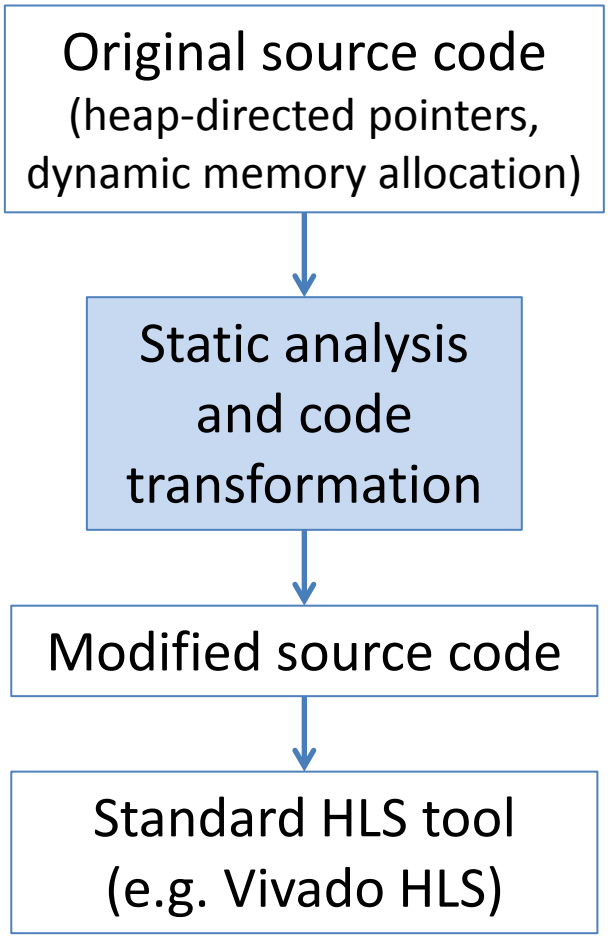
SW memory model



Outline

Executive summary

- Static program analysis
  - Analyse pointer-based memory accesses
  - Identify independent, disjoint regions in memory
- Source-to-source transformations
  - Partition heap across on-chip memory banks
  - Automatic parallelization



Motivating example

Can we parallelize this loop?

```
s = PUSH(root, s);
while s!=0 do
   s = POP(&u, s);
   … do something
   if (u->left!= 0) && (u->right!=0) then
      s = PUSH(u->right, s);
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   end if
   delete u;
end while
```

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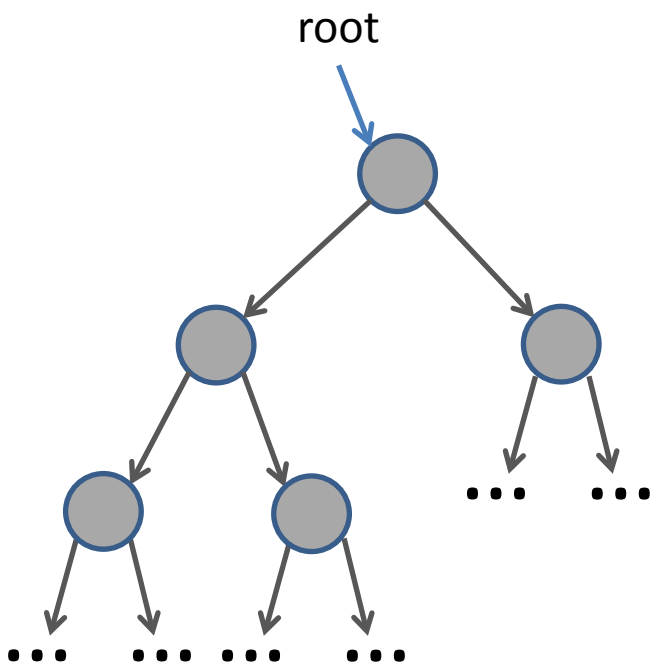


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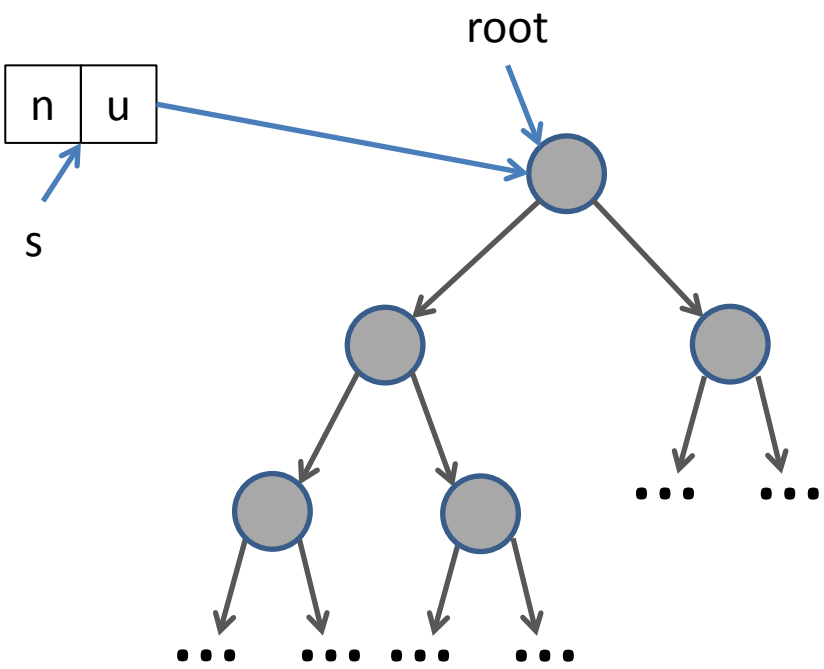


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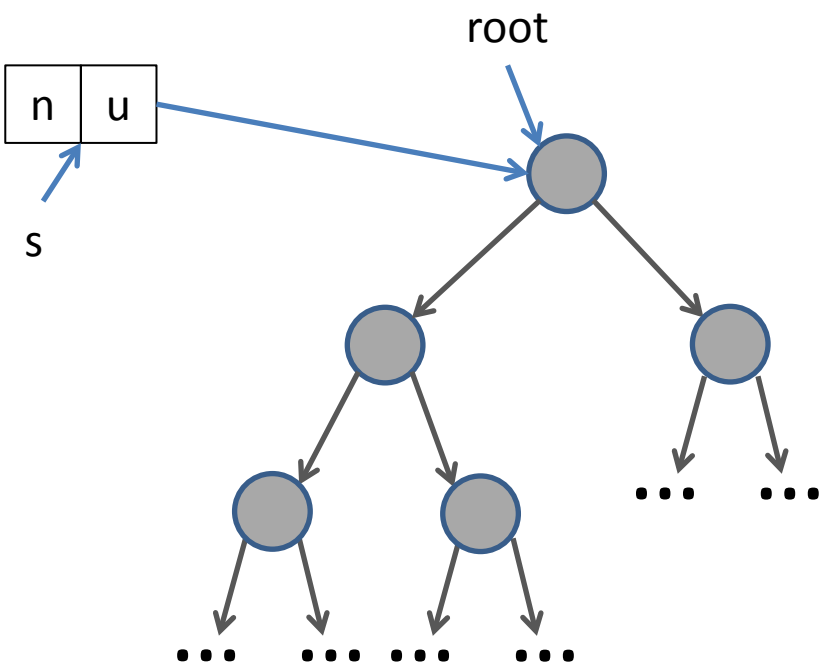


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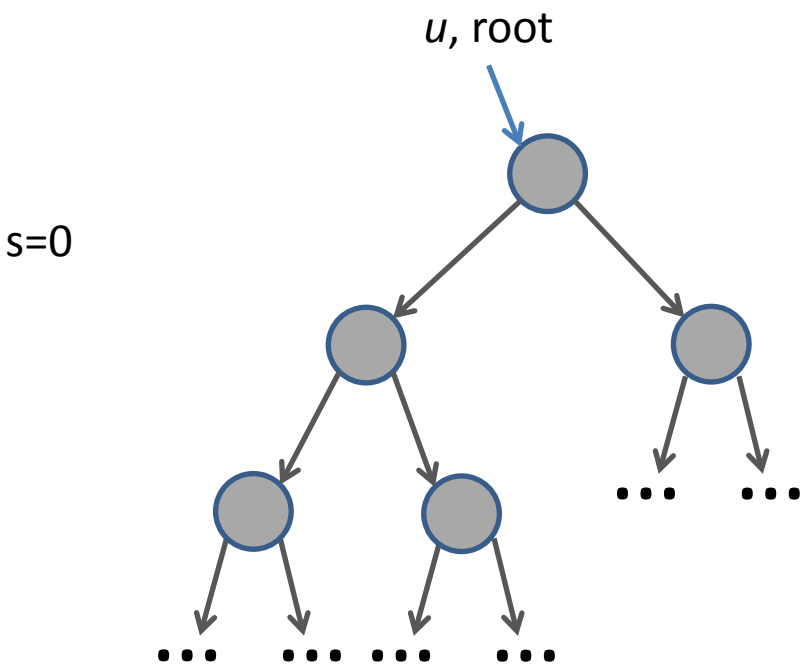


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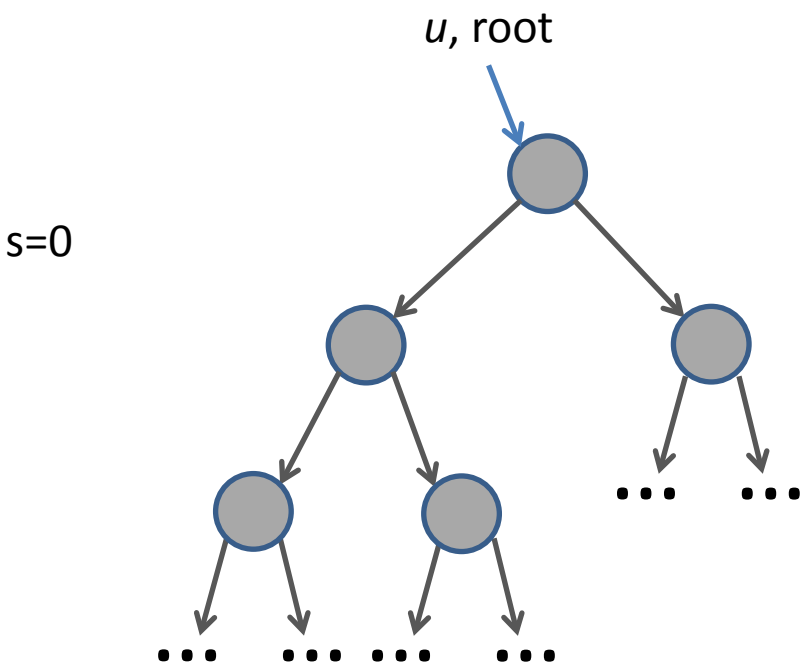


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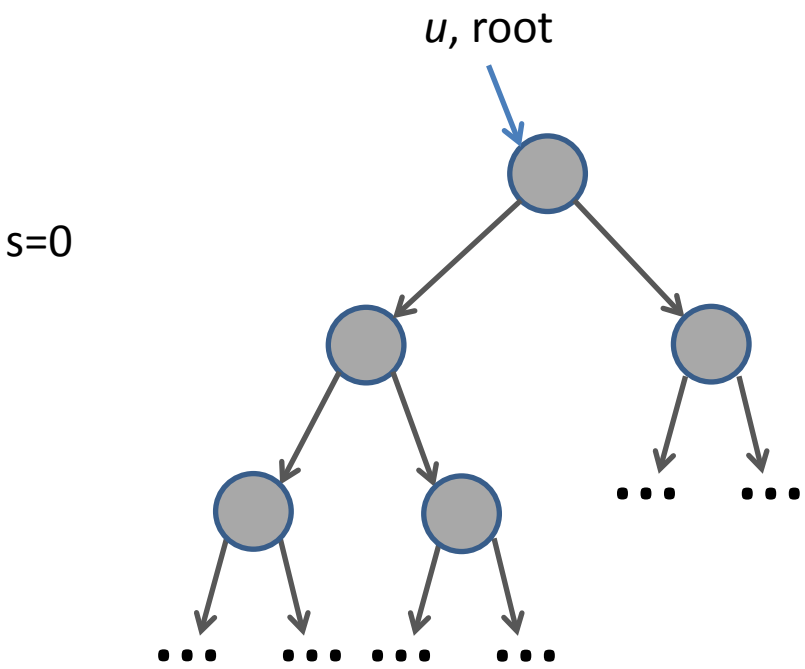


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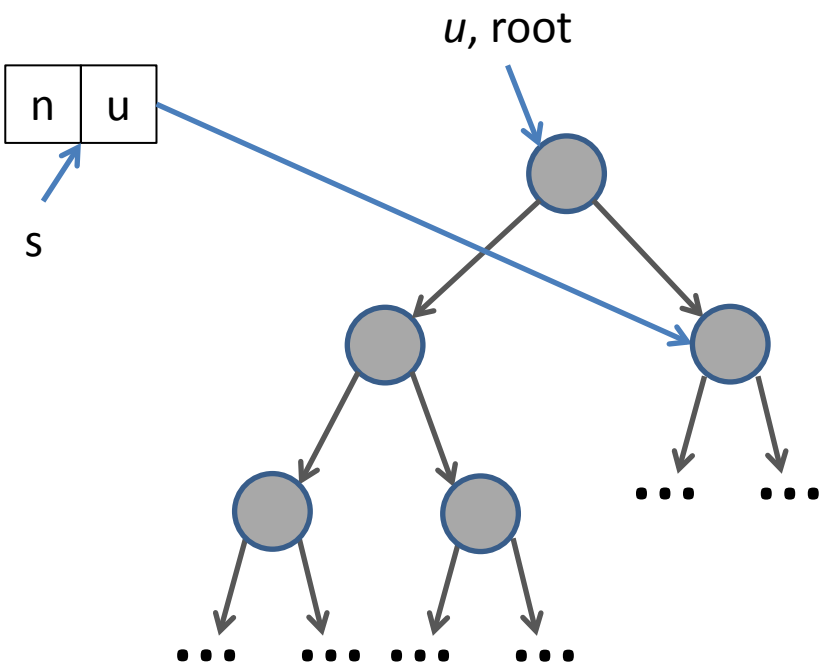


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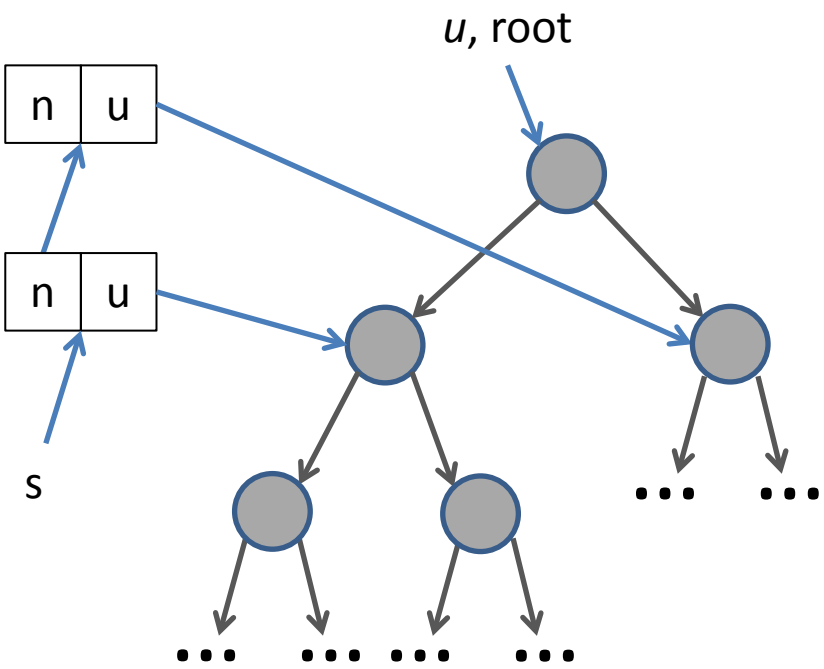


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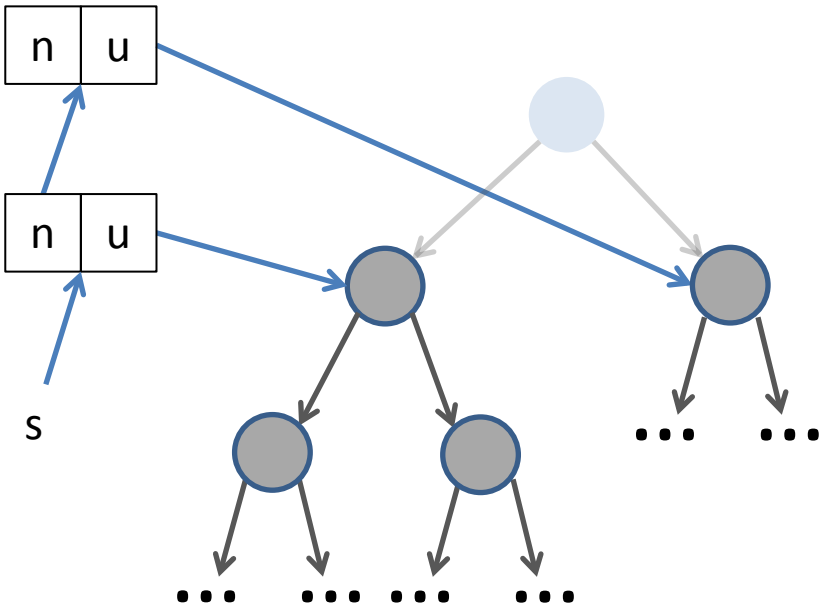


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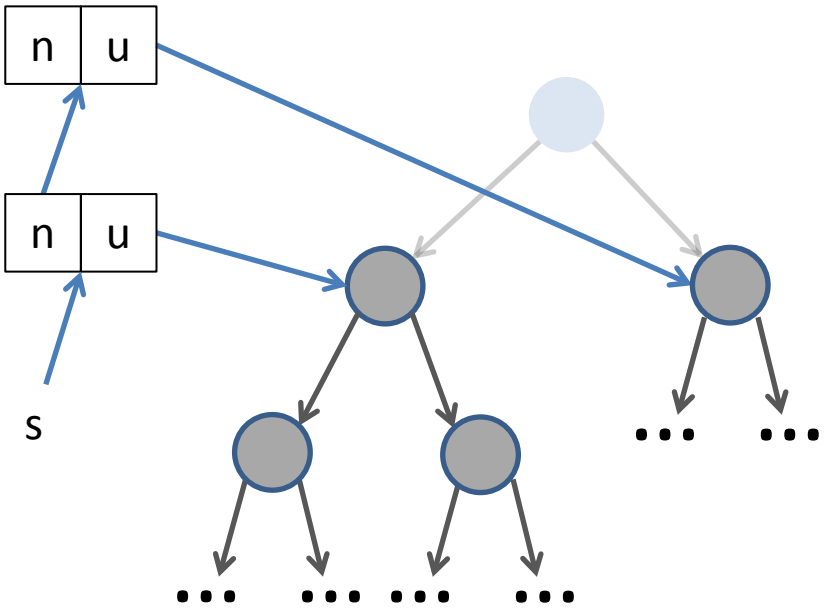


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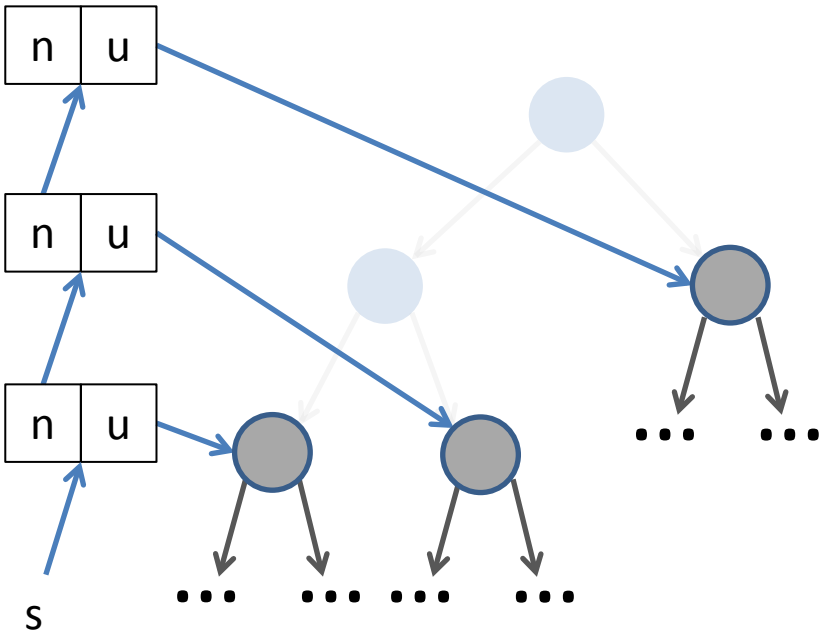
Motivating example

After two iterations…

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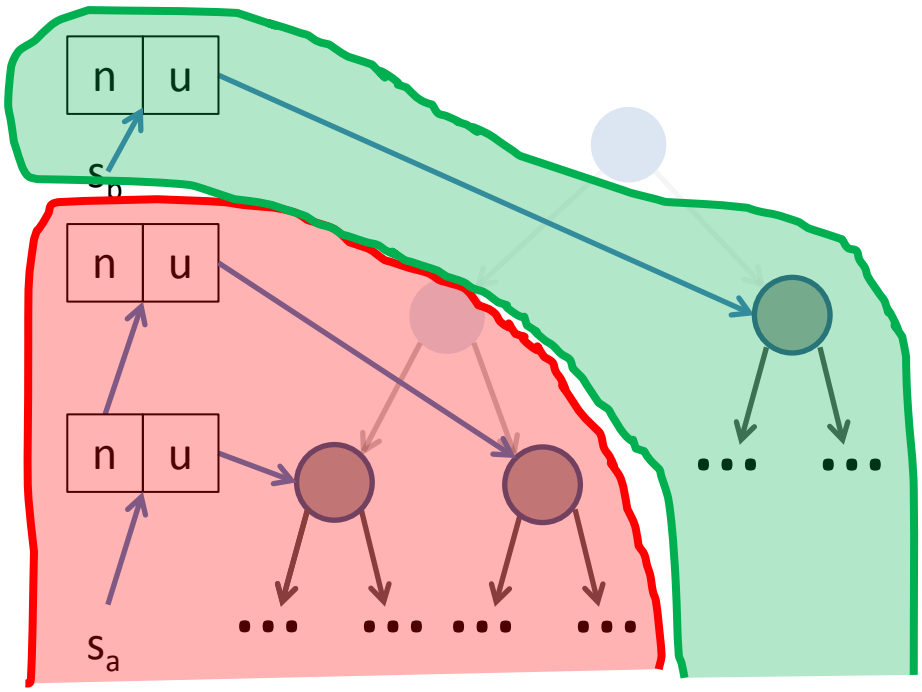


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- Partition linked list and tree

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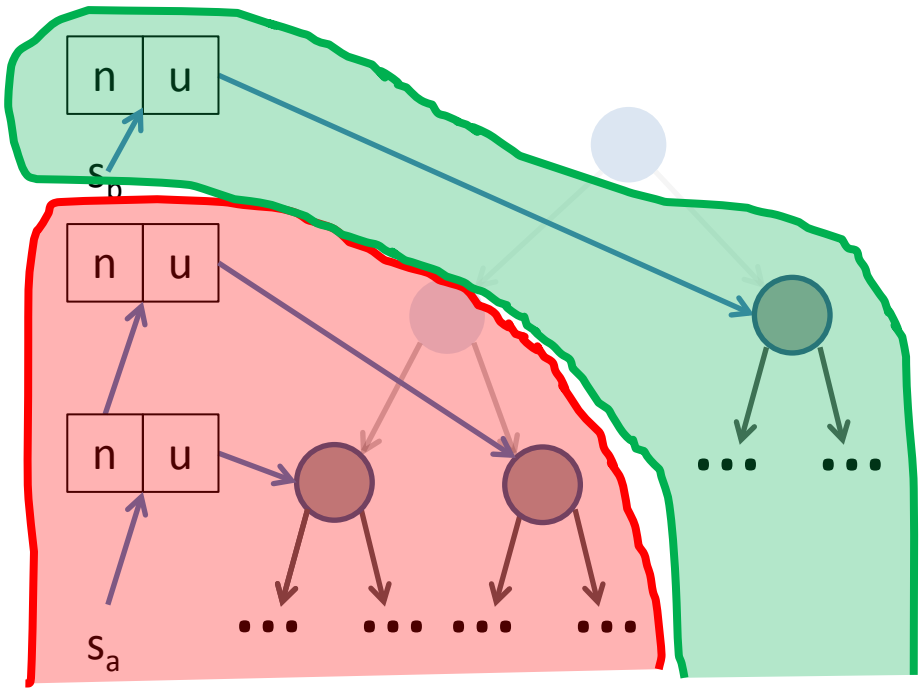

… preamble (accessing root node)

while s_a!=0 **do**
  … loop body (access left sub-tree)
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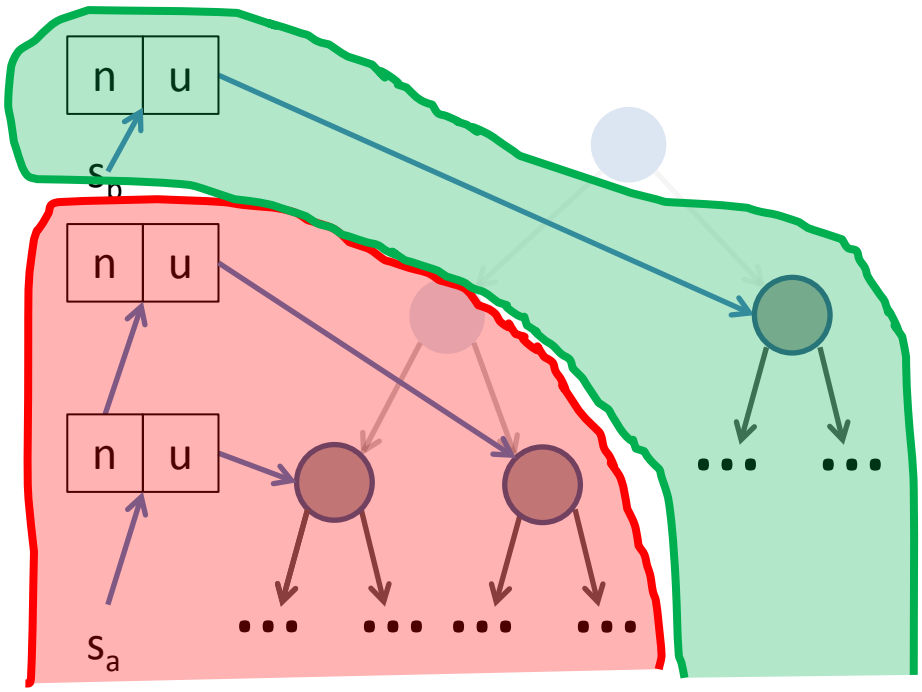

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- Will the red loop ever access data in the green partition?

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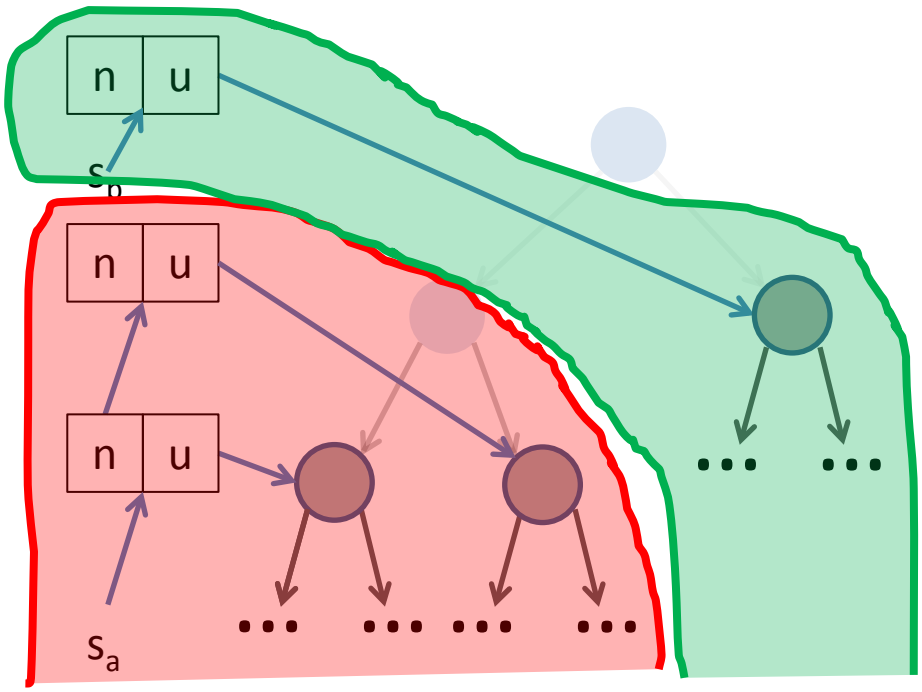

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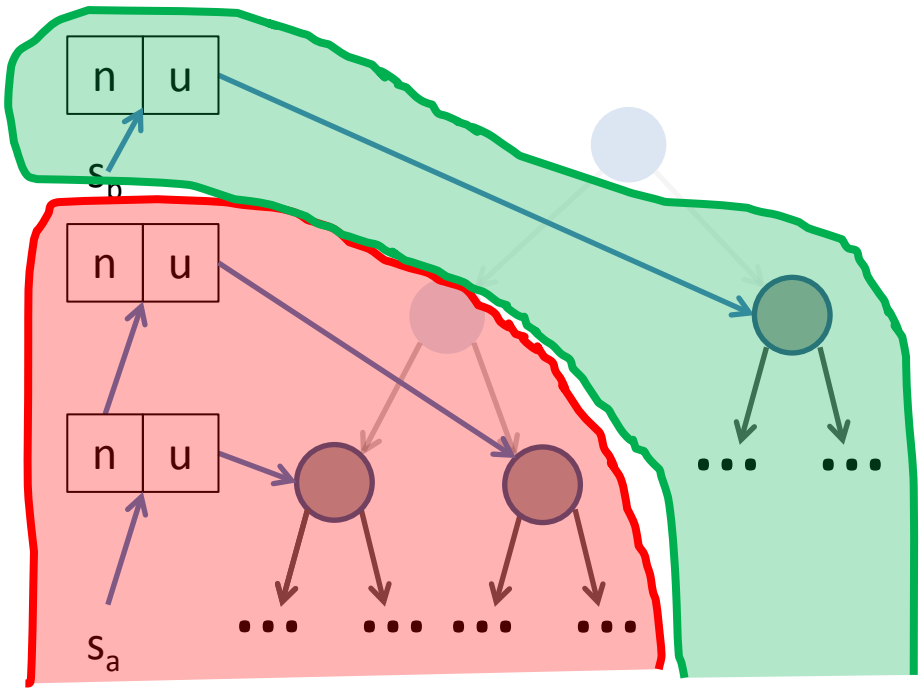

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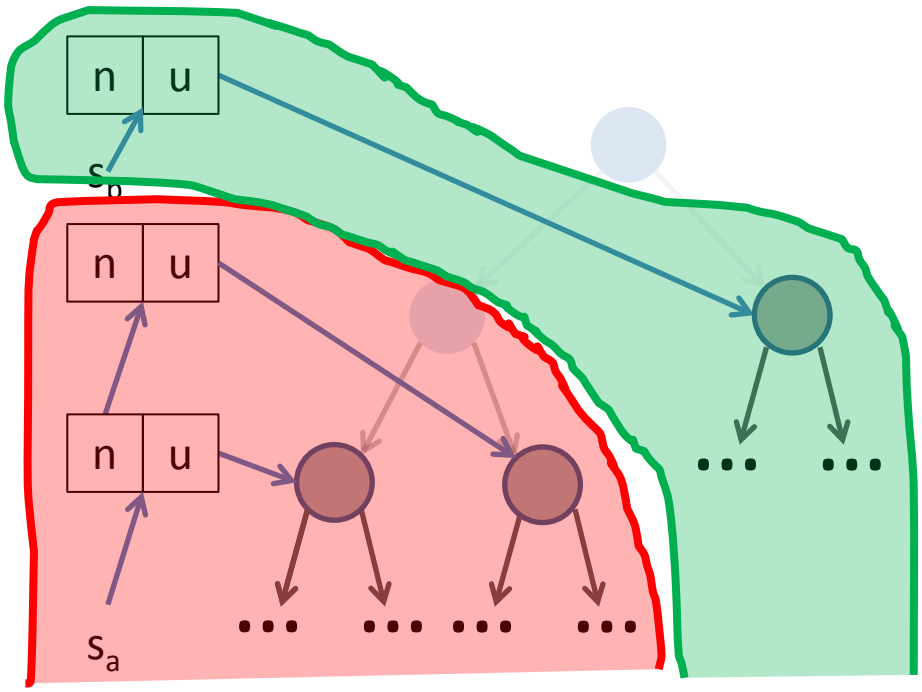

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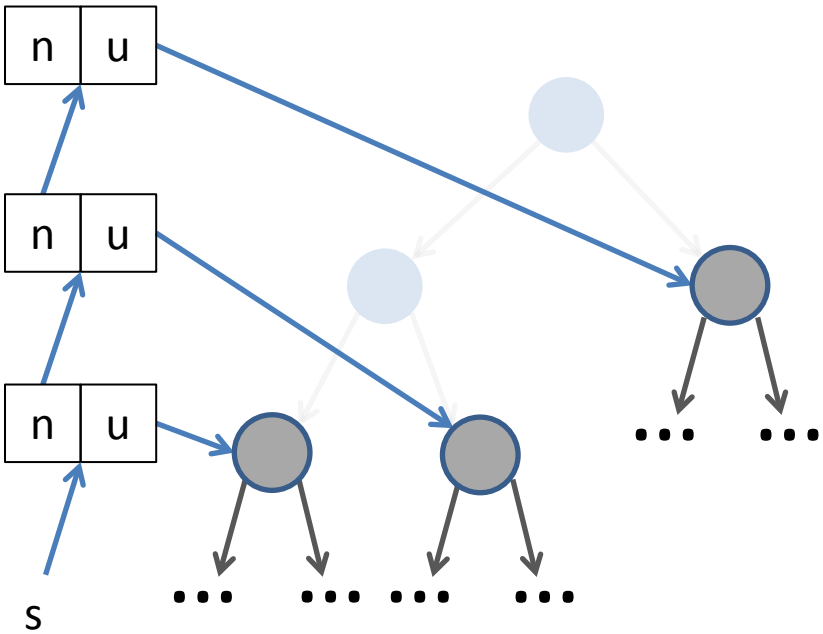
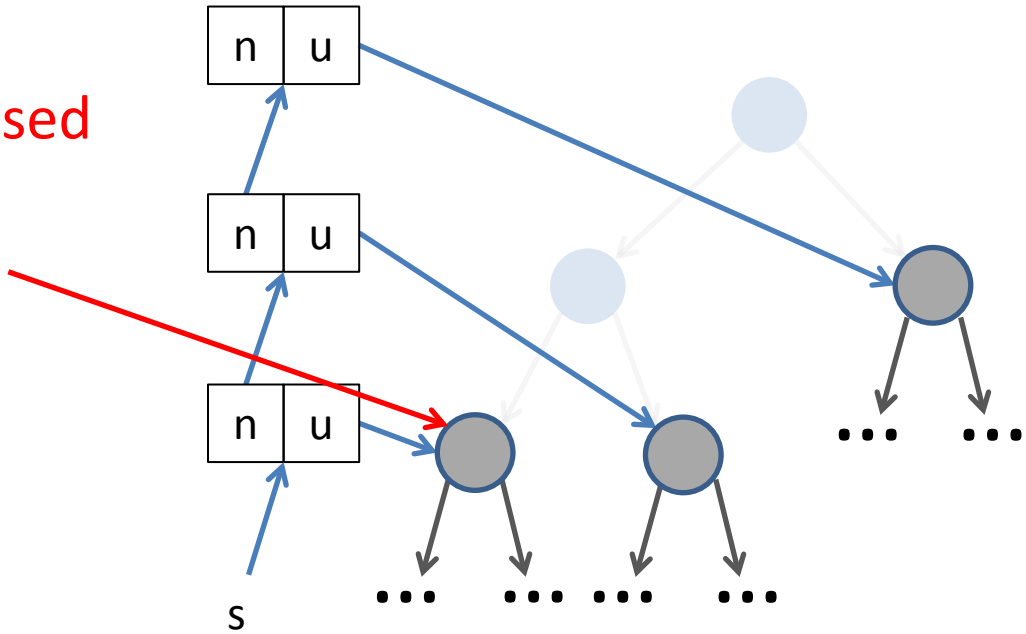
- Partition linked list and tree
- Will the red loop ever access data in the green partition? No!
- Parallelization is legal (does not violate data dependencies)
- Why is it hard for a tool to figure this out?

The problem



The problem

Heap accessed in the next iteration



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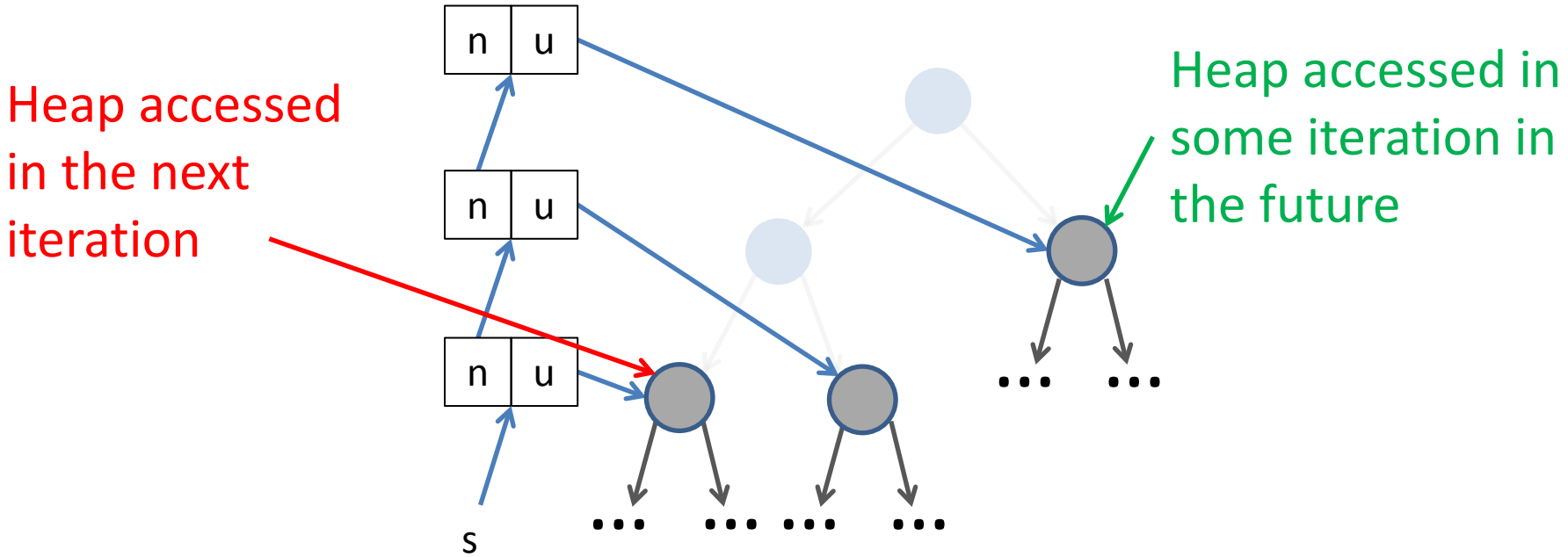
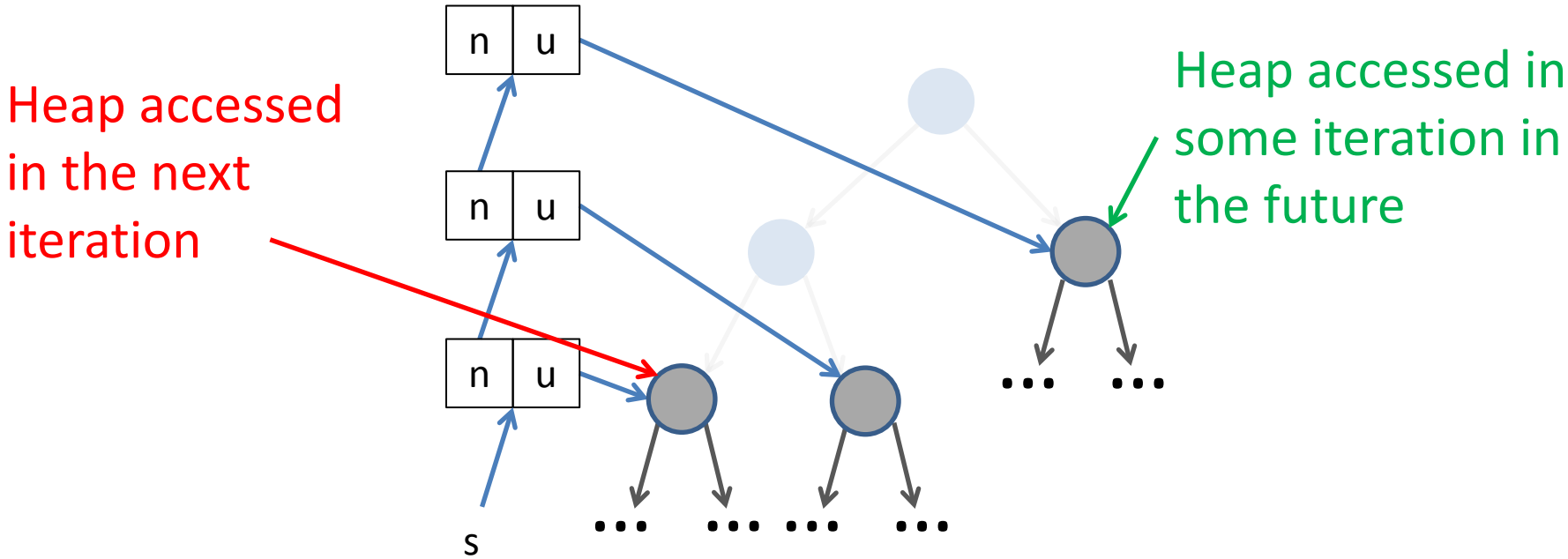

Heap accessed in the next iteration
Heap accessed in some iteration in the future
n
u
n
u
n
u
s

The problem



- Do these iterations access the same memory cell?

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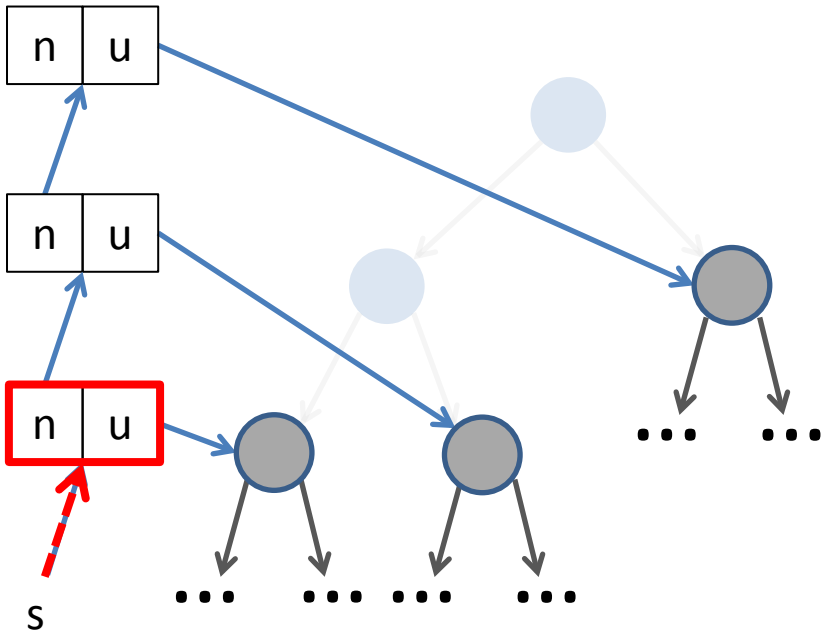

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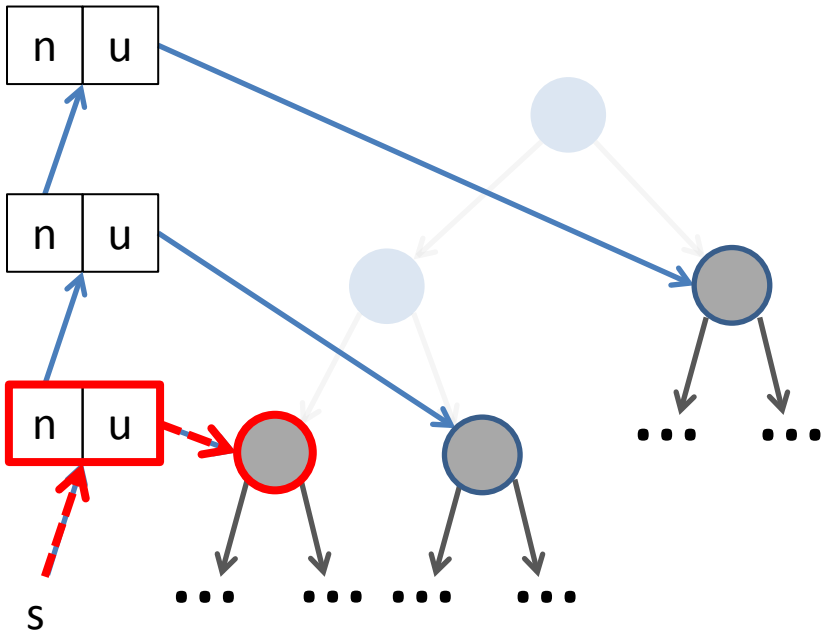
  heap[s]

The problem



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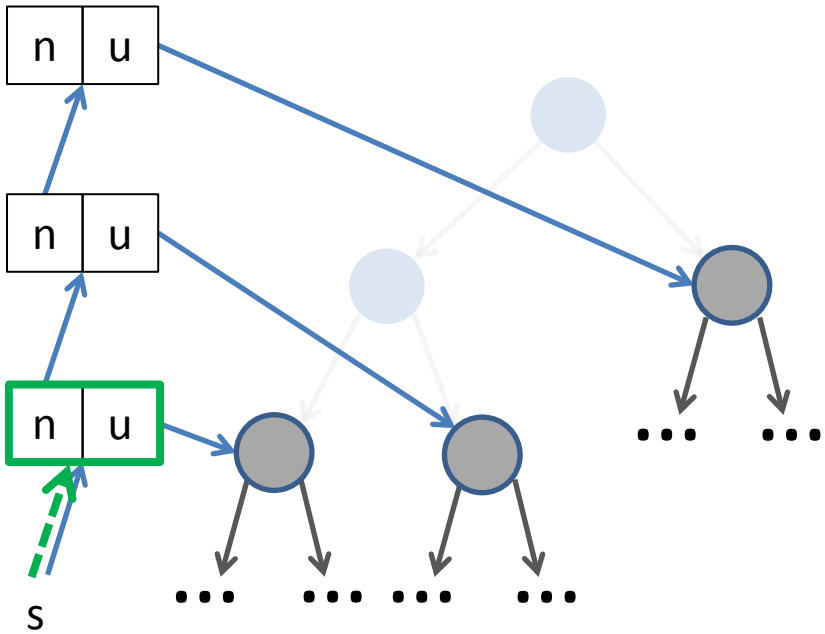
  heap[heap[s].u]

The problem



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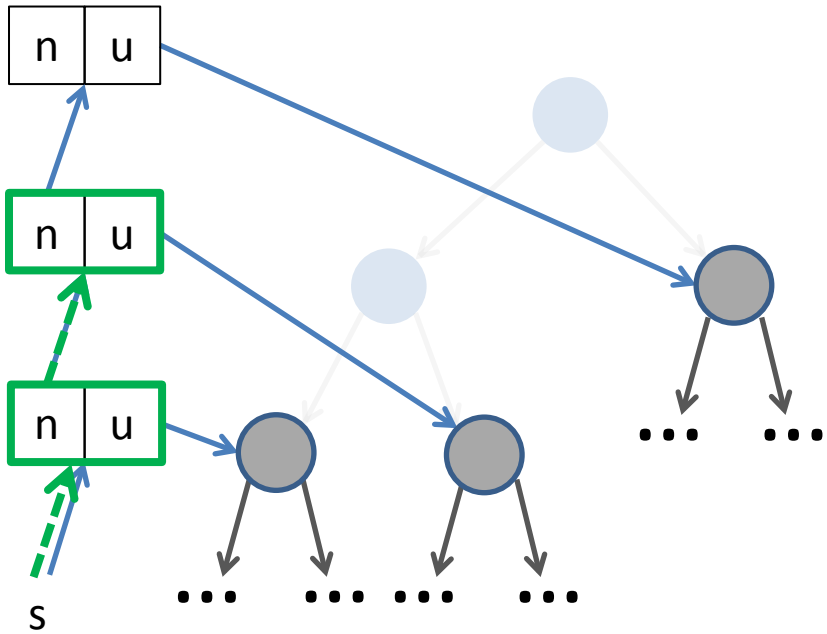
heap[heap[s].u] heap[s]

The problem



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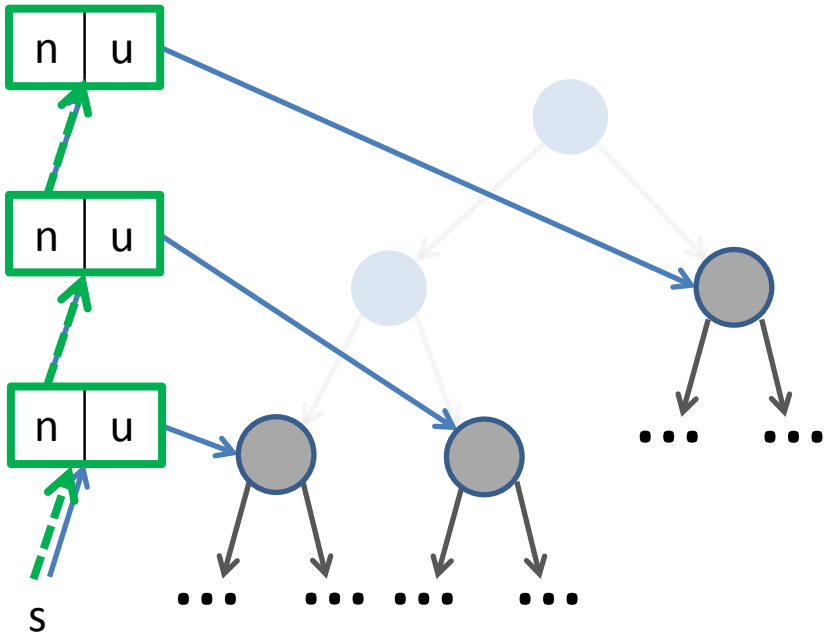
heap[heap[s].u] heap[heap[s].n]

The problem

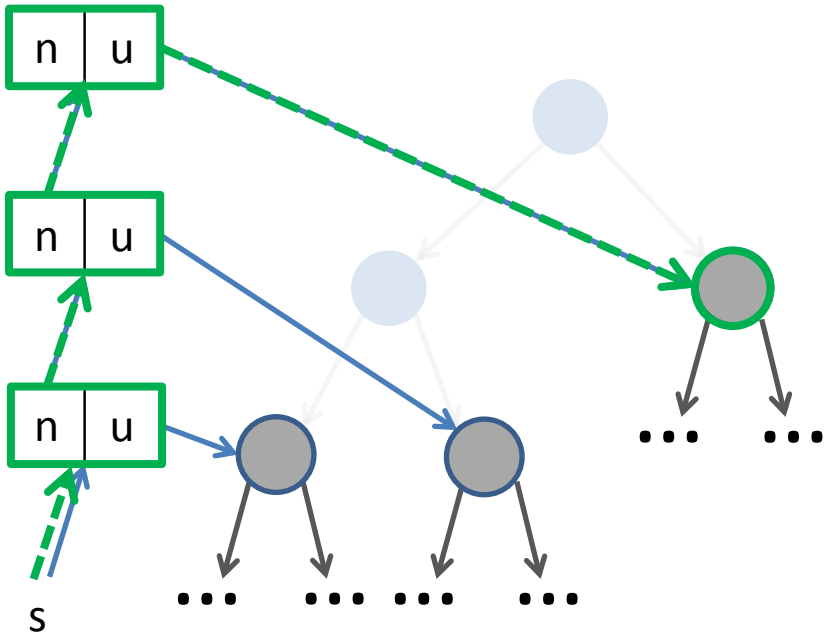


- Do these iterations access the same memory cell?

heap[heap[s].u]

heap[heap[heap[s].n].n]

The problem



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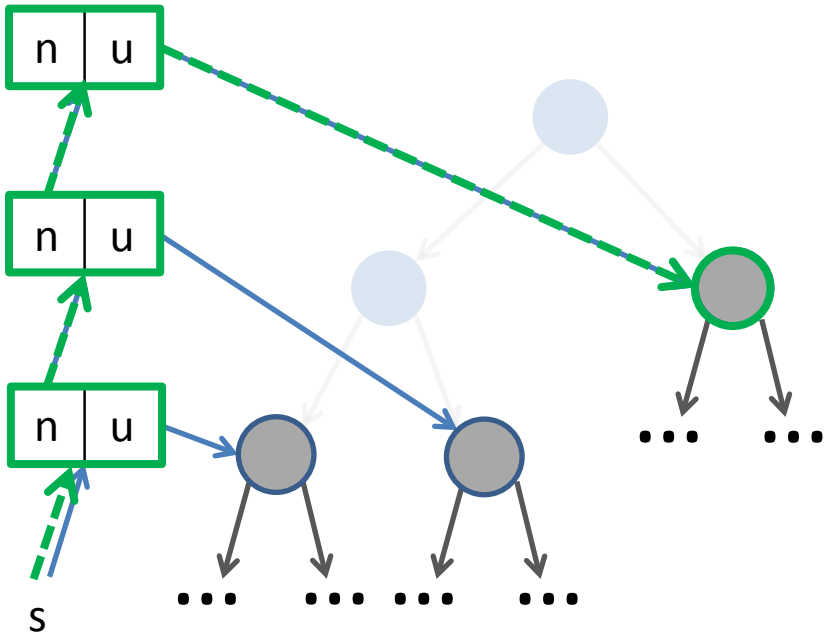
The problem



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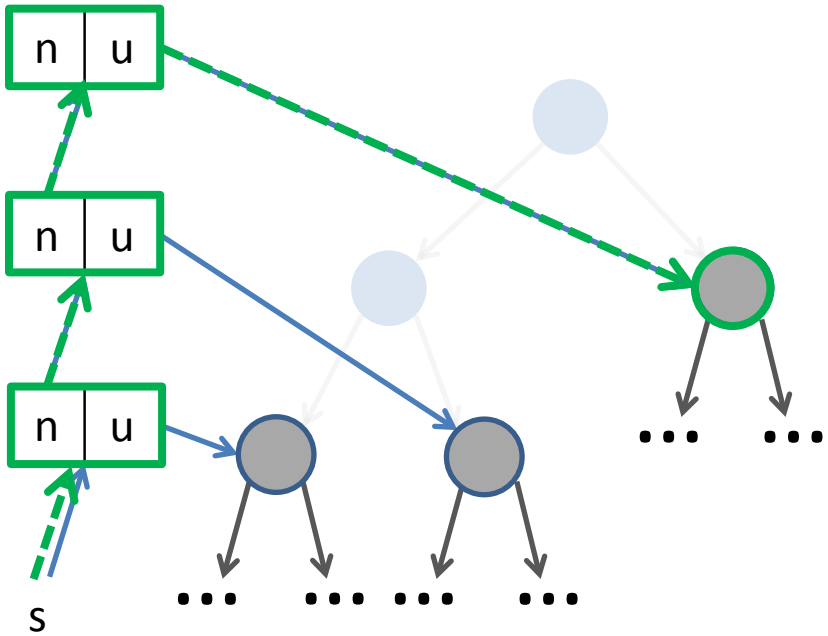
heap[heap[s].u] heap[heap[heap[heap[s].n].n].u]

= ?

The problem



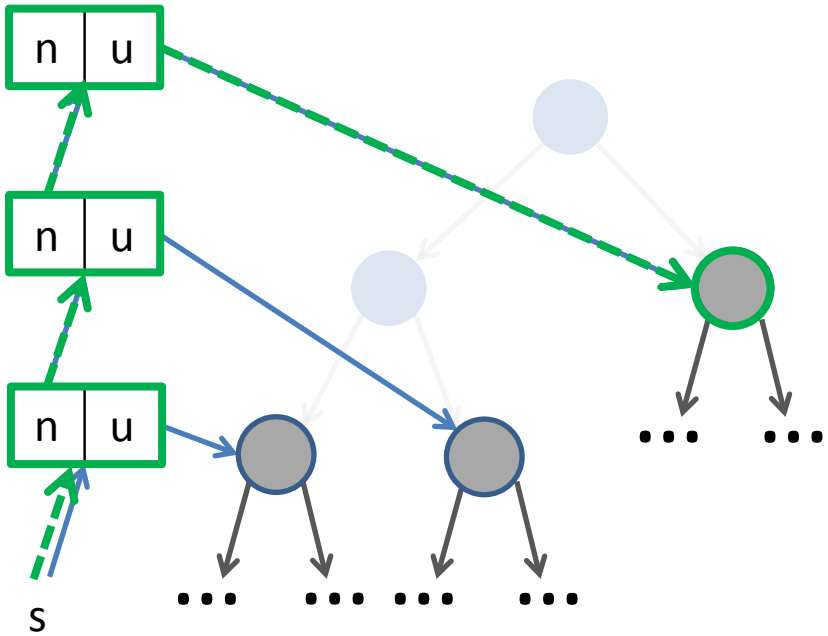
Traverse a linked list

- Do these iterations access the same memory cell?

heap[heap[s].u] heap[heap[heap[heap[s].n].n].u]

= ?

The problem



... which has links to sub-trees

- Do these iterations access the same memory cell?

heap[heap[s].u] = ? heap[heap[heap[heap[s].n].n].u]

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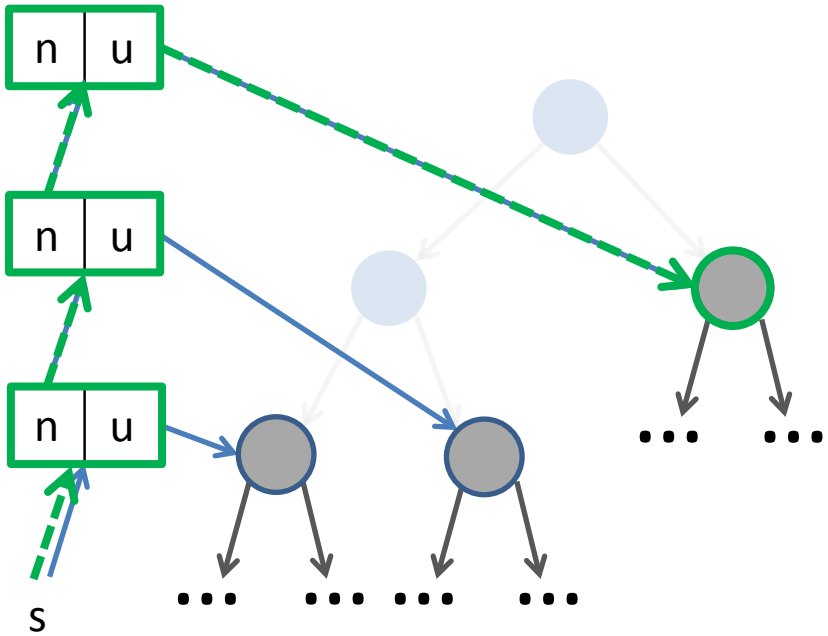

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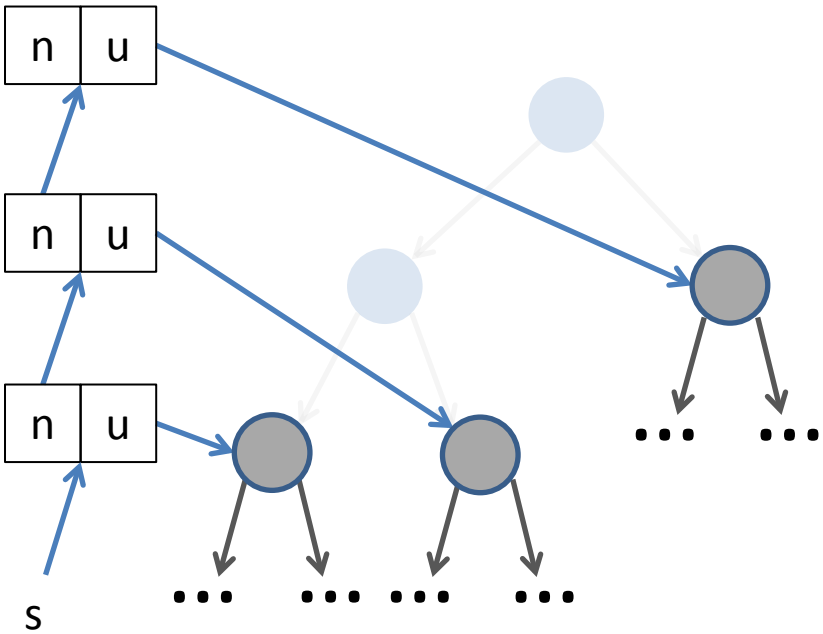
heap[heap[s].u] = ? heap[heap[heap[heap[s].n].n].u]

- Need to reason about structure, heap layout and disjointness
- None of this is explicit in the above representation

Classical first order logic

Describe heap layout with formulae



Classical first order logic

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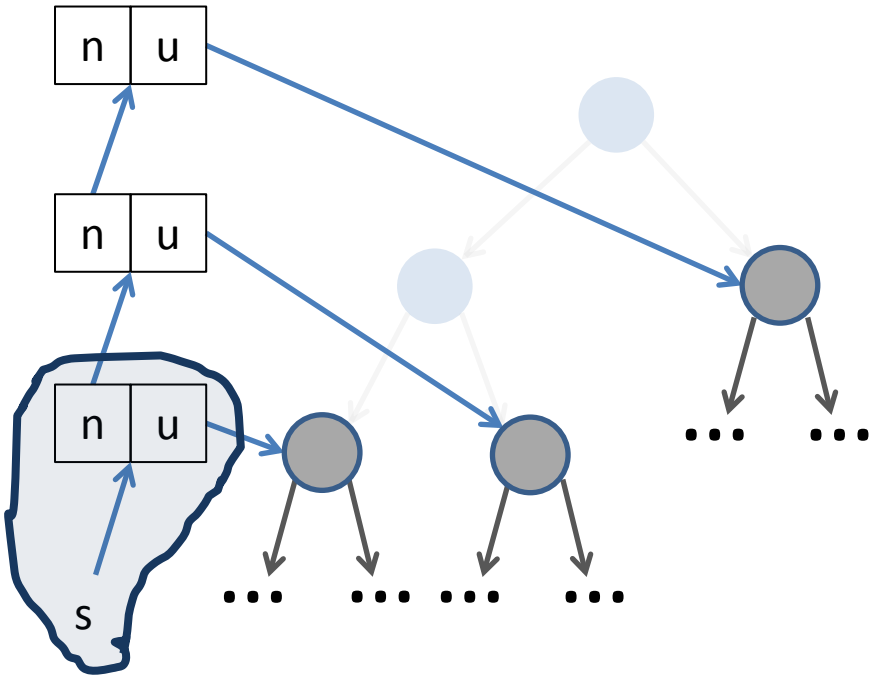

$$\underbrace{s \rightarrow}\ \underbrace{[u\colon u_1', n\colon s_1']}$$

"*s* points to a record with fields *u* and *n*"

Classical first order logic

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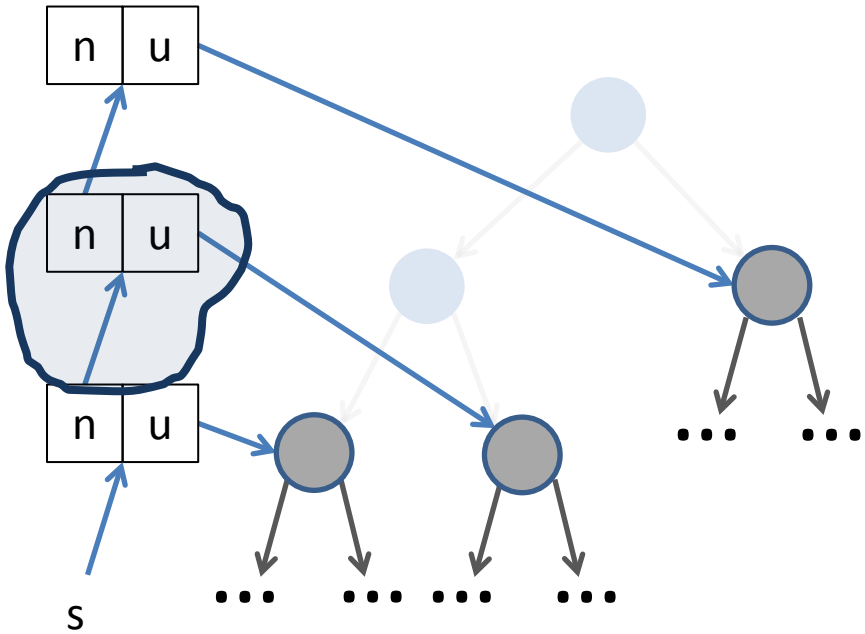
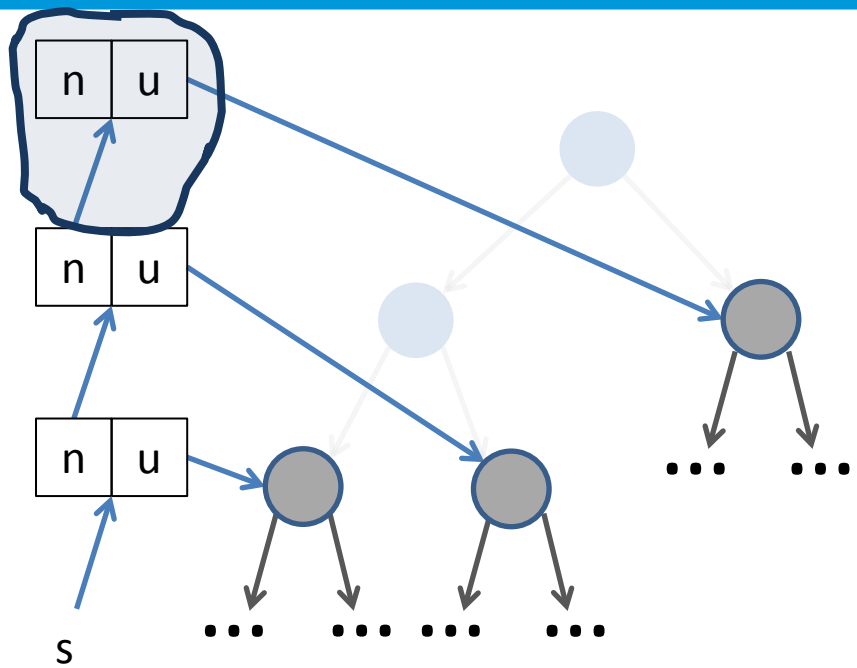


$$s \rightarrow [u: u_1', n: s_1'] \;\; \wedge \;\; s_1' \rightarrow [u: u_2', n: s_2']$$

Classical first order logic

Describe heap layout with formulae



$$s \rightarrow [u: u_1', n: s_1'] \ \wedge \ s_1' \rightarrow [u: u_2', n: s_2'] \ \wedge \ s_2' \rightarrow [u: u_3', n: 0]$$

Classical first order logic

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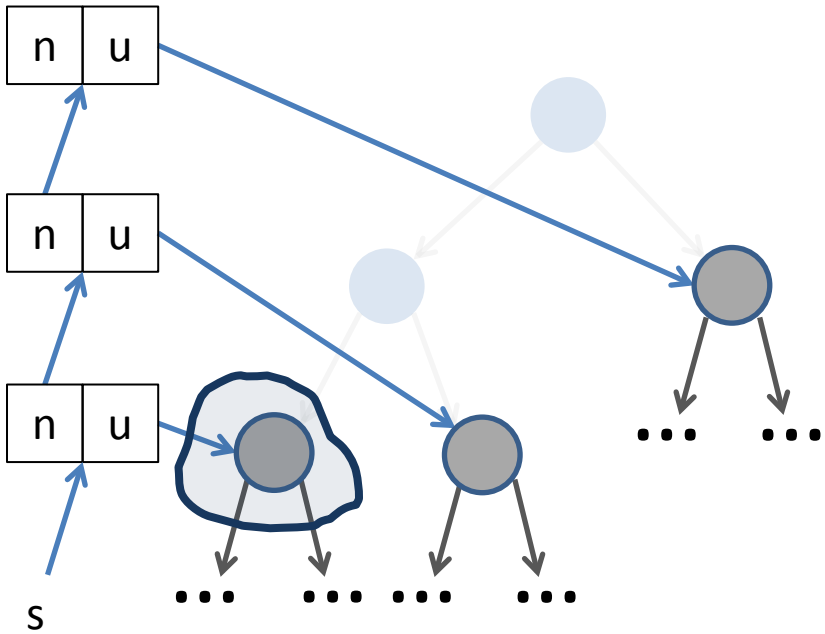
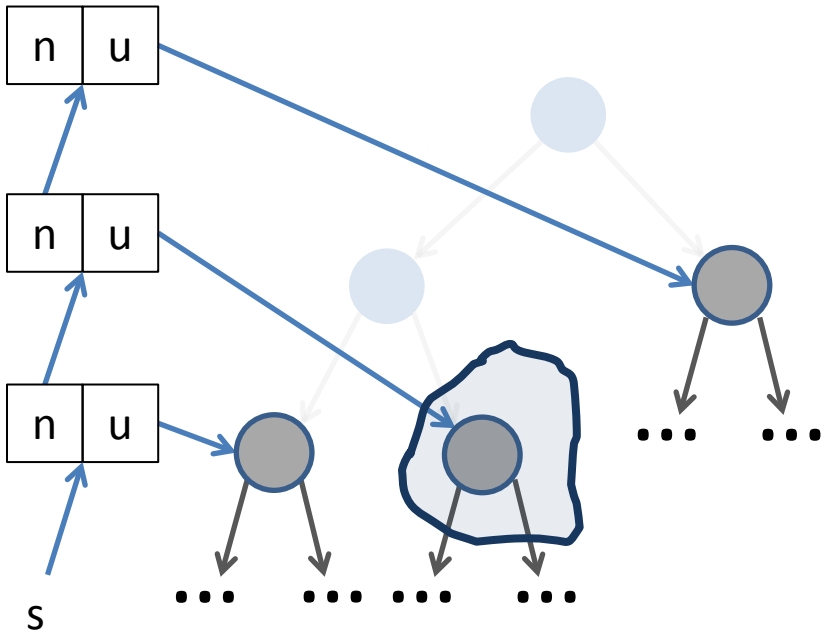


$$s \rightarrow [u: u_1', n: s_1'] \;\wedge\; s_1' \rightarrow [u: u_2', n: s_2'] \;\wedge\; s_2' \rightarrow [u: u_3', n: 0]$$
$$\wedge\; u_1' \rightarrow [l: u_4', r: u_5']$$

Classical first order logic

Describe heap layout with formulae



$$s \rightarrow [u: u_1', n: s_1'] \;\wedge\; s_1' \rightarrow [u: u_2', n: s_2'] \;\wedge\; s_2' \rightarrow [u: u_3', n: 0]$$

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Classical first order logic

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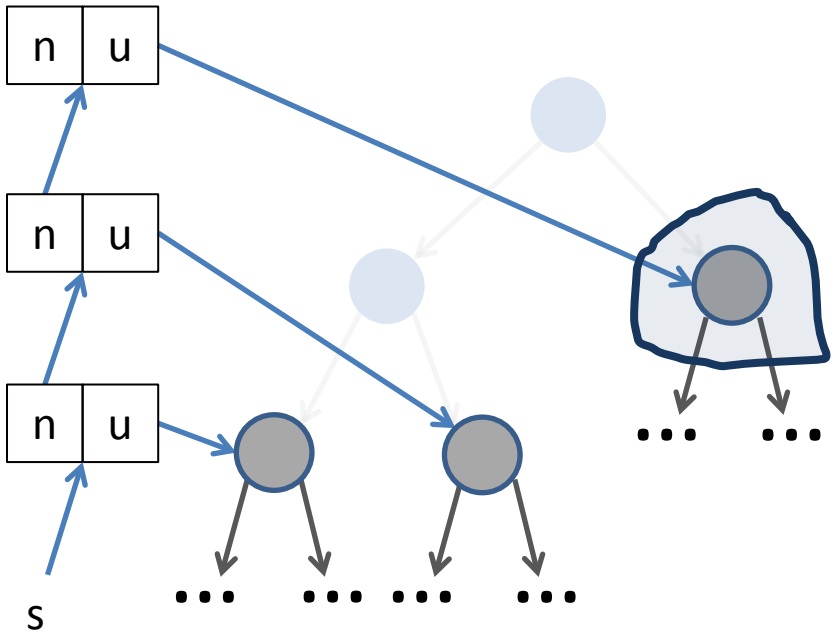

$$s \rightarrow [u: u_1', n: s_1'] \;\wedge\; s_1' \rightarrow [u: u_2', n: s_2'] \;\wedge\; s_2' \rightarrow [u: u_3', n: 0]$$

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Classical first order logic

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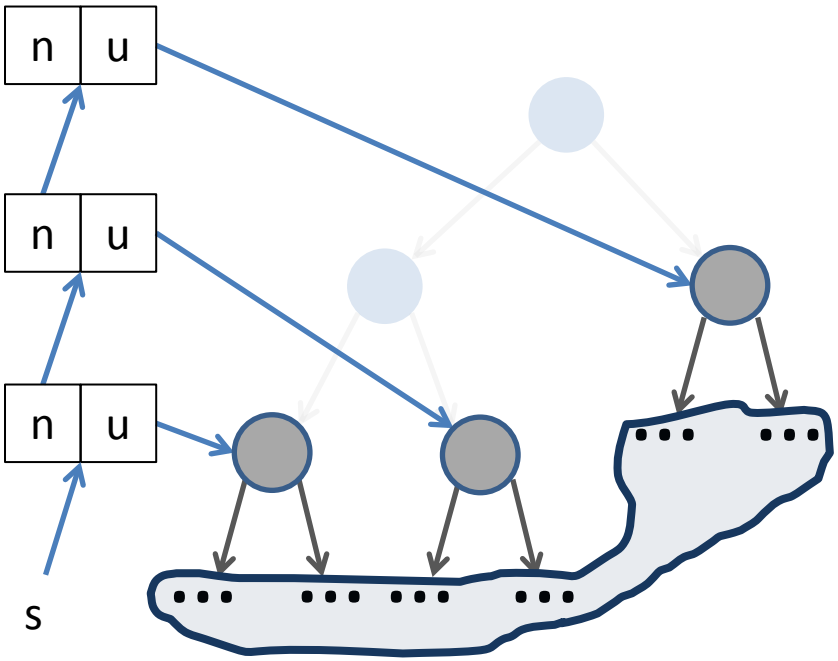

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$$\wedge\; \ldots$$

Classical first order logic

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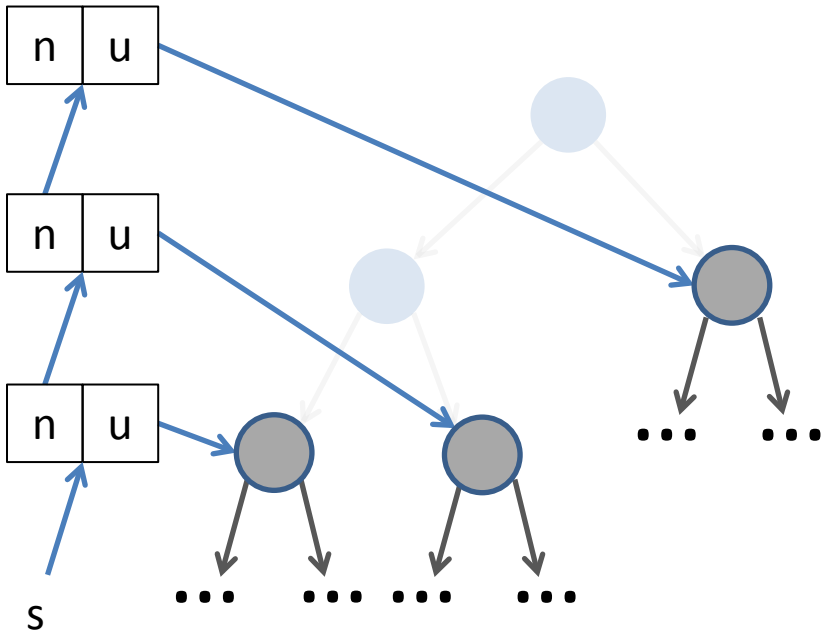

Conjunction '∧' does not rule out aliasing!

$$s \rightarrow [u: u_1', n: s_1'] \wedge s_1' \rightarrow [u: u_2', n: s_2'] \wedge s_2' \rightarrow [u: u_3', n: 0]$$

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Classical first order logic

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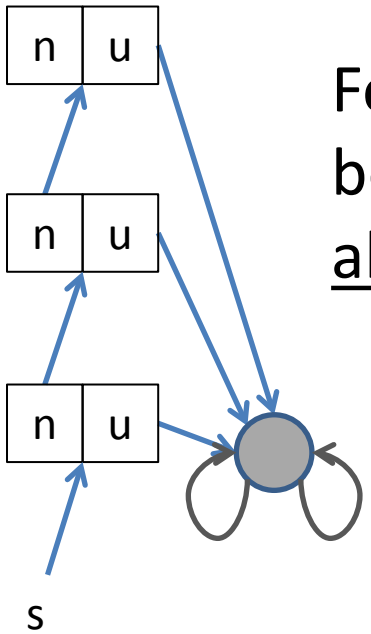

Formula below can <u>also</u> mean this

Conjunction '∧' does not rule out aliasing!

$$s \rightarrow [u: u_1', n: s_1'] \;\wedge\; s_1' \rightarrow [u: u_2', n: s_2'] \;\wedge\; s_2' \rightarrow [u: u_3', n: 0]$$
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Classical first order logic

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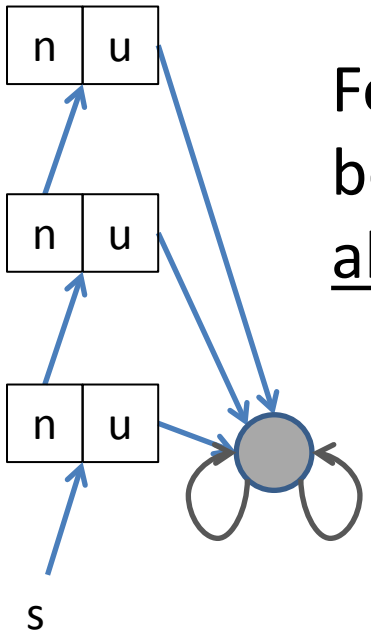

Formula below can <u>also</u> mean this

Conjunction

All u-pointers alias

$$u'_1 = u'_2 = u'_3 = u'_4 = u'_5 = u'_6 = u'_7 = u'_8 = u'_9 = \cdots$$

aliasing!

$$s \rightarrow [u: u'_1, n: s'_1] \;\wedge\; s'_1 \rightarrow [u: u'_2, n: s'_2] \;\wedge\; s'_2 \rightarrow [u: u'_3, n: 0]$$

$$\wedge\; u'_1 \rightarrow [l: u'_4, r: u'_5] \;\wedge\; u'_3 \rightarrow [l: u'_8, r: u'_9] \;\wedge\; u'_2 \rightarrow [l: u'_6, r: u'_7]$$

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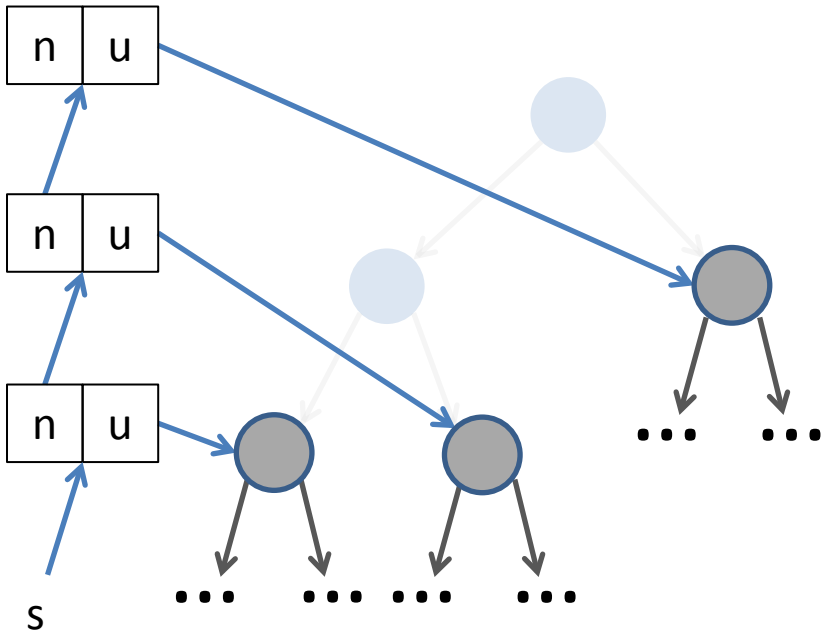
Classical first order logic

Describe heap layout with formulae



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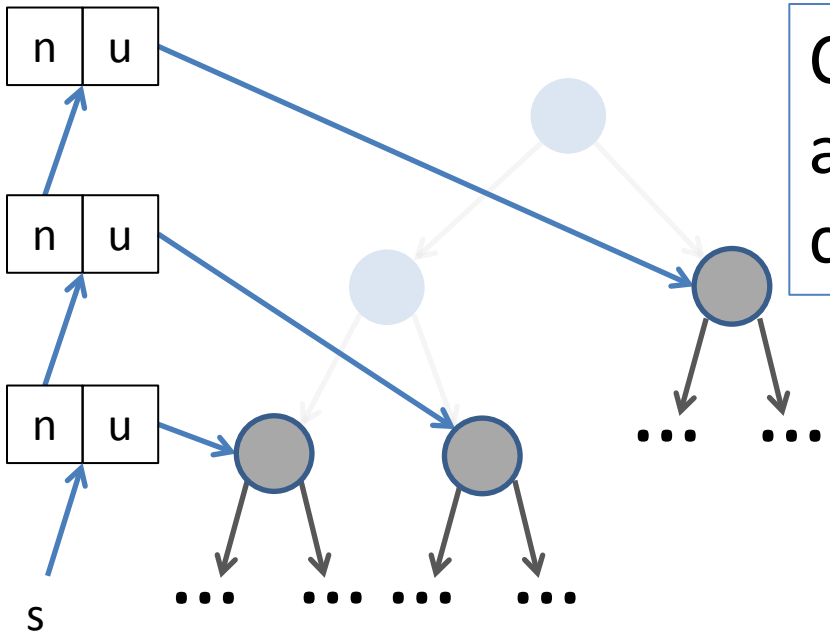

Could add loads of constraints

Conjunction '∧' does not rule out aliasing!

$$s \rightarrow [u{:}\,u_1', n{:}\,s_1'] \;\wedge\; s_1' \rightarrow [u{:}\,u_2', n{:}\,s_2'] \;\wedge\; s_2' \rightarrow [u{:}\,u_3', n{:}\,0]$$

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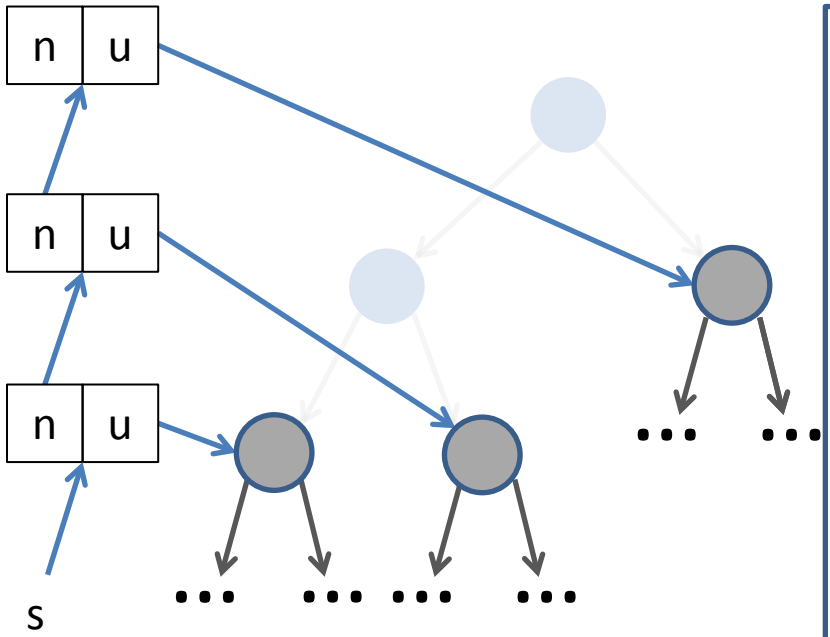
$$\wedge\, u_3' \neq u_8' \wedge u_2 \neq u_3' \wedge u_2' \neq u_4' \wedge u_2' \neq u_5' \wedge u_2' \neq u_6' \wedge \ldots$$

Separation logic

Describe heap layout with formulae



O'Hearn, Reynolds, Ishtiaq, Yang:

Separating conjunction '*'

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Separation logic

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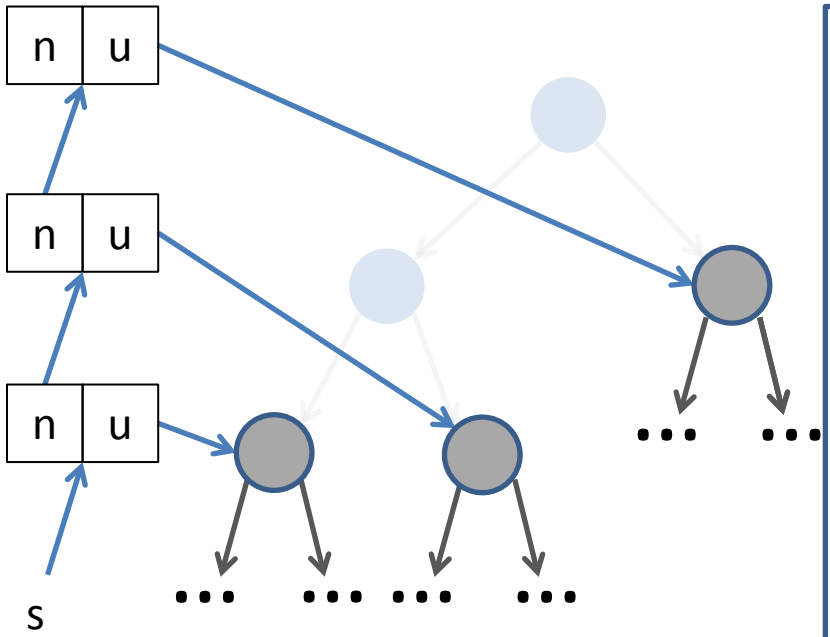

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Separating conjunction '∗' rules out aliasing!

$$s \rightarrow [u{:}\,u_1', n{:}\,s_1'] \;\wedge\; s_1' \rightarrow [u{:}\,u_2', n{:}\,s_2'] \;\wedge\; s_2' \rightarrow [u{:}\,u_3', n{:}\,0]$$

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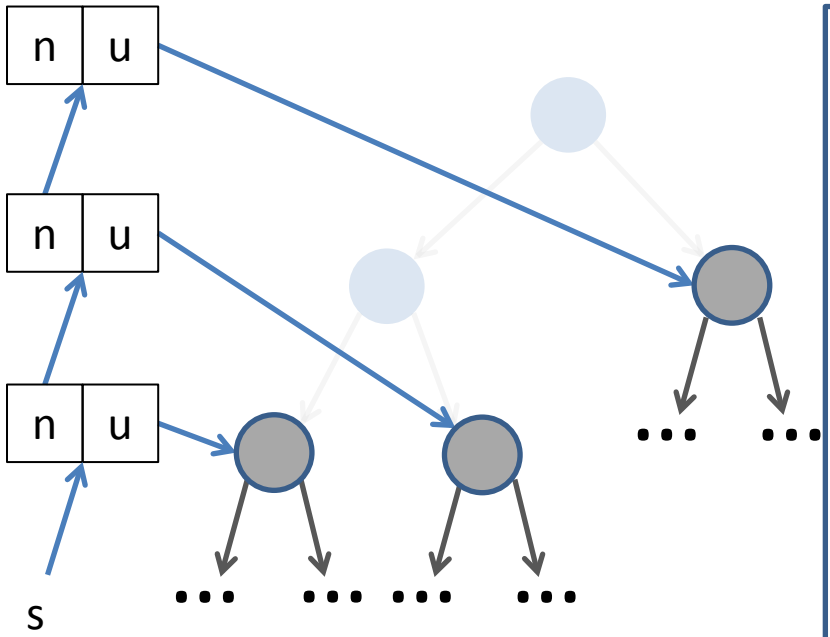

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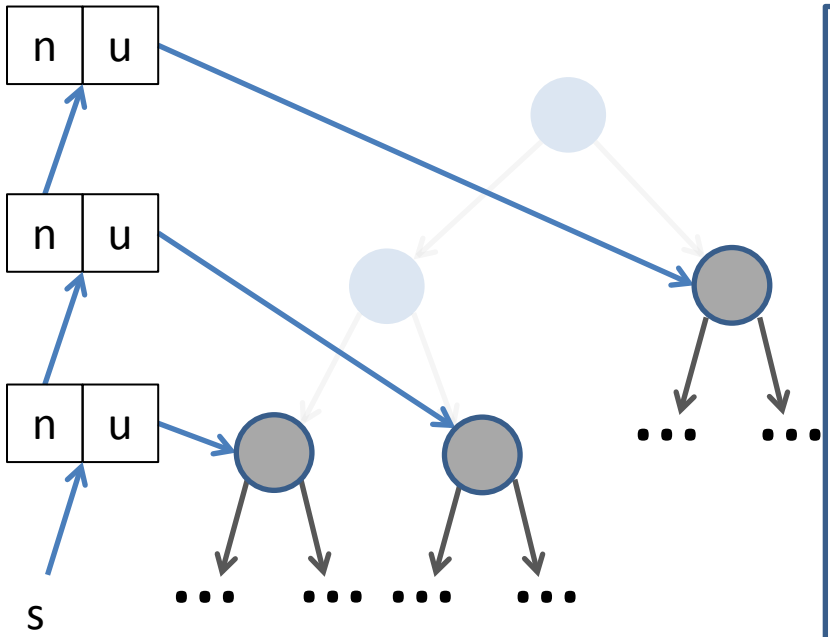

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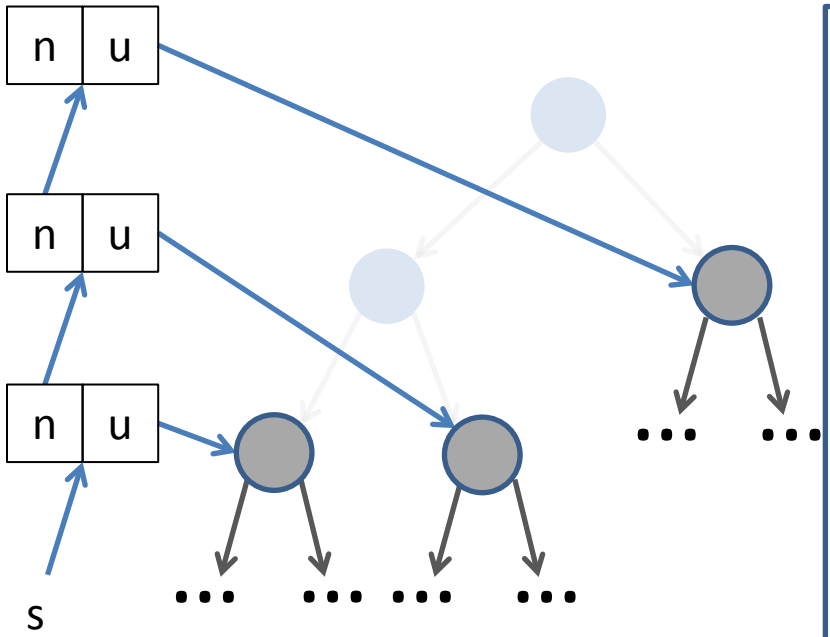

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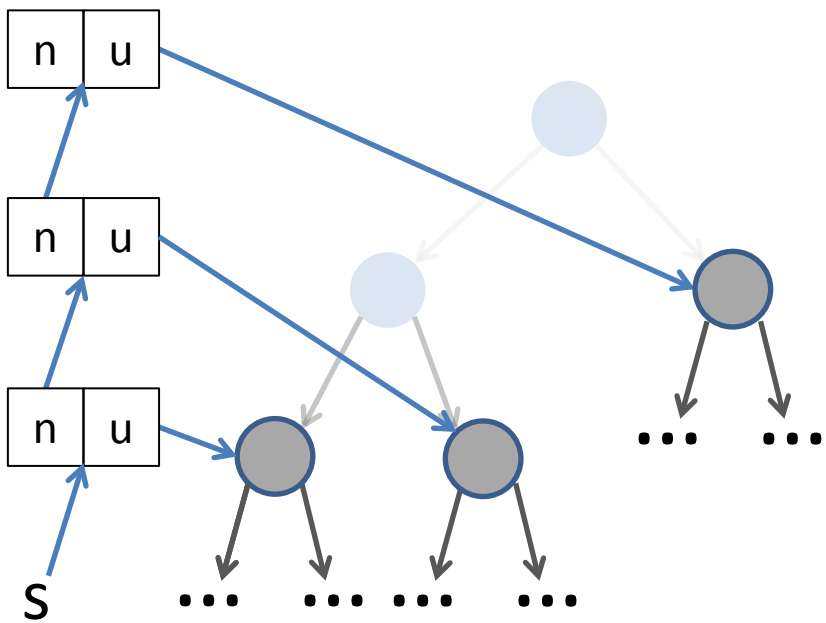
- Tractable heap analysis – very popular in SW verification
- We use it to prove disjointness of heap regions

Back to our partitioning task



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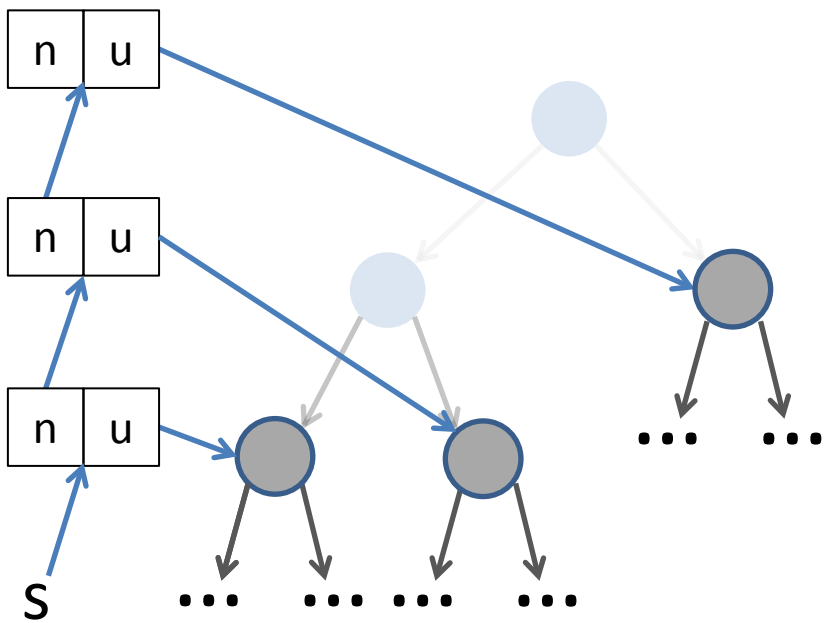
Back to our partitioning task



- Partitioning the heap = partitioning the formula describing it

$$s \rightarrow [u: u_1', n: s_1'] \ * \ s_1' \rightarrow [u: u_2', n: s_2'] \ * \ s_2' \rightarrow [u: u_3', n: 0]$$

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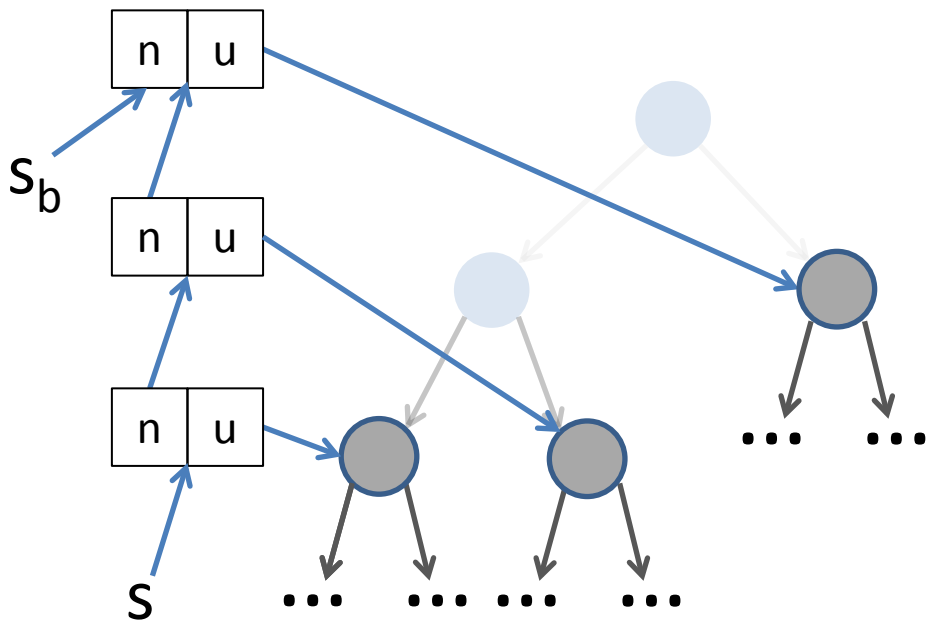
Back to our partitioning task



- Partitioning the heap = partitioning the formula describing it
- Add a second 'hook' into the data structure

$$s \rightarrow [u: u_1', n: s_1'] \ * \ s_1' \rightarrow [u: u_2', n: s_2'] \ * \ s_2' \rightarrow [u: u_3', n: 0]$$

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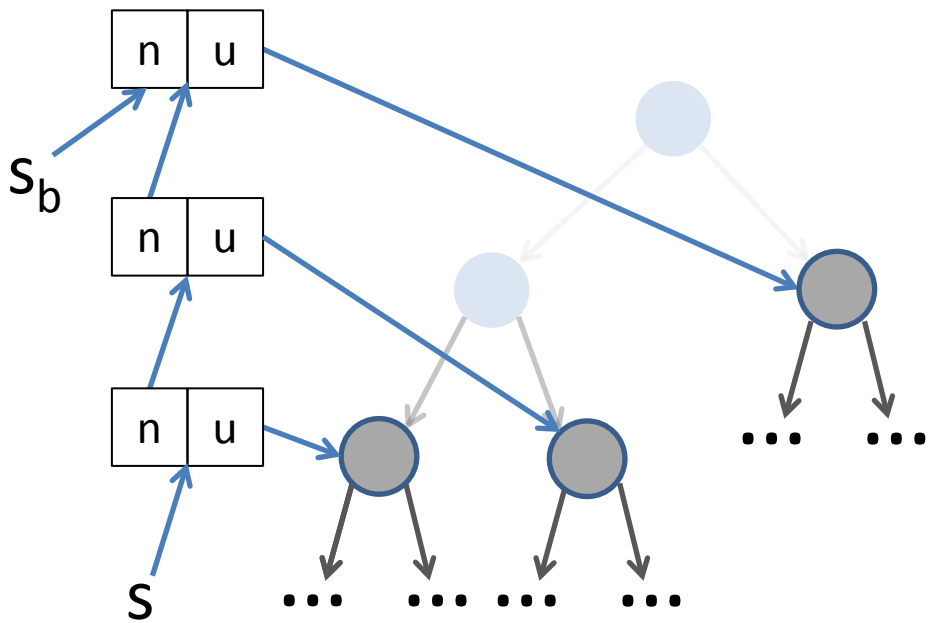
Back to our partitioning task



- Partitioning the heap = partitioning the formula describing it
- Add a second 'hook' into the data structure
- 'Symbolically' step through loop iterations

$$s \rightarrow [u: u_1', n: s_1'] \ * \ s_1' \rightarrow [u: u_2', n: s_2'] \ * \ s_2' \rightarrow [u: u_3', n: 0]$$

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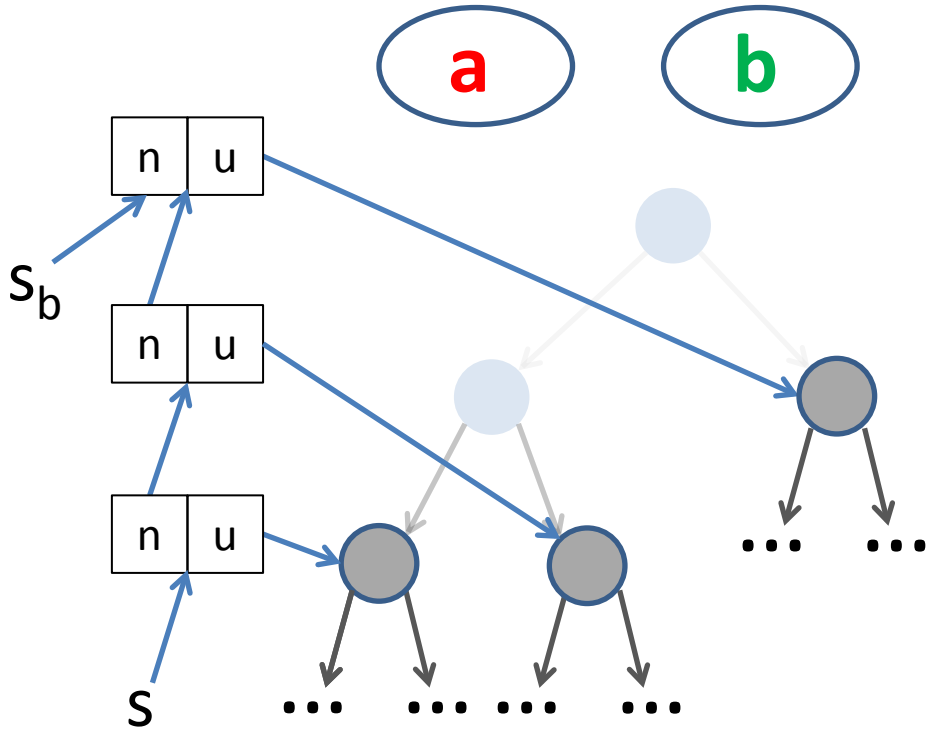
Back to our partitioning task



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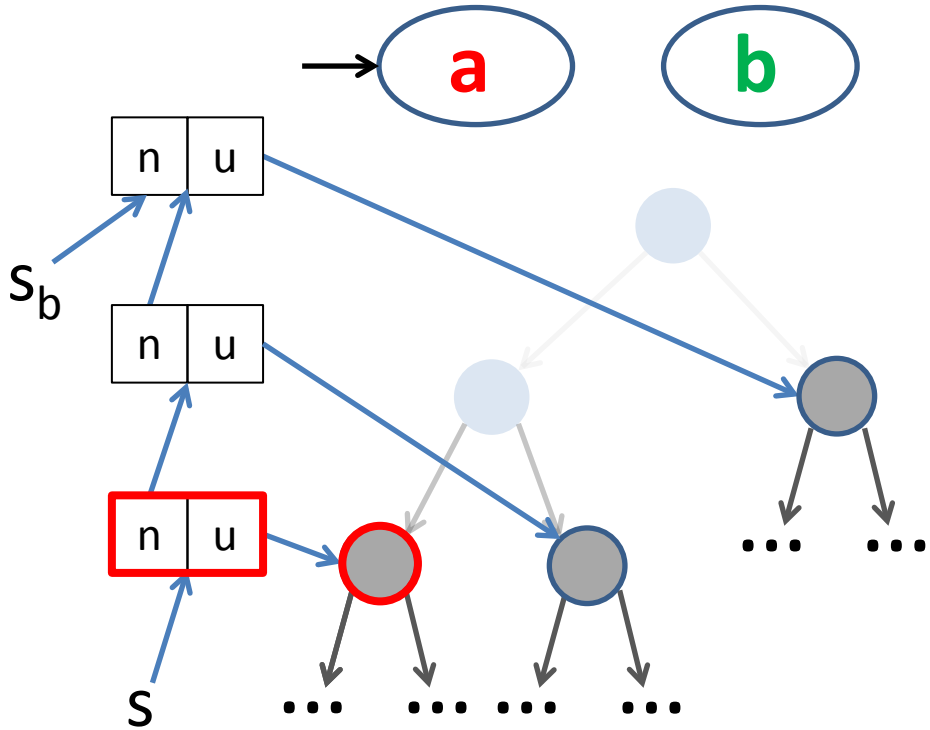
Back to our partitioning task



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- Add a second 'hook' into the data structure
- 'Symbolically' step through loop iterations

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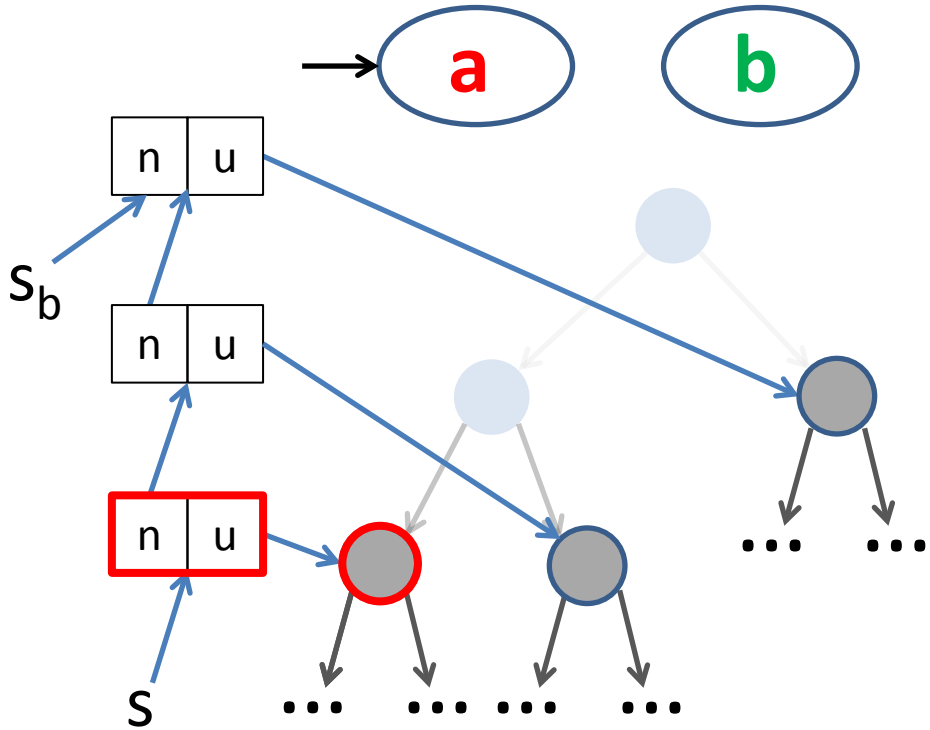
Back to our partitioning task

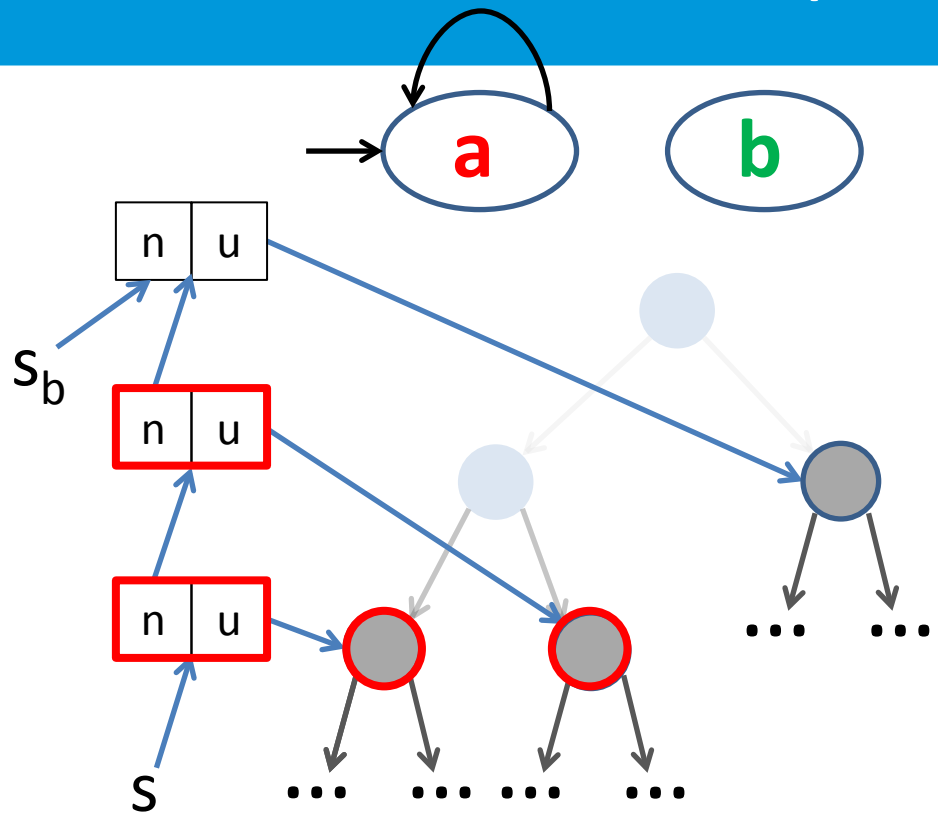


- Partitioning the heap = partitioning the formula describing it
- Add a second 'hook' into the data structure
- 'Symbolically' step through loop iterations
- Attach labels to heaplets

$$s \rightarrow [u{:}\,u_1', n{:}\,s_1']_{\mathbf{a}} * s_1' \rightarrow [u{:}\,u_2', n{:}\,s_2'] * s_2' \rightarrow [u{:}\,u_3', n{:}\,0]$$

$$* \; u_1' \rightarrow [l{:}\,u_4', r{:}\,u_5']_{\mathbf{a}} * u_3' \rightarrow [l{:}\,u_8', r{:}\,u_9'] * u_2' \rightarrow [l{:}\,u_6', r{:}\,u_7']$$

Back to our partitioning task



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- Attach labels to heaplets

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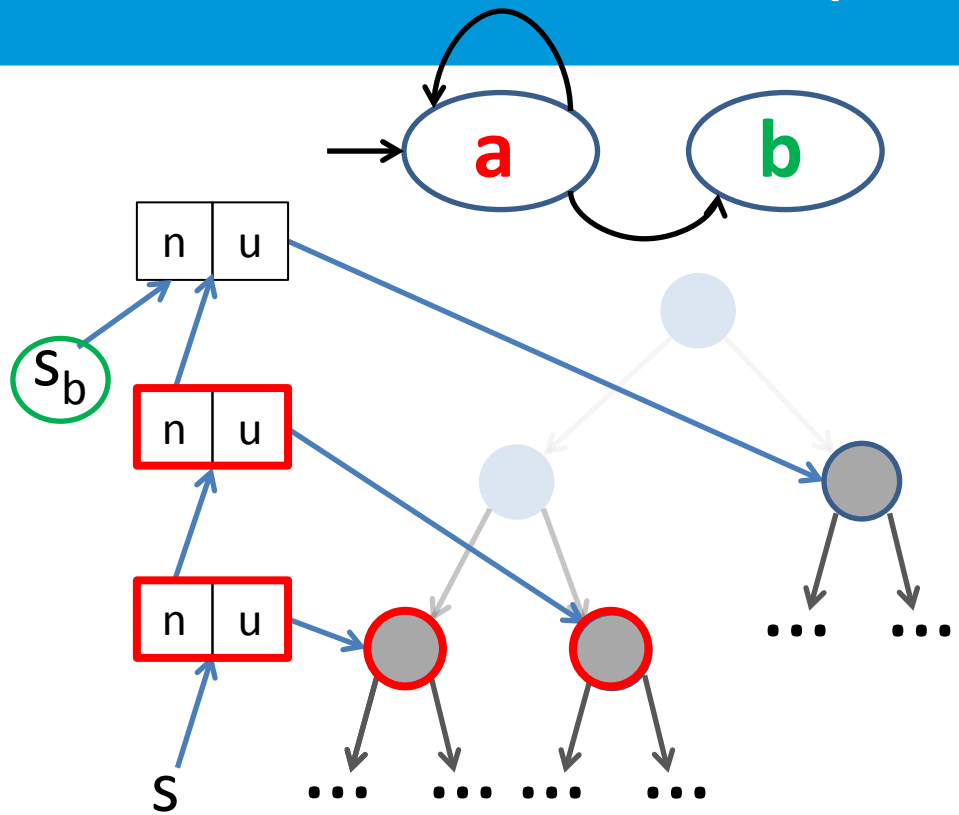

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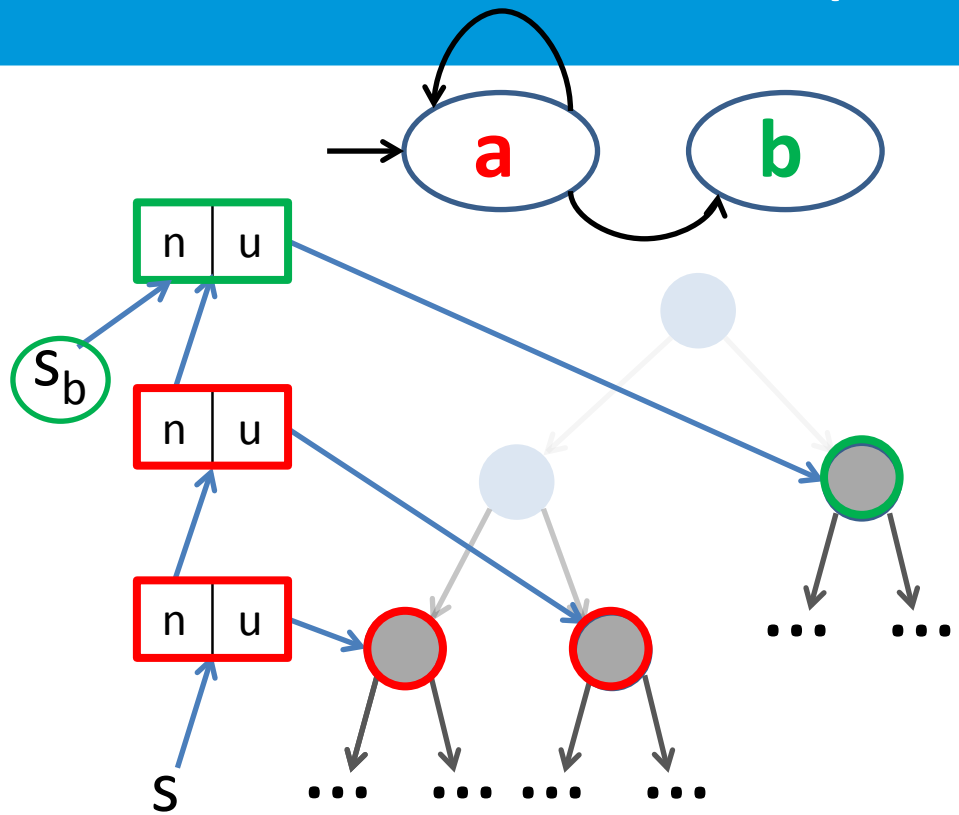

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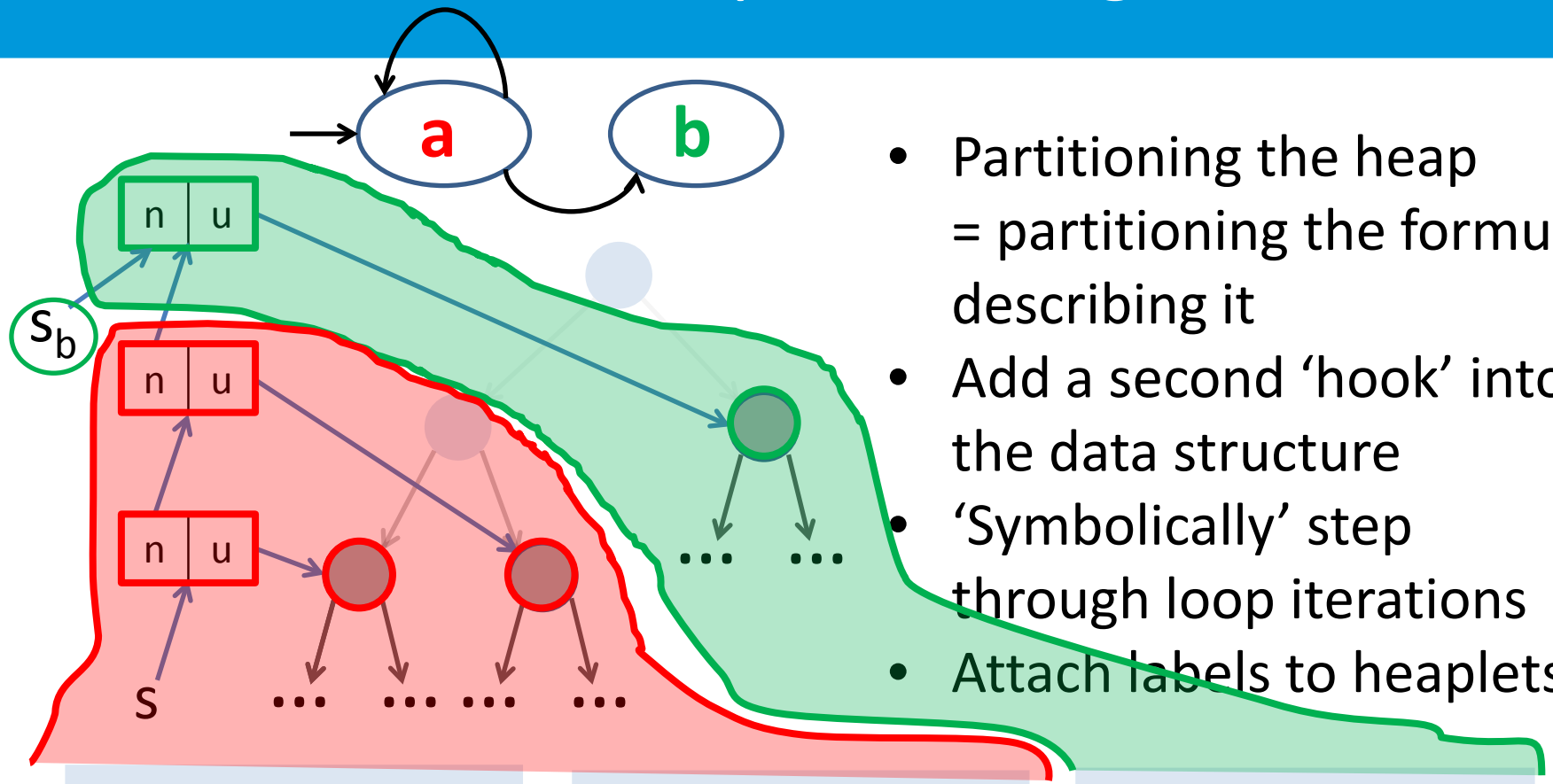

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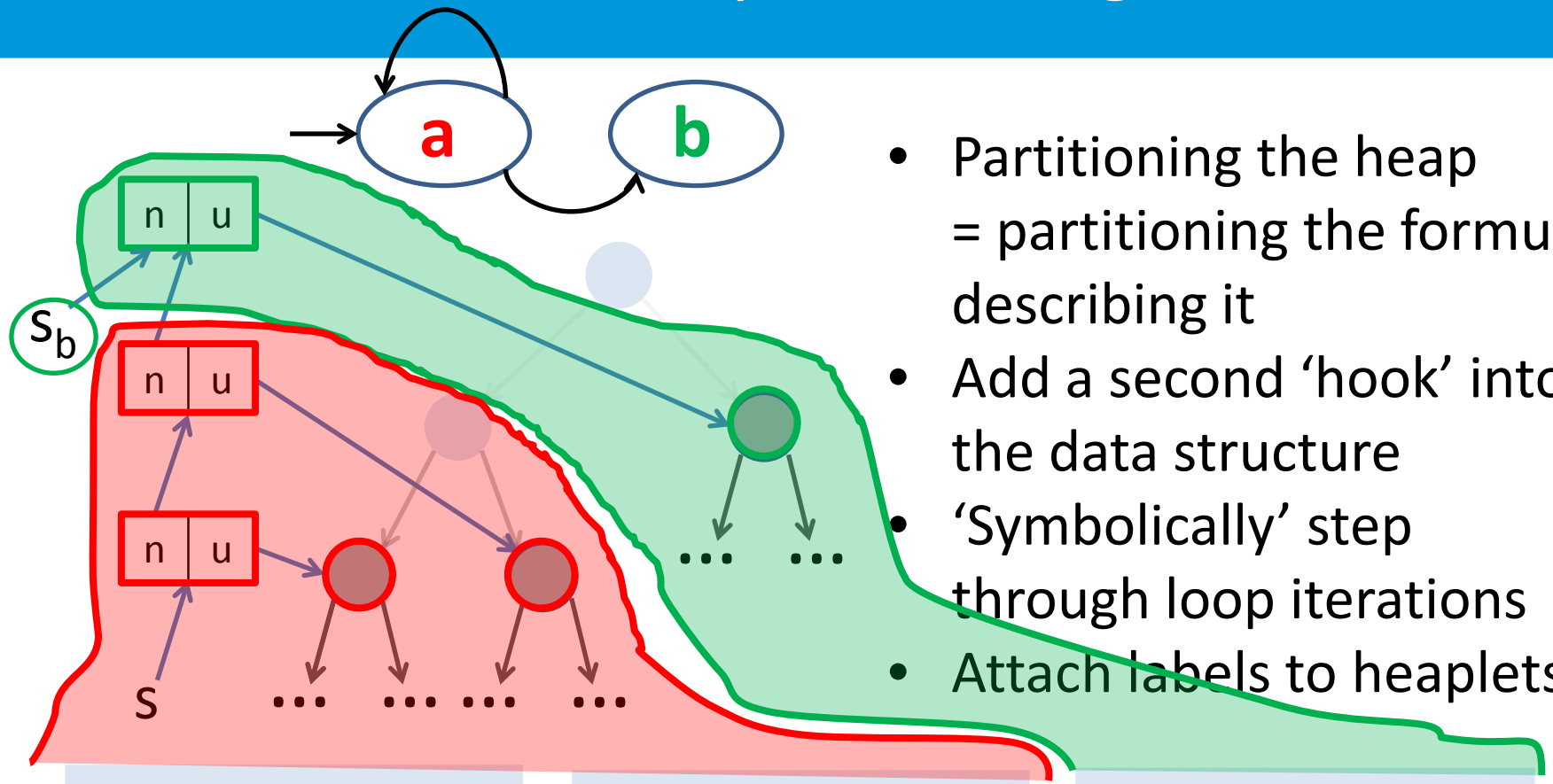
Back to our partitioning task



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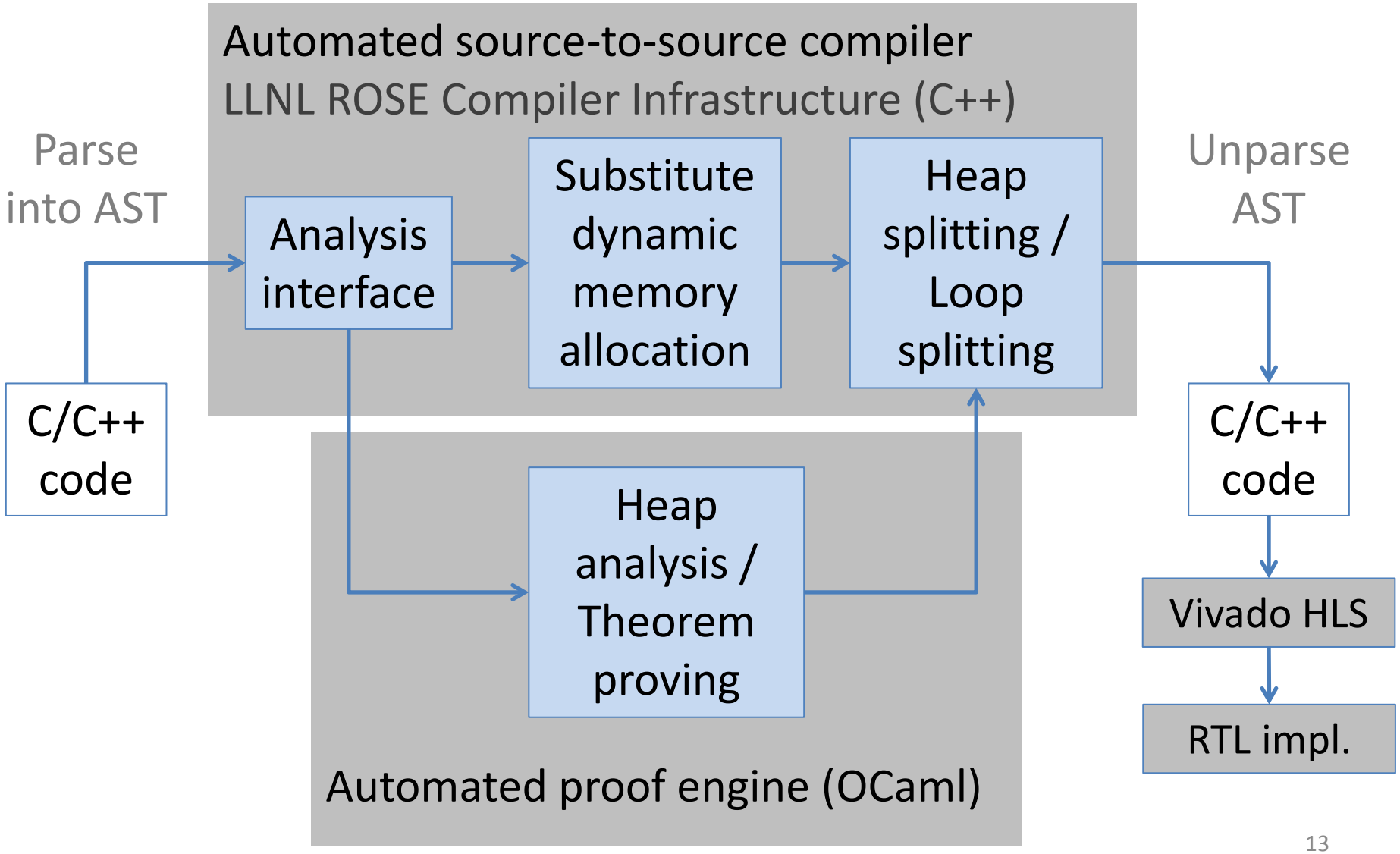
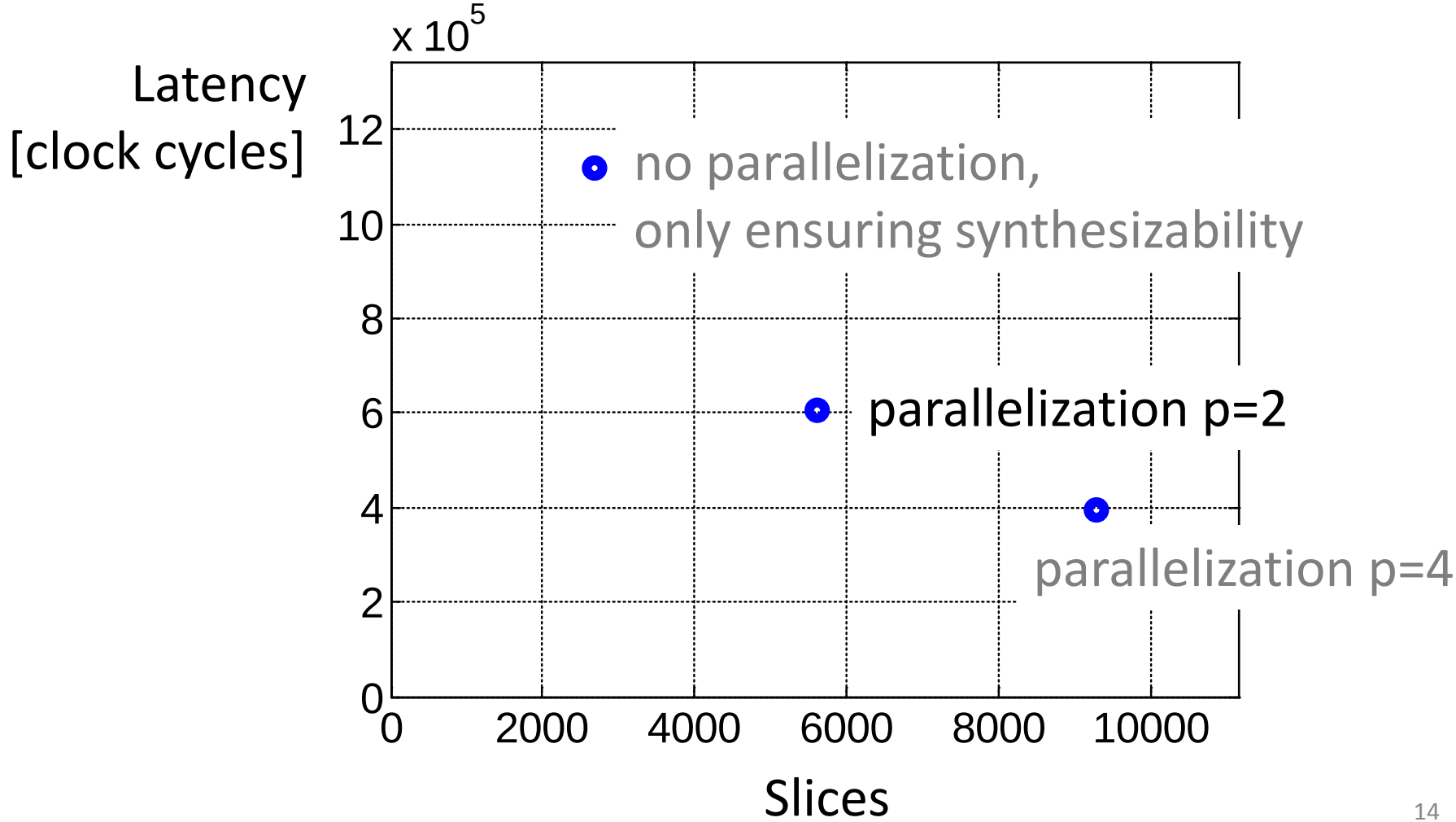
Communication-free parallelism: Never $\ldots_{\mathbf{ab}}$

Implementation



Case Studies (I)

Tree-based *K*-means clustering



Case Studies (II)

		P	Slices	Clock	Cycles	
1	**Merger (linked lists)**					
	Baseline (no par.)	1	574	9.0 ns	21167k	x4
	Autom. Parallelization	4	965	8.7 ns	5483k	
2	**Tree deletion (tree, linked list)**					
	Baseline (no par.)	1	1521	5.2 ns	901k	x2
	Autom. Parallelization	2	4069	6.0 ns	487k	
3	***K*-means (tree, linked list, single heap records)**					
	Baseline (no par.)	1	2694	6.1 ns	1120k	x2
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Conclusion

- Static analysis of heap-manipulating programs
  - Leveraging recent advances in separation logic
  - Distribute heap across on-chip memory banks
  - Loop parallelization
- Tool implementation
  - Automated heap analyzer
  - Automated source-to-source transformations (synthesizability and parallelization)
  - Successful parallelization using standard HLS tools
- Future work
  - Use this analysis for efficient loop pipelining
  - … and automatic on-chip buffer insertion in interface to external memory
  - Compute worst-case/average-case bounds on heap usage

Thank you for listening.

http://cas.ee.ic.ac.uk/people/fw1811/