Physically-Aware Analysis of Systematic Defects in Integrated Circuits

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Conventional Test $\equiv$ Filtering

**TEST DEFINES YIELD**

$YIELD = \frac{\text{Good chips}}{\text{Total chips}}$

**TEST ENSURES QUALITY**

**ACTL Focus:**

**TEST DATA MINING**

$\text{ESCAPE} = \text{BAD chips tested as good}$

$\text{YIELD LOSS} = \text{Good chips tested as bad}$
ACTL Research

- **Fault modeling and evaluation:** Fault Tuples [TCAD 06], METER [TCAD 11] [ISTFA 12], [ICCAD11]
- **Diagnosis:** DIAGNOSIX [VTS05] [ITC06] ITC[10][D&T12]
- **Adaptive and PAN-detect Test:** [ITC 08] [ITC 09] [VTS 10] [ICCAD 11]
- **Learning in Test:** [DAC 12] [TCAD 11][VTS09][ITC08][VTS08]
- **On-Chip Diagnostics:** [ITC12]
- **Volume Diagnostics for Yield Learning:** [D&T12][TCAD12][ITC11][DAC11][VTS11]
Talk Outline

- DFM Rule Evaluation
  - Making sure systematic defects are prevented

- Systematic Defect Identification
  - Finding systematic defects using volume diagnosis data

- Virtual Failure Data Creation
  - Validating/improving proposed methodologies
Design for manufacturability (DFM) ≡ layout constraints
- DFM costs are clear, yield benefits are not

Goal: A Test-Data Mining methodology that
- Measures DFM rule relevance
- Measures relative effectiveness of DFM rules
- Quantifies yield benefit on a per-rule basis
- Identifies new rules when needed
DFM Rule Evaluation

- **Failing ICs**
- **Volume diagnosis**
- **IC layout**
- **Passing layout area**

**Q1**: DFM violation leads to failure?
**Q2**: Which rule is more important?
**Q3**: How much yield would be recovered?
Q1: Association Confirmation

DFM rule check data summary

<table>
<thead>
<tr>
<th></th>
<th>Passing layout area</th>
<th>Failing layout area</th>
<th>$\sum$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Adhered rule</td>
<td>$X_{00}$</td>
<td>$X_{01}$</td>
<td>$X_{0.}$</td>
</tr>
<tr>
<td>Violated rule</td>
<td>$X_{10}$</td>
<td>$X_{11}$</td>
<td>$X_{1.}$</td>
</tr>
<tr>
<td>$\sum$</td>
<td>$X_{0}$</td>
<td>$X_{1}$</td>
<td>$X_{..}$</td>
</tr>
</tbody>
</table>

Hypothesis testing

$H_0 :$ DFM independent of failure  
$H_1 :$ DFM associated with failure

$$T = 2 \sum_{i=0}^{1} \sum_{j=0}^{1} X_{ij} \log \left( \frac{X_{ij} X_{..}}{X_{i..} X_{.j}} \right)$$

Likelihood Ratio Test

Reject $H_0$ if $T > t_\alpha$
Q2: Which Rule Is More Important?

Relative risk

\[
RR = \frac{P(\text{Failure} \mid \text{Violation})}{P(\text{Failure} \mid \text{Adherence})} = \frac{P(F \mid A')}{P(F \mid A)} \approx \frac{X_{01}X_{10}}{X_{11}X_{00}} \approx \frac{(X_{01} + 0.5)(X_{10} + 0.5)}{(X_{11} + 0.5)(X_{00} + 0.5)}
\]

Range of \( RR \) | Interpretation
-- | --
0.00 < \( RR \) << 1 | Adherence 1/\( RR \) × more likely to cause failure
\( RR \) ≈ 1 | Violation and failure independent
1 << \( RR \) | Violation \( RR \) × more likely to cause failure
### Experiment Setup

- **Nvidia 90nm GPU**
  - > 9 million gates
  - ~4000 test patterns
  - ~8.5mm x 9mm layout area
  - 9400 failed chips analyzed

- **4 categories/19 DFM rules evaluated**

<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
<th>Total</th>
<th>Analyzed</th>
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</thead>
<tbody>
<tr>
<td>MX.ENC.1R</td>
<td>Metal-via enclosure check</td>
<td>7</td>
<td>5</td>
</tr>
<tr>
<td>MX.ENC.2R</td>
<td>Metal-via enclosure check</td>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>MX.DEN.3R</td>
<td>Density check</td>
<td>7</td>
<td>2</td>
</tr>
<tr>
<td>MXY.WD.4R</td>
<td>Metal width and density check</td>
<td>7</td>
<td>5</td>
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</table>

#### Layout region

<table>
<thead>
<tr>
<th>Rule</th>
<th>Passing</th>
<th>Failing</th>
<th>Total</th>
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</thead>
<tbody>
<tr>
<td>M8.ENC.2R</td>
<td>75</td>
<td>163</td>
<td>238</td>
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<tr>
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<td>1,329</td>
<td>5,252</td>
<td>6,581</td>
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<tr>
<td>Violated rule</td>
<td>1,404</td>
<td>5,415</td>
<td>6,819</td>
</tr>
</tbody>
</table>

Certain DFM rules have no violation. Excluded from the analysis.
Experiment Results – Rule Ranking

**Observation 1:** via issues may cause more yield loss than density issues in this design/process

**Observation 2:** Relative risk and yield impact produce different ranking

Assumption: 15% yield loss and 50% of violations are corrected
Systematic Defect Identification

Diagnose large number of IC failures

Volume diagnosis

Generate layout images at the failure location

Layout snippet

Group similar snippet images into clusters

Snippet clustering

Confirm systematic defect existence (simulation/PFA)

Defect validation
## Clustering Result – LSI Test Chip Failures

<table>
<thead>
<tr>
<th>Layer</th>
<th>No. clusters $K$</th>
<th>Cluster weight</th>
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<th></th>
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<tr>
<td></td>
<td></td>
<td>min</td>
<td>max</td>
<td>avg.</td>
<td></td>
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<tr>
<td>polysilicon</td>
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<td>135</td>
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<tr>
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<td>1</td>
<td>344</td>
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<tr>
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<tr>
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<tr>
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<td>47.1</td>
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<td>Lithography simulations</td>
<td>SEM photos</td>
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<tr>
<td>-----------------</td>
<td>-------------------------</td>
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<td></td>
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<tr>
<td>Weight 40 polysilicon layer</td>
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<td><img src="image2.png" alt="Image" /></td>
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<tr>
<td>Weight 29 metal-2 layer</td>
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<td><img src="image4.png" alt="Image" /></td>
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</tr>
</tbody>
</table>
Fast & Accurate Defect Simulation

**SLIDER**: Simulation of _Layout_- Injected Defects for Electrical Responses
Defect Generation

Random defects
- Random defects
- Defect density & size distribution (DDSD)
- Defect injection that follows DDSD

Systematic defects
- Systematic defects
- Pattern to match
- Defect injection at pattern-matched locations

User-specified defects
- User-specified defects
- User gives defect locations (x,y), layer, polygon vertices, etc.
Experiment – Scalability

100 random defects simulated for runtime measurement

No. of cells

Total

Total

Analog

Simulation time (s)

SLIDER overhead (s)

<table>
<thead>
<tr>
<th></th>
<th>80%</th>
<th>85%</th>
<th>90%</th>
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<tr>
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<tr>
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Application – Virtual Test Data Creation

- 100 random DDSD defects + 100 systematic defects
- Mix them in different proportions (0%, 10%, 20%, ..., 100%)

SLIDER enables bug fix and technique improvement
Summary

- **DFM Rule Evaluation**
  - Statistical analysis to identify important rules
  - Rule ranking prioritizes rule adherence
  - **Experiments:** Nvidia GPU, simulation

- **Systematic Defect Identification**
  - Clustering analysis to identify systematic issues
  - Problematic patterns can be formulated into new rule
  - **Experiments:** LSI test chip, Nvidia GPU, simulation

- **Virtual Failure Data Creation**
  - Validating/improving proposed methodologies

- **Acknowledgments:** SRC, NSF, Nvidia, and LSI
Relevant ACTL Publications www.ece.cmu.edu/~actl

1. X. Yu and R. D. Blanton, “Diagnosis-assisted Adaptive Test,” To Appear: IEEE Transactions on CAD.


