Large-Reach Memory Management Unit Caches
Abhishek Bhattacharjee
Department of Computer Science, Rutgers University

1. Address Translation Overhead
• Nominally-sized applications: 10% - 15%\(^1,2\)
• Virtualization: 89%\(^1,2\)
• Big-data workloads: 5-85%\(^3\)

2. Address Translation Hardware

3. Real-System Measurements
• Intel i7, 8 cores, 8GB memory, 512-entry TLBs
• 32-entry L2 PSC, 4-entry L3 PSC, 2-entry L4 PSC

4. Coalesced MMU Caches

5. Shared MMU Caches

6. Results
• Multiple ports and PTWs give 1-2% perf on 8-core CMP
• Combined approach within 3-5% of ideal case (3x larger MMU cache)
• Coalesced MMU caches provide more predictable performance improvements (10 – 12% on average)

7. References