The new VCO uses a two-stage emitter follower as buffers for each output. Two back-to-back junction diodes are used as the varactor, and the anode is connected to the base of the BJT to minimize the N/sub parasitic capacitance effect. The spiral inductor uses two turns to generate a 740pH inductance. A single differential inductor is used for higher Q and to save area. Because the tanks are connected to the bases of the transistors, the two tanks can be easily combined without using additional components.

For the measurements, we use RF probes to directly connect to the bare die. Single ended measurement setup is used throughout. Figure 9.7.4 shows the measured output power spectrum. The measured tuning range is compared with the simulated tuning range in Fig. 9.7.5. Measurement results show more than 5GHz (25%) tuning range. The VCO core consumes 2mA, and each emitter follower branch drains 0.5mA from 4.5V respectively. The maximum output power variation is less than 3.5dBm over the whole frequency tuning range. Figure 6 shows the measured phase noise. A low power signal close to the noise floor is injected at the other differential output to eliminate the random drifting of the free running VCO. At high injection levels, the phase noise of the VCO follows the phase noise of the source. But at low injection levels the phase noise approaches its intrinsic level. The measured phase noise is –101.17dBc/Hz at a 1MHz offset from 19.4GHz with the minimum injection signal power (1dB above the noise floor).

In this paper, a negative-resistance cell that utilizes a MOS capacitor for emitter degeneration is proposed. The MOS transistors are cross-linked common-source amplifiers to further enhance the negative resistance. The proposed cell maintains its negative resistance value up to very high frequencies, and the target negative resistance for a given frequency can be achieved using a small transconductance value. Hence a low-power and low-noise design is possible. The small effective parasitic capacitance allows for a wide tuning range or alternately can be used to provide a larger output swing using an increased value inductor. The tank connection to the base of a transistor minimizes power supply pulling and makes a single tank design easy. The 20GHz VCO with the proposed negative-resistance cell shows a 5GHz tuning range. The VCO core consumes 9mW and the buffers consume an additional 9mW. The measured phase noise is –101.7dBc/Hz at 1MHz offset from 19.4GHz. The proposed negative-resistance cell implemented using BJTs can also be realized as a MOS structure and is technology independent.

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References:

A low phase-noise wide tuning range VCO is a critical building block in high-performance serial interface circuits. A negative-resistance cell that has a small effective parasitic capacitance combined with high-quality LC tanks are crucial for high quality VCOs. There have been several efforts to reduce the parasitic capacitance of the basic Armstrong structure [1,2] to improve the VCO performance, but these structures require an integrated transformer that is non-trivial to design, especially at high frequencies. This paper presents a capacitive emitter-degenerated differential negative-resistance cell that has a very small effective parasitic capacitance, with the result that it is capable of a large tuning range with low phase noise and small power consumption. The 20GHz VCO design is implemented in a 0.25µm SiGe BiCMOS, and shows a wide tuning range, 5GHz, with small power consumption and low phase noise.

A capacitive emitter-degenerated transistor provides a negative resistance looking into the base terminal as shown in Fig. 9.7.1. The small-signal equivalent shunt resistance (R_{eq}) and equivalent capacitance (C_{eq}) are also shown in this figure. When g_m^2 is larger than C_e/C_i, the equivalent resistance is always negative even above the transistor F_T, showing the effectiveness of this design for high frequency operation. Also note that the equivalent capacitance is smaller than C_i. First, C_e and C_i are in series. Second, the g_m cell affects the charge buildup across each capacitance and increases the effective C_i while decreasing the effective C_e, thus further reducing the effective series capacitance.

Differential signaling is essential in high-speed IC design. Fig. 9.7.2 shows the evolution of the differential negative-resistance cell. Two negative-resistance cells are designed and an NMOS transistor is added to each emitter. The drain of each NMOS, operating as common source amplifier, is cross-linked as shown. The C_e of the MOS devices provides the equivalent emitter degeneration capacitor and the two current sources are combined as shown in Fig. 9.7.2. The positive feedback path due to the cross-coupled MOS devices provides additional negative resistance improving the cell’s effectiveness. The combined effect of emitter degeneration and MOS positive feedback allows us to use small bias currents to generate effective negative resistance. This has a dual effect, it reduces the power consumption and it also reduces the noise contribution from the VCO core bipolar transistors improving the overall phase noise performance.

Figure 9.7.3 compares the typical Armstrong VCO architecture [3] with the proposed architecture. The tank in the Armstrong structure sees three transistors, the base of Q2, the collector of Q1 and the base of the buffer transistor Q3. But in the proposed architecture, the tank only sees one transistor, the base of Q1. Moreover, recall that the equivalent capacitance looking into the base of Q1 is much smaller than the C_e, showing the effectiveness of this new architecture is its small power supply pulling effect. In the Armstrong architecture, any change in the power-supply voltage only affects the collector-base junction capacitance, which has only a small contribution to the total tank capacitance. At 20GHz, the simulated R_{eq} is -500Ω and C_{eq} is 13.5pF. Note that the equivalent capacitance is about 1/9th the value of the C_i’s of Q1 (128pF).
Figure 9.7.1: Basic negative-resistance cell and equivalent shunt R and C.

\[ R_{eq} = \frac{\alpha r_s^2 (C_e + C_r)^2 + (1 + g_m r_s)^2}{\alpha C r_s (C_e - C_r g_m r_s)} \]

\[ C_{eq} = \frac{\alpha r_s^2 C_e (C_e + C_r) + C_r (1 + g_m r_s)}{\alpha r_s^2 (C_e + C_r)^2 + (1 + g_m r_s)^2} \]

Figure 9.7.2: Evolution of the differential negative-resistance cell.

Figure 9.7.3: Comparison between Armstrong and new proposed structure.

Figure 9.7.4: Measured VCO output power spectrum.

Figure 9.7.5: Measured and simulated tuning range.

Figure 9.7.6: Phase noise measurement data.
Figure 9.7.7: Chip micrograph.
$R_{EQU} = \frac{\omega^2 r_\pi^2 (C_\pi + C_e)^2 + (1 + g_m r_\pi)^2}{\omega^2 C_e r_\pi (C_e - C_\pi g_m r_\pi)}$

$C_{EQU} = \frac{\omega^2 r_\pi^2 C_\pi C_e (C_\pi + C_e) + C_e (1 + g_m r_\pi)}{\omega^2 r_\pi^2 (C_\pi + C_e)^2 + (1 + g_m r_\pi)^2}$

Figure 9.7.1: Basic negative-resistance cell and equivalent shunt R and C.
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