

A High Performance DDR3 SDRAM Controller

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Abstract—The paper presents the implementation of compliant DDR3 memory controller. It discusses the overall architecture of the DDR3 controller along with the detailed design and operation of its individual sub blocks, the pipelining implemented in the design to increase the design throughput. It also discusses the advantages of DDR3 memories over DDR2 memories operation. Double Data Rate (DDR) SDRAMs have been prevalent in the PC memory market in recent years and are widely used for networking systems. These memory devices are rapidly developing, with high density, high memory bandwidth and low device cost. However, because of the high-speed interface technology and complex instruction-based memory access control, a specific purpose memory controller is necessary for optimizing the memory access trade off. In this paper, a specific purpose DDR3 controller for high-performance is proposed.

I. INTRODUCTION

In computing, DDR3 SDRAM, an abbreviation for double data rate type three synchronous dynamic random access memory, is a modern kind of dynamic random access memory (DRAM) with a high bandwidth interface. It is one of several variants of DRAM and associated interface techniques used DDR3 SDRAM is not directly compatible with any earlier type of random access memory (RAM) due to different signaling voltages, timings, and other factors. DDR3 is a DRAM interface specification. It is the 3rd generation of DDR memories, featuring higher performance and lower power consumption with earlier generations. The actual DRAM arrays that store the data are similar to earlier types, with similar performance. The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). In addition, the DDR3 standard permits chip capacities of up to 8 gigabits. However, in comparison to Random Access Memory (RAM) technology, Content Addressable Memory (CAM) technology is restricted in terms

of memory density, hardware cost and power dissipation. CAM is widely used in network equipment for fast table look up [1]. Recently, a Hash-CAM circuit [2], which combines the merits of the hash algorithm and the CAM function, was proposed to replace pure CAM based lookup circuits with comparable performance, higher memory density and lower cost. Efficient DDR bandwidth utilization [3] is a major challenge for lookup functions that exhibit short and random memory access patterns. Most importantly, off-chip high-density low-cost DDR memory technology has now become an attractive alternative for the proposed Hash-CAM based lookup circuit. However, DDR technology is optimized for burst access for cached processor platforms.

The rest of this paper is organized as follows. In section II, some related works are reviewed. Section III illustrates the Design methodology. Section IV gives the experimental results and section V the conclusion.

II. RELATED WORK

A. Higher operating frequency

The DDR3 has four banks open at time [4]. According to JEDEC [6], DDR3 will be running at 800MHz to 1666 MHz. That would be double the frequency of DDR2. This will bring operational performance to systems by slashing the read and write time into half.

DDR3 Key Improvements

		DDR2	DDR3	Remark
Data rate/pin		400 ~ 800 Mbps	800 ~ 1600 Mbps	Performance
Vdd/Vddq		1.8V +/- 0.1 V	1.5V +/- 0.075 V	Low Power
DQ	ODT	Read	Other term.	High Speed Interface
		Write	Other term. + Self	
	Shielding on PKG	Limited	All DQ signals	
C/A	Termination	No	Yes	
	Topology	Conventional T	Fly-by	
Driver Control		OCD Cal.	Self Cal. with ZQ	
Thermal sensor		No	Yes (Optional)	

Figure 1. Datasheet specification of RAM

B. Lower voltage and power

DDR3 operates at 1.5V instead of the 1.8V for DDR2. The power saving factor is, therefore, 16%. This will offset the higher power consumption brought by increasing the operational frequency. At the same time, die shrinking will also help in power reduction to give DDR3 twice the performance per watt of power. DDR3 is also built-in with power conservation features like partial refresh. The precious system battery power will no longer need to spend on refreshing the portion of the DRAM that is not in active use. It also includes a thermal sensor to allow the system to provide minimum refresh cycles when the system is not in high performance demand thus to achieve further power saving.

C. Modules on fly-by topology

For the higher frequency operations, DDR3 is now more critical on signal integrity of the memory module (DIMM). At the extreme frequencies, the signal path can no longer be balanced, but have to be tuned (trained) to match to each DRAM. The module signal path topology is called the “fly-by” vs. “T branches” as on the DDR2 module. That means the address and control lines will be a single path chaining from one DRAM to another instead of the T topology that branches on DDR2 modules. This method takes away the mechanical line balancing and turn to automatic signal time delay generated by the controller fixed at the memory system training. Each DDR3 DRAM has an automatic leveling circuit for calibration and to memorize the calibrated data.

IV. DESIGN METHODOLOGY

The following discusses the technical difficulties on DDR3 memory systems. To achieve maximum memory efficiency on the system level, system front side bus frequency has to follow suit. The most optimum is to have the front side bus run at the memory data execution frequency. That is 800MHz to 1600MHz. That puts the burden on the processor and also the chipset. On the other hand, higher frequencies also mean more signal integrity issues. Both motherboard and module design engineers have to deal with strip line, micro strip, termination impedance and return loss all those new radio frequency terms. Test equipment for verification of the circuit is no longer available at low costs. The “Fly-By” timing technology puts the burden on system calibration. Memory system is calibrated each time the computer is turned-on. The controller and the DRAM circuit design allow the calibration to be done in an automatic mode. To make this calibration, extra circuit and intelligence has to be added to the controller and to the DRAM. Extra die area on the chip is also required to accommodate. This will add cost to the final system. New processors come with 1MB to 2MB of on-board cache memories. That means there might be no main memory hit during normal non-graphical operations. Therefore, one might never see the performance increase with faster DRAM at

normal applications. Another point of system argument is number of memory slots required for the system. DDR3 specification calls for maximum of 2 two rank modules per channel at the lower frequency of 800MHz to 1333MHz. Only one memory slot is allowed at the maximum operational frequency of 1600MHz.

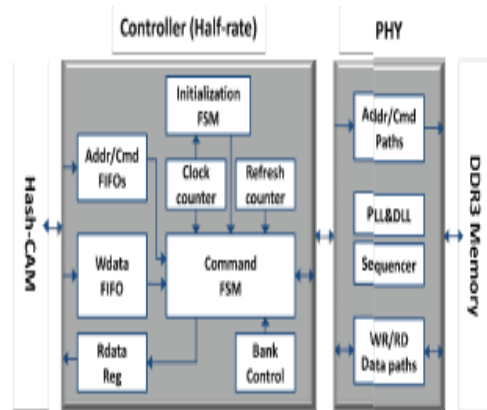


Figure 2. DDR SDRAM interface

A. WR/RD cycle

The starting column and bank address are provided with WRITE command. Fig (3) gives the normal write/read operations with auto precharge option. The write/read cycles must satisfy the delay parameters, such as t_{RCD} , t_{WL} . With this approach, the next access must wait a certain period of time. A fast read can also be achieved by switching banks. This is illustrated in Fig.(4). Apart from this, in DDR3 there are Write and Read levelling mechanisms. This mechanism allows the controller to adjust internal DQS to compensate for unbalanced loading on the board for write and read operations. This will not compensate on per bit basis, only on a byte or DQS basis.

A. DRAM Power Calculators

The IDD values referenced in this article are taken from Micron’s preliminary 1 GB DDR3- 1067 data sheet, and they are listed in “Data Sheet Specifications”. While the values provided in data sheets may differ from between vendors and different devices, the concepts for calculating power are the same.

B. Background Power

CKE is the master on-off switch for the DRAM. When CKE is LOW, most inputs are disabled. This is the lowest power state in which the device can operate, and if all banks are

precharged, it is specified in the data sheet as IDD2P. If any bank is open, the current consumed is IDD3P. IDD2P has two possible conditions, depending on whether mode register bit 12 is set for a slow or fast power-down exit time. The appropriate IDD2P value should be used for the power calculations based on how the application sets this mode register. CKE must be taken HIGH to allow the DRAM to receive ACT, PRE, READ, and WRITE commands. When CKE goes HIGH, commands start propagating through the DRAM command decoders, and the activity increases the power consumption. The current consumed is specified in the data sheet as IDD2N if all banks are precharged or IDD3N if any bank is active. Fig. (2) shows the typical current usage of a DDR3 device when CKE transitions, assuming all banks are precharged. When CKE is HIGH, the device draws a maximum IDD2N of 65mA of current; when CKE goes LOW, that figures drops to an IDD2P of ~10–25mA, depending on how slow or how fast the power-down exit time is. All of these values assume the DRAM is in the precharged state. Similarly, if the device is in the active state, it consumes IDD3P current in power-down (CKE = LOW) and IDD3N current in standby (CKE = HIGH).

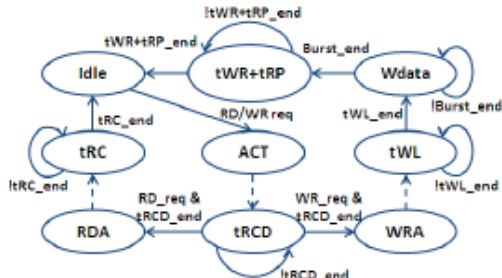


Figure 3. Normal write/read with auto precharge

D. Advantages of DDR3 over DDR2

DDR3 is the next-generation, high-performance solution for CPU systems it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR3 supports data rates of 1066 to 1600 MT/s, with clock frequencies of 533 to 800 MHz, respectively—effectively doubling the speed of DDR2. DDR3’s standard 1.5V supply voltage cuts power consumption by up to 30% over DDR2.

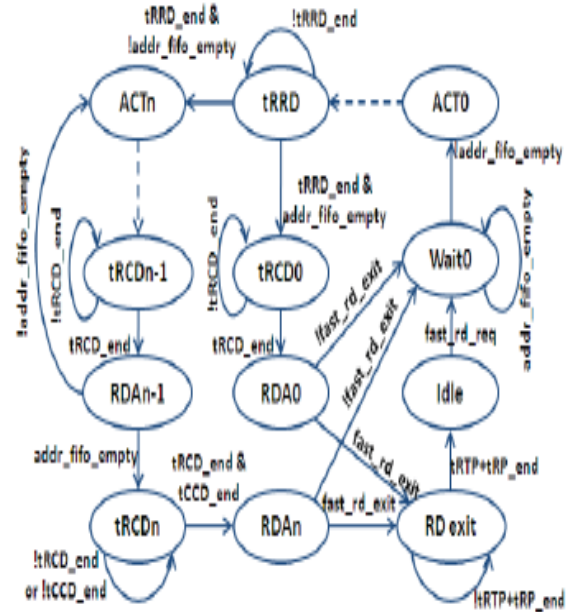


Figure 4. Fast read with auto precharge

V. EXPERIMENTAL RESULTS AND ANALYSIS

In order to validate the proposed controller architecture within a data lookup application, a complete test circuit comprised of Hash-CAM block, Altera’s PHY megacore [6] and Micron’s DDR3 memory model (MT41J128M8) [7] are used. The prototype is designed to work at half-rate frequency of 200MHz and the Hash-CAM sub-block is designed to work at quad-rate, at 100MHz. The functional simulation results are shown in Figure 5. The input data (S_data_in) is clocked at 100MHz. For each hash value (CRC_addr), the DDR3 controller returns two output values in two clock cycles at 200MHz, e.g. $R0$ and $R0'$. Each output data pair ($R0$ and $R0'$) is comprised of an address and a data field, stored in the DDR3. The $R0$ and $R0'$ data fields are compared in parallel with the input data (S_data_in). The corresponding address field of the matching data set is asserted as the final address value ($Addr_out$). The total lookup latency for each request is 15 clock cycles at 100MHz. Because the system is fully pipelined, successive address outputs are expected after 15 clock cycles at every clock cycle. The complete circuit was synthesized using Altera’s Stratix III technology and tested with a 64-bit wide DDR3 module. The estimated on-chip power dissipation in this work is 4513.79mW.

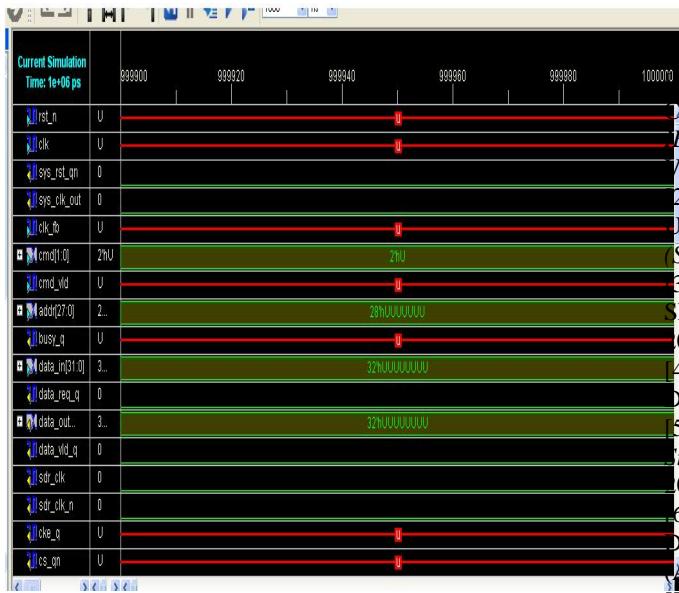


Figure 5. Result of our simulation.

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TABLE I. PERFORMANCE OF DDR3 CIRCUIT

Data width	32bits
table entrants	128K
Depth	512
Hash function	CRC-16
Lookup Frequency	100MHz
Registers	23,549
PLLs	1
DLLs	1

The above experimental results clearly validate the expected performance of the proposed custom purpose DDR3 controller architecture

VI. CONCLUSIONS

The design study shows that high-performance and large lookup table circuits can be implemented using low-cost state-of-the-art FPGA and DDR3 technology. The proposed DDR3 Hash-CAM circuit is prototyped for a 128K table entry and verified for a 2Gbyte DDR3 address space. Synthesis results presented in Table I show that a CAM circuit with 104bit wide and 512-entry can be built on standard FPGA devices at 100MHz, operating frequency. At 2GB at 1066MHzz, DDR2 and DDR3 are almost identical. Same with 4GB. DDR level separated from frequency doesn't seem to matter a bit.