Ultra-Low-Power Software-Defined Radio for LTE Wireless Baseband:
an embedded systems grand challenge

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Two Curves

Why Are These Curves Exciting?
- Incredible density mean true single-chip integration
- High volume on range of semiconductor designs
- New opportunities for processors

Why are These Curves Frightening?
- Moore’s Law enables high density, but how to we cope with complexity and rate of change?
- Many required functions, but few viable single-function chips
  - Silicon platforms must integrate or die:
- So many transistors, so little battery capacity
  - Steeper improvement in density than energy efficiency (new transistor types?)
A Grand Challenge Problem: LTE Handsets

Design Goals
• High data rates: 150Mbps DL/50Mbps UL
• High spectral efficiency with
  – Orthogonal Frequency Division Multiplexing
  – Multiple-Input Multiple Output
• Scalable bandwidth: 1.25MHz to 20 MHz
• Both Frequency-Division and Time Division Duplex
• All IP Networks

Implementation Needs
• Low silicon cost: <20mm² for digital PHY
• Low power: < 2mW/Mbps DL

Paradox: Reach performance and power goals while building a programmable system
Frame structure: 10ms = 10 subframes

Subframe structure: 1ms = 2 slots

Slot = 7 symbols
1 Symbol = 2048 tones → 1200 useful tones
1200 useful tones = 100 RBs x 12 tones
1 tone = up to 6b (64QAM)
Building Solutions to Solve Problems

- The raw material: more efficient processors

- A range of building blocks: baseband processors

- A solution architecture: LTE Reference Architecture
The Essential Building Block
Xtensa LX3 Extensible Dataplane Processor

Processor Controls
- Exception Support
- Exception Registers
- Trace Port
- JTAG Tap Control
- On-Chip Debug
- Data Address Watch Registers
- Instruction Address Watch Registers
- Timers
- Interrupt Control

Instruction Fetch / Decode
- VLIW (FLIX) Parallel Execution pipelines
- Base Instruction ISA Execution Pipeline
- Base Register File
- Base ALU
- Register Files Processor State

Optional Functional Units
- Designer-Defined Functional Units
- Designer-Defined Dual Load/Store Unit
- Data Load/Store Unit

Inst. Memory Management, Protection & Error Recovery
- Inst. Memory RAM
- Inst. Memory ROM
- Inst. Memory Cache

External Interface
- Xtensa LX3 Processor Interface Control
- Write Buffer
- PF Bridge

External RTL & Peripherals
- RAM
- DMA
- Device

System Bus
- AHB-Lite/AXI

Data Memory Management, Protection & Error Recovery
- Data RAM
- Data ROM
- Data Cache

Designer-Defined Queues, Ports & Lookups
- GPIO32
- QIF32

RTL, FIFO, Memory, Xtensa

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The Essential Automation
Xtensa Processor Generator

Complete Hardware Design
Source pre-verified RTL, EDA scripts, test suite

Processor Configuration
1. Select from menu
2. Explicit instruction description (TIE)
3. Automatic instruction discovery (XPRES)

Xtensa Processor Generator

Extensions
Use standard ASIC/COT design techniques and libraries for any IC fabrication process

Customized Software Tools
C/C++ compiler, Debuggers, Simulators, RTOSes

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Multiple Core Communication = Interconnect + Software

Software for Multi-core:

- Modeling at every level:
  1. Gate/RTL level
  2. FPGA netlist
  3. Pin exact
  4. Cycle accurate
  5. Instruction accurate

- Multi-core debug and analysis
- Communications APIs
- Complete DSP Libraries
- Solution stacks for LTE
  - L1 PHY
  - L2/L3 MAC, RLC

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Scalable platform for all design approaches

Deeply integrated Task Engines
(Xtensa performs specific tasks in HW flow)

Small, programmable DPU/DSP
(Xtensa control HW accelerators)

Function-Specific Light-Weight DSP
(Xtensa Foundation + DSP Module Extensions)

Baseband Engines DSPs, Multi-Standard SDR
Core 1: ConnX BBE16 Baseband Engine

Ultra-High Performance and Programming Ease

Architecture:
- 16 simultaneous 18bx18b MAC per cycle
- 8 way SIMD + 3 way VLIW
- Dual load/store unit (128b wide)
- Scalar CPU pipeline with general 32b RISC instructions
- Extended precision with guard bits
- 6 addressing modes

Performance:
- 16 multiply-adds per cycle
- Three 8-way ops per cycle
- 4 complex FIR taps / cycle
- 1 Radix-4 FFT butterfly / cycle
- 17GB/s memory bandwidth(@ 550MHz)
- 40-bit accumulation on all MAC operations without performance penalty
Core 2: ConnX SSP16 Processor

Processing soft bit streams – 3x more efficient than std DSP

**Data-types:**
- 10-bit and 8-bit Vectors
- 8-bit, 16-bit and 32-bit Scalars

**Performance:**
- 16 arithmetic operations per cycle
- 2 issue VLIW architecture
- ~10GB/s memory bandwidth

**Software:**
- Vectorizing compiler
- Multi-core debugger
- Fast, cycle-accurate simulator
- Energy models
- Function libraries and 3rd party cellular stacks
Core 3: ConnX BSP3 Processor
“Bit Stream Processing at minimal size and power”

Data-types:
• 8-bit, 16-bit and 32-bit Scalars

Performance:
• Dual Load/Store
• 3 issue VLIW architecture
• 600MHz in 45nm
• >4GB/s memory bandwidth

Software:
• C/C++ compiler
• Multi-core debugger
• Fast, cycle-accurate simulator
• Energy models
• Function libraries and 3rd party cellular stacks
Core 4: ConnX Turbo16
Programmable Turbo Decoding Engine

- Customized Processor based solution for LTE Turbo decoding at 150 Mbps
  - Matches throughput of hardwired RTL solution with similar area, power

- MAX-Log-MAP based decoding
  - Uses: $\exp(\log(a) + \log(b)) \sim \max(a,b)$

- 8-parallel windows based decoding
  - Two bits from each window processed per update
  - Interleaving and deinterleaving operations integrated with load/store operations to the local memories (Odd and Even D-RAM)

- Confidence estimator for software-based early-termination \(\rightarrow\) lower power
LTE Reference Architecture “Atlas”

- Demonstration of best practices for low-cost/low-power multi-core-based digital PHY sub-system
  - 100% processor-based – no RTL blocks
  - Highlights agile configuration of ConnX processors

- Proves efficiency of digital-PHY solution with processors
  - Reference architecture implements all blocks, memories and interconnect
  - Port of complete PHY software solution: mimoOn mi!MobilePHY™ 3GPP Fully Compliant LTE PHY

- 7 core solution for Cat 4 UE (150Mbps DL/50Mbps UL 20MHz):
  - 3 x BBE16
  - 2 x SSP16
  - 1 x BSP3
  - 1 x Turbo16
ATLAS-LTE UE

Typical utilization of cores: 60%
Wrap-up

1. Data-plane processors combine three characteristics
   - **Adaptable**: interface, instruction set, memory system automatically fit need
   - **Programmable**: proven instruction sets, compilers, libraries, SW stacks
   - **Efficient**: Rivals hardware area and power dissipation on complex problems

2. LTE handset challenge shows need … and possibility …for better solutions

3. Even bigger challenges ahead” - SOC complexity in 2010 = 0.0