2.4 GHz RF DOWN-CONVERSION MIXERS IN
STANDARD CMOS TECHNOLOGY

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ABSTRACT

In this paper, we have investigated several mixer structures including single-ended, single-balanced and double-balanced RF down-conversion mixers in 0.25 µm standard CMOS technology. The comparison of designed mixers with the recent literature shows significant improvement in some of the major performance parameters. The final differential double-balanced current-switching mixer shows a conversion gain of 6.1 dB, simulated noise figure of 8.3 dB and input 1-dB compression point of -8.3 dBm, consuming 5.6 mW at 2.4 GHz input RF and 250 MHz output IF frequency.

1 INTRODUCTION

The latest advancements in sub-micron CMOS technology have resulted in reduction of minimum channel length of the MOS device consequently increasing the unity current gain cut-off frequency to such an extent that now it is comparable to that of BJT and GaAs devices. Quite a few fully integrated CMOS transceivers for various applications have been reported in the literature targeting operating frequencies from 900 MHz to 2.4 GHz [1-4]. However, with the continuous scaling down of CMOS devices, the frequencies well into the upper microwave range (5-10 GHz) would soon be achievable.

The explosive growth of wireless services and consumption of wireless products has resulted in severe congestion in the usual 900 MHz frequency band for cellular applications. The commercially available 1900 PCS band will also soon be facing the same situation. The advent of Wireless LAN and Wireless Internet has further pushed the operating RF frequency towards 2.4 GHz, 3.5 GHz and 5-6 GHz unlicensed frequency spectrum. These system level requirements have directly been transferred to RF circuit designers demanding to evolve novel high frequency chip architectures and designs. RF down-conversion mixer, whose job is to convert high frequency signals to lower frequency spectrum where high performance digital and analog blocks (especially high Q filters) can be implemented quite efficiently, is one of the most important part of the system because its performance directly affects the overall performance of the whole front-end receiver.

2. CMOS RF MIXER TOPOLOGIES

Mixers are, generally, classified as active and passive mixers. The major difference between both classes is the amount of conversion gain they provide. Active mixers can achieve conversion gain and may require lower Local Oscillator (LO) power than their passive counterparts and essentially, are transistor circuits [5]. By virtue of their gain, active mixers reduce noise contributed by the subsequent stages of the receiver and are widely used in RF applications. Passive mixers, on the other hand, typically show conversion loss but exhibit excellent Intermodulation (IM) performance, high linearity and speed at the expense of high LO power requirements and find their applications in microwave and base station circuits. Active CMOS mixers are well suited to integrated circuit design because large LO drives, besides reducing LO-to-RF and LO-to-IF isolation, are difficult to realize in low voltage and low power environments. However, passive CMOS mixers followed by gain stages, have also been reported for fully integrated CMOS transceivers [4].

2.1 Single and Double-Balanced Current-Switching Mixers

Mixers based on the multiplication of two signals exhibit superior performance as they ideally generate only the desired mixing products. Both the RF and LO signals are applied at different ports resulting in high degree of inherent isolation among all the three ports. Down-conversion mixers usually employ LO short at the IF port to achieve optimum IM performance. The LO short is practically important for the active mixers because LO signal is typically larger than the RF signal and it is further amplified by the active devices. The mixer that accommodates a differential LO signal and a single-ended RF signal is termed as single-balanced mixer (Figure 1).

![Figure 1: Single-Balanced Current-Switching Mixer](image)

In Figure 1, the incoming RF voltage signal is first converted into a current signal and then multiplied in current domain. The FETs \( M_{LO1} \) and \( M_{LO2} \) are biased slightly above their threshold level. This results in the LO alternatively switching \( M_{LO1} \) and \( M_{LO2} \) on and off. Consequently, one LO transistor is always on, while other LO transistor is ideally off, keeping the RF transistor in saturation. Hence, the LO signal can be considered as a square wave consisting of odd harmonics of the LO frequency. The magnitude of this signal should be large enough to ensure complete switching of the differential LO transistors. The RF input current signal is multiplied by the odd-order harmonics of LO signal, resulting in mixing products to appear at the output IF port. The analytical description to derive a first order relation of the voltage conversion gain is given below.

If the switching LO signal is given by an ideal square wave \( LO(t) \) with an amplitude of \( \pm 1 \), to achieve an instantaneous switching action, then it can be represented by its Fourier series equivalent as shown in the Equation 2.1

\[
LO(t) = \sum_{k=1}^{\infty} \frac{\sin \left( \frac{k\pi}{2} \right)}{k} \cos(\omega_{LO}t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\sin \left( \frac{k\pi}{2} \right)}{k} \cos(\omega_{LO}t) \tag{2.1}
\]
The RF transistor is modeled by:

\[ \frac{\cos(\omega_{LO}t)}{\pi} - \frac{1}{3} \cos(3\omega_{LO}t) \]  (2.2)

The RF transistor is modeled by:

\[ I_dRF(t) = I_T + g_m v_{RF}(t) \]  (2.3)

where \( I_T \) is the DC tail current. Taking \( v_{RF}(t) \) as a sinusoidal signal \( v_{RF}(t) = V_{RF}\cos(\omega_{RF} t) \)

The mixer current-switching action can now be expressed by combining Equations 2.2 and 2.3

\[ i_{o}(t) = \left( I_T + g_m V_{RF}\cos(\omega_{RF} t) \right) \left[ \frac{4}{\pi} \cos(\omega_{LO} t) - \frac{1}{3} \cos(3\omega_{LO} t) \right] \]  (2.4)

Equation 2.4 can be written as

\[ i_{o}(t) = \frac{4}{\pi} I_T \cos(\omega_{LO} t) - \frac{1}{3} I_T \cos(3\omega_{LO} t) \]

\[ + \frac{2}{\pi} g_m V_{RF} \cos(\omega_{RF} - \omega_{LO} t) + \cos(\omega_{RF} + \omega_{LO} t) \]  (2.5)

In Equation 2.5, the second term in square brackets is the actual mixing term, where we have both the down-converted and up-converted sidebands present simultaneously. The output load, as shown in Figure 1, is \( R_L \), therefore output IP voltage after filtering out the up-converted sideband is given by

\[ v_{IP}(t) = \frac{4}{\pi} R_L \left( I_T \cos(\omega_{LO} t) - \frac{1}{3} I_T \cos(3\omega_{LO} t) \right) \]

\[ + \frac{2}{\pi} g_m R_L V_{RF} \cos(\omega_{RF} - \omega_{LO} \frac{1}{2}) \]  (2.6)

where \( \omega_{IF} = \omega_{RF} - \omega_{LO} \) is the fundamental down-converted frequency. Equation 2.6 is specific to a single-balanced mixer where the first term gives the LO leakage or feedthrough at the IF output. We can calculate the voltage conversion gain of the single-balanced mixer as output IF amplitude divided by the input RF amplitude i.e.

\[ G_v = \frac{V_{IF}}{V_{RF}} = \frac{2}{\pi} g_m R_L \]  (2.7)

The analysis for single-balanced CMOS Current-Switching (CS) mixer can directly be applied to a double-balanced CS (Gilbert) mixer as the double-balanced structure is just a combination of two single-balanced structures connected in parallel i.e. 180° out of phase for the LO signal while in-phase for the RF signal. Hence, LO signal feedthrough at the IF output is ideally suppressed completely as output port acts as a virtual AC ground for LO signal. In addition, all the even-order harmonics of the mixed output are cancelled out, resulting in better 1-dB compression and third-order intermodulation intercept point, consequently better dynamic range and linearity response. The only drawback is that being a combination of two single-balanced mixers, double-balanced mixer takes twice as much the current, however, conversion gain remains the same. Figure 2 shows the basic configuration of double-balanced current-switching mixer.

2.2 Single Cascode, Single and Double-Balanced Cascode Mixers

In contrast to current-switching mixers where we have two types of configurations, there are three types of CMOS dual gate or cascode mixer structures. The first and the simplest is a single cascode mixer. The other two types i.e. single-balanced and double-balanced cascode mixers are just the combination of two and four cascoded structures respectively, which progressively helps in achieving a LO short at the output IF port without using passive LO rejection circuitry.

Figure 3 shows a simple CMOS single-cascode mixer. The upper transistor has several effects on the mixer operation. Its primary use is to control the small signal transconductance of the lower device and therefore, the RF gain of the device, making it useful as a mixer [6]. In addition, this configuration is well suited to CMOS technology since the drain and source of the two cascoded devices can be shared reducing capacitance at the common junction. It has been proved that the usual mode of operation is the one in which LO signal is applied to the top gate (\( M_{LO} \) in the Figure 3) and the RF signal is fed to the lower gate [6-7]. This not only improves the RF-to-IF isolation but also enhances the linearity by allowing the use of standard port matching techniques for the RF signal. The applied LO signal modulates the common node voltage (node \( X \) in Figure 3). The modulated node is the drain of \( M_{RF} \) resulting in the mixing of LO and RF signal. The gate-source voltage of \( M_{RF} \) is approximately constant because the RF signal is usually very small and the modulated drain-source voltage swings \( V_{DS} \) in and out of linear and saturated regions of operation over the LO cycle. Frequency mixing occurs due to the modulated transconductance \( g_m \) and drain-source conductance \( g_{ds} \) of \( M_{RF} \) and \( M_{LO} \) remains in current saturation over most of the LO cycle, thus, it operates, simultaneously, as a source-follower amplifier for the LO and a common-gate amplifier for the IF. This gate should be grounded at the IF.
harmonic, which can be done by placing a series resonant structure, tuned to IF. The drain of M_{LO} should also be shorted to ground at the LO frequency. This short circuit keeps the drain voltage constant and guarantees that M_{LO} remains in saturation over most of the time [6].

The disadvantages of single cascode mixer are the inevitable use of passive components for LO and IF rejection making it less useful in low frequency RFIC implementation. The cascode mixer can be implemented as a single or double-balanced structures, as stated above, which helps in achieving LO rejection without using passive components.

3. SIMULATION AND MEASUREMENT RESULTS

The mixer structures are designed in 0.25 µm standard CMOS technology (f_t ≈ 30 GHz) using spectreRF simulator in Cadence environment. Layouts of the designs are performed using Cadence IC design tool Virtuoso and designs are fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) through Canadian Microelectronics Corporation (CMC).

In order to evaluate the effects of different CMOS mixer structures and topologies, it is necessary to design and optimize one configuration as a reference design and compare its performance with other topologies and structures with respect to the major performance parameters like conversion gain, linearity and noise figure. In this work, single-balanced CMOS current-switching mixer is chosen as a reference configuration because of its relatively simple structure and the fact that more complex structures like double-balanced current-switching mixers are just the combination of two single-balanced mixers.

No matching networks are provided for RF and LO ports as the designed mixer will eventually be employed as a part of whole front-end system, where corresponding matching between different blocks is more important than matching down to 50 Ω. However, output buffer is placed at the IF output for ease of measurement procedure, which also provides good output matching (output return loss greater than industrial standard of 10 dB).

The design is optimized to achieve moderate conversion gain as it is usually undesirable for active mixers to have large conversion gain because of the trade-off between conversion gain/noise figure and dynamic range of down-conversion mixers. This trade-off comes from the fact that higher conversion gain tends to overload the output of the mixer, resulting in lower input P_{1dB}. Also, to increase the linearity, the current flowing through the device needs to be increased but too much current tends to degrade the noise figure of the mixer due to the higher gate-source capacitance. The noise figure and input P_{1dB} are also simulated for the optimized design and results are provided in the following discussion.

During simulations, it was found that the simulator spectreRF shows the output power in terms of dBV, instead of dBm. The relation between dBV and dBm, when the ports are matched to 50 Ω is given as follows:

\[
P_{dBm} = 10 \log \left( \left( \frac{P_{dBV}}{1000mW} \right)^2 \left( \frac{1}{50} \right) \left( \frac{1000mW}{1mW} \right) \right)
\]

\[
\Rightarrow P_{IF(dBm)} = P_{IF(dBV)} + 10dB
\]  

(3.1)

i.e. the power in dBV (at 50 Ω) is 10 dB less than the power expressed in dBm, therefore, to get the output power in dBm, 10 dB has to be added to the power given in dBV. However, the input power P_{RF} is specified in dBm in the simulator i.e. no correction is needed in input power and therefore, in the simulated input P_{1dB}. This 10 dB correction is shown in the P_{IF} vs. P_{RF} and the P_{IF} vs. P_{LO} plots as a correction note indicating the post-simulations normalization.

![Figure 4: Output IF Power vs. Input RF Power](image)

![Figure 5: Output IF Power vs. LO Power](image)

![Figure 6: Frequency Spectrum of 2.4 GHz CMOS Mixer](image)

Figure 4 and 5 show the simulation and measurement results of single-balanced current-switching mixer. Figure 6 shows the frequency spectrum of mixer, where we can observe the presence of LO feedthrough at the output port. However, RF signal is completely rejected at the output port, as suggested by the IF voltage equation (Equation 2.6). Other mixer structures i.e. double-balanced CS mixer, single and double-balanced cascode mixers are also designed using the same device sizes obtained from the optimization of single-balanced CS mixer.

Table 1 gives the comparison of simulation and measurement results for all the designed mixers.
The conversion gain numbers are generally in agreement with each other except in the case of single-cascode mixer where there is about 40% variation. The input $P_{1dB}$ numbers are not matching well, which is due to the difference in the amount of LO power applied (not shown) in simulations and measurements. Also, the error can be attributed to the fact that the device models in CMOS technology are optimized for the digital designs. The models, not optimized for high frequency RF designs, might result in inaccuracies in the simulations.

Figures 7 and 8 gives the comparison of conversion gain and input $P_{1dB}$ against power consumption for CMOS Gilbert mixers reported in recent literature and this work.

### 4. CONCLUSIONS

Several single-ended, single-balanced and double-balanced CMOS RF mixers, working at 2.4 GHz input RF frequency are designed and fabricated. The comparison of designed mixers with the recent literature shows significant improvement in terms major performance parameters like power consumption and noise figure with comparable conversion gain and linearity (Figures 7 and 8).

In essence, it has been shown that CMOS technology, although considered as a digital technology, has started showing good RF performance as the device channel length is getting smaller and smaller. This offers a great opportunity of putting DSP, analog back-end and high frequency RF front-end on the same chip using a standard CMOS technology, resulting in lower power consumption and manufacturing cost.

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### 6. REFERENCES


