History of Some Early Developments in Ion-Implantation Technology Leading to Silicon Transistor Manufacturing

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Invited Paper

Ion implantation of dopant impurities to form p-n junctions and other doped regions in silicon transistors has evolved from an experimental curiosity in solid-state physics to become a dominant technology in today's integrated circuit manufacturing. This paper traces the key inventions and early developments in ion beam doping concepts from the early 1950's through the 1970's as they were applied to the development of metal–oxide–semiconductor (MOS) and bipolar transistors. Early on, scientists were fascinated with possible applications of radiation damage resulting from ion bombardment of semiconductors for building novel devices with room-temperature processing or, at most, maximum heating temperatures of a few hundred degrees Celsius. As a result, the early work initially overlooked the real potential of the technology for providing a highly controlled means of substitutional impurity doping in combination with high temperature annealing above 800° C. Subsequently, a number of key researchers contributed to the knowledge base surrounding the penetration of energetic ions into semiconductors. However, the true potential of ion implantation would be realized by more device-oriented engineers driven by design and manufacturing issues who looked for ways of applying and integrating ion implantation with conventional transistor manufacturing methods. Ion implantation allowed for good lateral and vertical junction position control, which were critical elements as both device dimensions and patterned feature tolerances were reduced. Ion implantation, high-temperature annealing, and self-aligned silicon gate technology fueled new process technologies in MOS devices such as arsenic source/drain doping, the ability to tailor threshold voltages in both enhancement and depletion transistors, and lightly doped drain extensions. In bipolar technology, ion implantation would make possible tight control of base-region doping and reduction of parasitic resistances, and would enable the use of arsenic emitters for high-frequency applications of discrete transistors as well as advanced, high-speed integrated circuits.

Keywords— *Bipolar transistors, ion implantation, MOSFET's, radiation damage-induced junctions, self-aligned gate, silicon doping, threshold voltage adjustment.*

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I. Introduction

Semiconductor chip technology has undergone dramatic advances over the past 30 years, enabling the manufacture of high-density integrated circuits (IC's) with millions of transistors on a single die. Each new generation of microprocessor or memory chips has many technological challenges that must be addressed before the fabrication processes are deemed to be manufacturable [1]. These advances in technology have evolved over time, however, and it is unusual today to see a revolutionary new technology introduced into the production line unless it can be integrated into present production processes, is cost effective, and is absolutely required to meet process or device targets. Engineers must also consider the huge new equipment and time-to-market costs to implement the new technology.

Ion implantation of doping impurities to form p-n junctions and doped regions in silicon transistors was one such revolutionary process from the mid-1960's through the mid-1970's, which is the period of time covered in this paper. The basic idea of ion-implantation doping as we know it today involves bombarding silicon with high-energy group III or V doping impurity ions, which penetrate into those regions where it is desired to change the local electrical conductivity or/and the conductivity type (n- or p-type). Upon heating the silicon sufficiently, each ion-implanted impurity atom replaces a silicon host atom. The doping impurities are approximately the same size as silicon, but they have a different number of valence electrons, leaving implanted regions either electron rich (n-type) or electron deficient (p-type). The major advantage of this technology is the ability to control and reproduce the number of dopant impurity atoms introduced into the semiconductor as well as both the depth and lateral locations of these impurities.

Prior to the invention of planar process technology in 1959 by Hoerni of Fairchild Semiconductor [2], junction alloying was being phased out in favor of impurity diffusion

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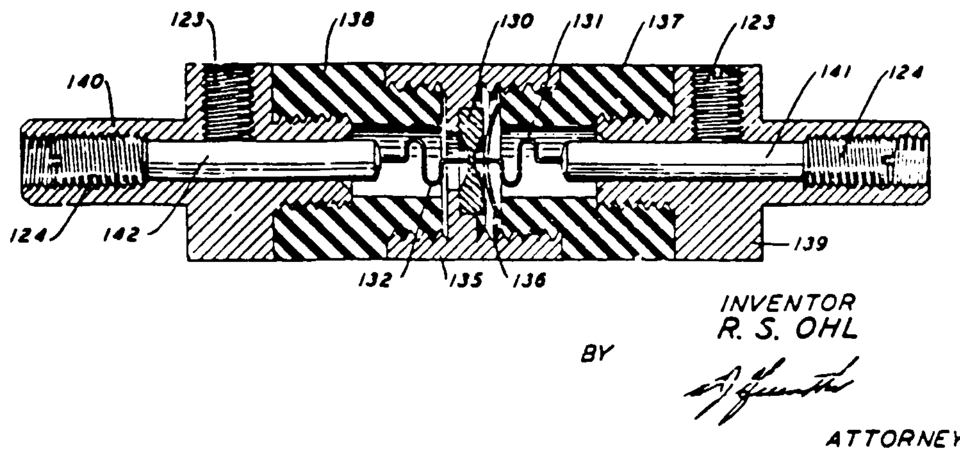


Fig. 1. Point-contact bipolar transistor by Ohl, in which either the emitter or collector contacts were subjected to an ionic bombardment process to improve surface electrical stability and to increase electron emission from the emitter (after [7]).

for creating p-n junctions The idea of using diffusion techniques employing chemical dopant sources to form p-n junctions was disclosed in a 1952 patent by Pfann [3], and the teachings of this patent in combination with planar process technology became firmly entrenched in manufacturing transistors in the early 1960's. As a result, the introduction of ion implantation into product manufacturing had to be "sold" with a similar level of compelling conviction that one would face in today's $150 billion worldwide IC market [4].

The introduction of ion implantation into the manufacturing of transistors and IC's in the 1970's was predicated upon advances in ion source and implantation-system technology, advances in the understanding of implantation annealing of semiconductors, and unique device applications of the technology that would put ion implantation into manufacturing facilities and make it available to process engineers. Progress was also made possible by a number of key inventions and scientific discoveries in the 1950's and 1960's. Ion-source and ion-beam technology evolved from nuclear physics research into "positive rays" and accelerator development for isotope separation [5]. In parallel efforts, investigations into the bombardment of semiconductors, radiation effects, and doping effects led to studies of materials' issues such as ion ranges and distributions based upon fundamental contributions from Bohr [6]. And in the early 1950's, several patents were issued that envisioned the use of ion bombardment in the fabrication of semiconductor devices, the first being Ohl's patent filed January 31, 1950 [7].

A. Key Inventions

Ohl, employed by Bell Laboratories, described the fabrication of a point-contact bipolar transistor, shown in Fig. 1, in which either the emitter or collector contacts were subjected to an ionic bombardment process to improve surface electrical stability and to increase electron emission from the emitter. Typically, the recommended bombarding ions included air, oxygen, hydrogen, nitrogen, helium, argon, carbon monoxide, and even chloroform. Ohl taught that these were ions of significant impurities, which were thought to enter the crystal surface and function in a manner such that "the impurity changes the number of electrical carriers present in the material thereby changing its electrical characteristics."

In hindsight, Ohl's explanation was wrong and may have misdirected workers in the field. As a result, others followed his lead with similar studies. Other early patents that discussed the application of ion bombardment or ion injection in the fabrication of semiconductor devices included the following.

1) Lark-Horivitz *et al.* at the Purdue Research Foundation [8] (filed May 9, 1950) described photoelectric devices and "a plurality of regions of P-N high resistance barrier layers in a unitary body of germanium" utilizing "charged nucleons." This patent demonstrated the use of a "plurality of strips of material 6 suitable for absorbing charged nucleons," thus introducing the concept of masking, as shown in Fig. 2.
2) Sziklai's patent filed on January 21, 1953 [9] and assigned to RCA described "a unitary (integrated) cascade semiconductor amplifier comprising regions of p-type and n-type conductivity material adapted to operate as emitter, collector and base electrode regions, whereby the p-type layers are created by bombardment by charged nucleons," as shown in Fig. 3.

Shockley at Bell Laboratories filed a patent on October 28, 1954 [10], that is widely credited with introducing the concept of implantation doping. Shockley disclosed the process of ion bombardment with group III or group V ions with sufficient energy to penetrate the surface of a semiconductor in order to affect conductivity changes inside. This is in contrast to only surface treatment, as suggested by Ohl's patent. Thus, Shockley was the first to appreciate the fact that the depth location of the implanted doping impurities could be determined by the energy of the ion beam. From a historical view, this observation was actually the first

March 4, 1952 K. LARK-HOROVITZ ET AL 2,588,254
PHOTOELECTRIC AND THERMOELECTRIC DEVICE
UTILIZING SEMICONDUCTING MATERIAL
Filed May 9, 1950

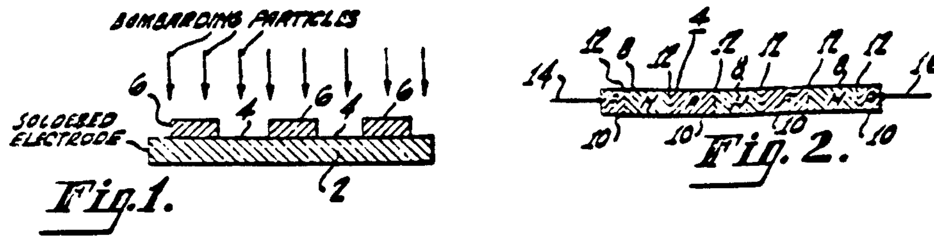


Fig. 2. Diagrammatic illustration from Lark-Horovitz of one method of preparation of a body of germanium semiconductor material for creating alternating n-type and p-type regions by masked particle bombardment (after [8]).

Feb. 21, 1956 G. C. SZIKLAI 2,735,948
MULTIELEMENT SEMICONDUCTOR DEVICES
Filed Jan. 21, 1953

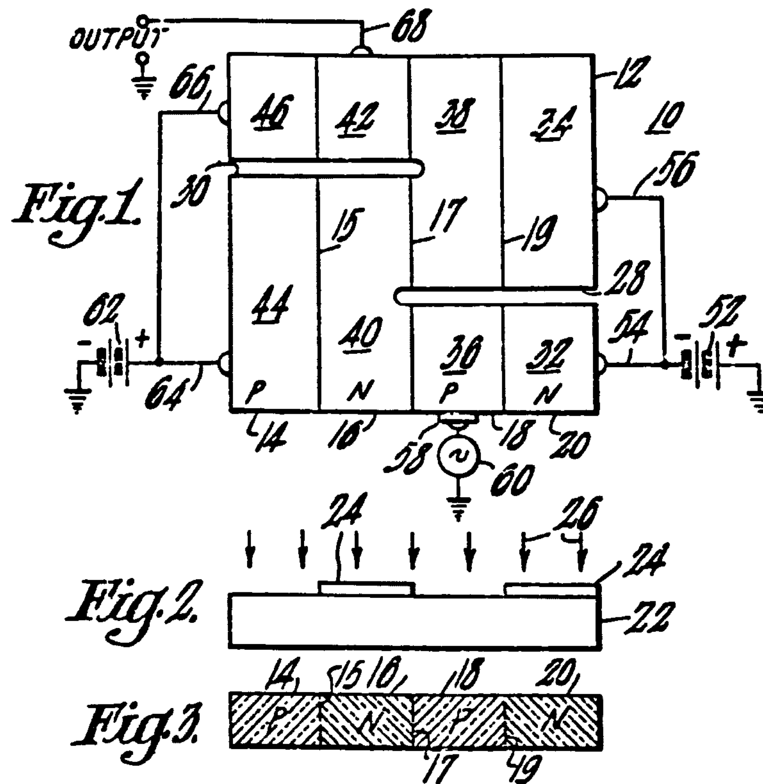


Fig. 3. Diagram from Sziklai's patent showing an IC semiconductor amplifier comprising regions of p-type and n-type conductivity material adapted to operate as emitter, collector, and base electrode regions, whereby the p-type layers are created by bombardment by charged nucleons (after [9]).

known useful feature of ion implantation—the ability to place impurities in the semiconductor where you wanted them.

Shockley also introduced the concept of heating the ion-bombarded semiconductor to a temperature of 400°C to repair the radiation damage in the bombarded regions. Despite the recommended annealing temperature, which was actually a factor of two too low, this disclosure represented amazing insight and revealed the secrets to success in applying ion implantation to device fabrication. It would take another ten years, however, before the semiconductor physics community would understand the significance of Shockley's patent and then improvise upon it. An example from Shockley's patent of an n-p-n transistor structure fabricated by ion implanting the p-type base layer with boron in germanium is shown in Fig. 4.

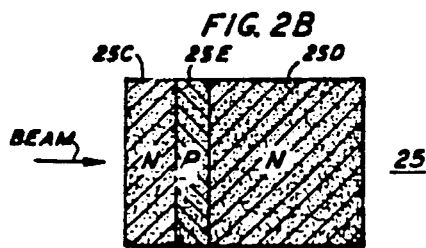


Fig. 4. Diagram from Shockley's patent of an n-p-n transistor structure fabricated by ion implanting the p-type base layer with boron in germanium. This was the first published suggestion of chemical doping by ion implantation (after [10]).

It is not widely known, but four months prior to Shockley's patent filing, J. W. Moyer at General Electric (GE) [11] had filed a disclosure with the U.S. Patent Office that described a method of "forming and directing a high velocity beam of . . . ionized vaporized [activator] element . . . upon a semiconductor crystal." The activator element was described as being an acceptor or donor type, and examples of donor-type elements were given as arsenic and antimony. The goal of the invention was to form graded p-n junctions at the limit of the ion penetration from the crystal surface. Moyer also taught that the bombarded crystal should then be heated to 500°C for 12 h. Moyer's patent was issued 15 months after Shockley's patent. But by then, the semiconductor world had already been introduced to the notion of p-n junction formation as well as transistor formation using ion beams comprising doping elements, and Shockley would be given most of the credit for this discovery.

B. Ion Source Developments

Similar progress was being made in the time period of the mid-1950's to early 1960's in the technology of ion sources [12]. Low-current, spark-gap ion sources, which had been around since 1900, and surface ionization sources discovered in the 1920's gave way to dc-plasma sources and accelerators with mass selection. As device applications grew and their commercial success became evident, the driving force for advanced ion-implantation systems emerged, as did improved understanding of the materials physics of bombarded semiconductors. These parallel developments are diagrammed in Fig. 5 as key milestones and themes in the development of ion-implantation technology. It is clear hindsight that the evolution of modern-day implantation systems has occurred in response to semiconductor device needs. It is also beyond the scope of this paper to chronicle the development of suitable ion beam systems. However, at various times in history, progress in the application of ion implantation to semiconductors was hampered by the unavailability of good sources of specific ions, such as boron in the early to mid-1960's. Or, on the flip side, many times, semiconductor scientists would study ion bombardment with whatever ion source they had available to them. As we will see, at one point in time, it mattered little which ion was chosen for bombardment, since similar results were usually obtained.

C. Historical Perspective and Scope of this Contribution

The recognition of the importance of Shockley's and Moyer's patents would take some time, since the semiconductor physics community was quite interested in studying conductivity-type changes in ion-bombarded semiconductors caused by radiation damage. There was little work, if any, on annealing processes that would place implanted group III and V elements into normal lattice sites in the semiconductor where they could act as acceptors or donors, respectively. And neither Bell Labs nor GE followed up with research and development (R&D) efforts to exploit ion implantation. It was this author's understanding and experience that at Bell Labs, this was a management decision. Ion implantation had to be sold to management over standard diffusion processing for p-n junction formation. This was in response to the need within Bell Labs to support the manufacturing operations at Western Electric with fabrication technologies, like standard diffusion, which were easier to implement and had a better chance of solving near-term problems. In fact, an ion-implantation group would not be set up at Bell Labs until the mid-1960's, ten years after Shockley's patent was filed.

Meanwhile, other groups at Hughes Aircraft Company, Stanford University, Chalk River Nuclear Laboratories, Rockwell, Aarhus University, etc. would lead the effort to establish a scientific basis for ion-implantation technology, including models for calculating the penetration range statistics of implanted ions. It is beyond the scope of this paper to review all of these outstanding fundamental contributions in ion-implantation research. An excellent review of the work on range distribution theory and experiments was published in the PROCEEDINGS OF THE IEEE in 1968 [12] by Gibbons, who headed a pioneering activity at Stanford University. A second review article by Gibbons appeared in this PROCEEDINGS in 1972 [13] and described the work on ion-implantation damage production and annealing up to that time. Rather, the present paper focuses primarily on the activities of those engineers and scientists who needed to build transistors within the constraints of practical fabrication methods. These workers not only were enabled by the research results of the above-named groups but they also depended on the development of more practical ion sources and ion-implantation systems. Device-oriented workers also paved the way for the practical use of ion implantation by exploring the critical area of high-temperature annealing of implanted semiconductors. This is the story of how the true potential of ion implantation would be realized through transistor manufacturing, which required improved methods of producing devices with better control and improved

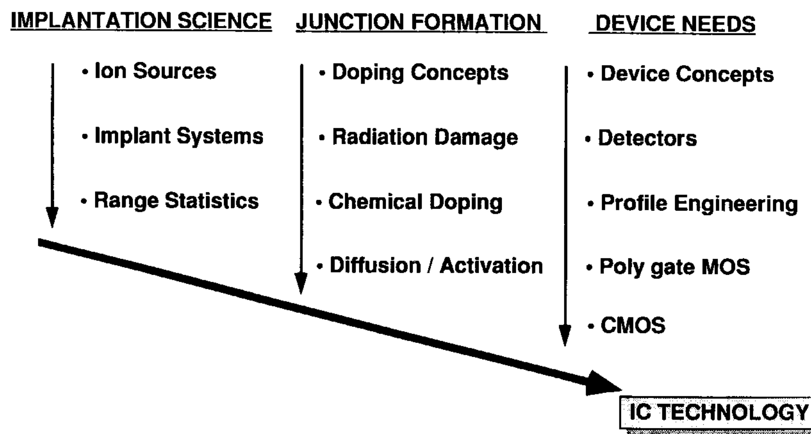


Fig. 5. Historical trends and milestones in the areas of implantation science, junction formation, and semiconductor device requirements, which together ultimately drove the establishment of ion implantation as an important technology in processing integrated circuits.

performance within the framework of existing fabrication methodologies.

In the next section, we will describe the period in the early to mid-1960's when there occurred a great surge in research activity involving "ion injection" into semiconductors for either new device applications or just to tap into newly available federal funding. Once the concept of chemical doping by ion implantation was realized, inventors began filing patents on new device fabrication methods employing ion implantation, some of which have become the cornerstones of today's semiconductor industry. We will describe these key inventions in the following section and describe some of the important activities in both unipolar and bipolar transistor development.

II. The Ion Beam Doping Controversy

Early investigations [14]–[16] of doping effects resulting from ion bombardment of semiconductors were concerned with radiation-induced damage centers. The ions chosen in such studies would not normally have been expected to demonstrate chemical doping effects. The prevailing theory was that bombardment damage affected the Fermi level in the semiconductor, causing it to move toward the center of the band gap. As a result, bombardment damage itself produced a doping effect that could change the inherent conductivity type of a semiconductor associated with the background doping. Thus, the dream of using this new ion-bombardment effect to construct various junction devices propelled researchers to bombard many types of semiconductors with a wide variety of ions from inert gas ions to rare earth species.

A. Radiation Damage-Induced Junctions

Thornton and Hanley [16] constructed point-contact Si diodes by oxygen bombardment. The normally observed reverse breakdown voltage of less than 5 V was raised to 130 V by oxygen bombardment. The authors attributed this result to the bombardment-induced Fermi-level shift as well as to an effective change in the chemical composition at the surface of the Si. Other studies of point-contact structures in Ge were made by Cussins [17] using bombarding ions of mass from H and B to Sb. Cussins reported that layers of p-type conductivity were formed, but upon heating the bombarded germanium to 500°C, the p-type layers disappeared. Cussins concluded that the effect of bombardment was "to produce defects which can act as acceptor impurities," and the effect was almost independent of the type of ion. This result would lead one to conclude that heating the semiconductor after ion bombardment was the wrong thing to do.

From 1956 to 1961, the ion-bombardment field was dormant. The Shockley and Moyer patents had been issued, but there was no apparent follow-on work at GE or Bell Labs. In a paper appearing in 1961, Rourke *et al.* [18] described ionic doping by "impregnating" Si with group III or V elements to achieve heavy doping concentrations of 10^{18} atoms/cm^3 in a shallow layer near the surface of an Si target. This work seemed to stimulate the application of ion bombardment in fabricating the first practical device based upon the chemical properties of the implanted ions. Alvager and Hansen [19] built a particle detector in which they implanted phosphorus ions at 10 keV into 9000 Ω-cm, boron-doped silicon crystal. Doping with group III and V elements at higher energies, 1 MeV, was reported in 1962 by King and Solomon [20].

H. Strack [21] at the Shockley Laboratory in Palo Alto, CA, proposed in 1963 to use ion bombardment in a hollow-cathode phosphine or diborane gas discharge apparatus operating at up to 920°C to selectively form high-doping impurity regions. In 1964, in the same laboratory, Amadei and Goetzberger [22] proposed, "The technique may have

application in the diffusion of very high frequency transistors." They apparently applied this method to the fabrication of a power transistor structure, which is shown in [22]. This plasma discharge doping method would reappear in the 1990's as plasma immersion ion implantation, which today holds promise for fabricating ultrashallow source and drain junctions for metal–oxide–semiconductor field-effect transistors (MOSFET's).

As an aside, Amadei and Goetzberger [22] also proposed the use of molybdenum masks over oxide on silicon to protect the underlying oxide from bombardment damage. This was an early concept that would be useful later in self-aligned-gate MOS technology, where a metal or polycrystalline silicon film over a gate oxide would be used to mask the implant and, therefore, establish the source and drain regions of a MOSFET. Thus, the underlying, sensitive gate oxide would be protected from ion bombardment by the thick gate material. The invention of the self-aligned-gate process will be discussed in Section III of this paper.

In spite of the promising work reported on dopant impurity ion bombardment, it still appeared that few had caught on to the fact that heating the crystal to normal diffusion temperatures (above 800°C) was necessary to achieve the real advantage of the technology. The solid-state community was enamored with the idea of shooting ions into semiconductor crystals to study radiation effects or to form novel, low-temperature fabrication processes for devices. However, a more pragmatic approach was being pursued by workers seeking to fabricate devices. For example, in 1963, Ferber [23] at Westinghouse reported that junctions formed by the bombardment of p-type silicon with B ions showed the best forward and reverse current–voltage characteristics after annealing at 300–400°C. However, Ferber reported that "the reverse characteristic of the junctions grew progressively worse with annealing, almost all diode characteristics having disappeared after annealing at 600°C." Ferber's conclusion was that while ion bombardment of B probably formed doping centers in the Si, a lot of other ions such as H and ionized B_2H_6 molecules from the ion source were being implanted also, which contributed to radiation damage. Thus, it would be required to form a mass-analyzed B^+ ion beam to get better results, where doping effects could dominate over radiation effects. This observation certainly was not the only recognition that a mass-analyzed beam would be required for p-n junction formation [18], but it was representative of the sea change in thinking in the early 1960's regarding ion beam doping for fabricating devices. In other laboratories, however, alternative schemes for creating ion-implanted devices were already under way.

B. Sodium Ion Injection

North American Aviation, Inc. (NAA) was winding down its work on ion propulsion engines in the early 1960's for the federal government's space program and began turning their cesium ion beams on semiconductor targets for new funding opportunities. A patent application filed in September 1963 by Dr. J. O. McCaldin [24] of NAA claimed that it was possible permanently to alter the electrical characteristics of Si by bombarding with ions of Na, K, Rb, and Cs at target temperatures of 300–700°C. The justification for using alkali metal ions was that such elements preferred to occupy interstitial positions in the Si lattice and, therefore, would become donors. As a result, the users of this invention would not have to be strapped with the difficulties associated with the use of substitutional type impurities for achieving desired electrical properties, which "requires heating to high temperature . . . and usually results in degrading the performance characteristics of the semiconductor." In spite of these claims, however, such an "undesirable" method would eventually become adopted by all of the semiconductor manufacturers in the world.

Sodium ion injection in Si was pursued for several years in the fabrication of diodes, transistors, and resistors [25] before it went away. In an invention application filed in October 1964 [26], a method was claimed for permanently inducing a change in the electrical characteristics of a silicon dioxide layer over silicon by bombarding the heated silicon dioxide surface during bombardment by space-charge-inducing ions such as Na. However, it was discovered a short time later, in 1965 [27], as well as in many semiconductor companies that the inadvertent introduction of Na into one's oxides produced unwanted electrical instabilities in MOS devices, severely degrading their performance. This was yet another example of an interesting idea with not-so-good implications in device fabrication.

Perhaps the most important result from McCaldin's work was the idea of heating the target wafer during ion implantation. When it became obvious that implantation damage was undesirable, the idea of heating the substrate during implantation was viewed by the scientific community with a degree of excitement. Workers were now looking for ways of avoiding implantation damage, and it was believed that the annealing out of postimplantation damage would become harder as more damage was produced. Thus, the concept of "hot" implantations promised continuous damage annealing as the damage was being formed, resulting in less damage at the end of the implant. After experimentation by several labs, however, it was determined that the postimplant damage remaining after hot implants was quite stable and was even more difficult to remove by postimplant annealing. Eventually, it would be found that room-temperature implants or implants performed into wafers cooled to liquid nitrogen temperatures produced better results, especially if the implantation dose was sufficiently high to render the wafer's surface region completely damaged (amorphous), i.e., damage of sufficient magnitude to cause complete removal of crystalline order. Modest anneals at 500–600°C would cause the amorphous layer to regrow back to its crystalline state with relatively low damage density in the regrown layer and high levels of electrically active doping impurity concentrations [29]. The idea of hot implants would survive for some time in certain MOS processes for fabricating aluminum-gate transistors where only implantation anneals below 500°C could be tolerated.

C. Ion Channeling

By 1964, work was under way to use postimplantation annealing to reduce the implantation damage to make the doping effects of the implanted atoms dominate. It was believed that by suitable annealing one could return a bombarded crystal to a nearly perfect state. But what annealing temperature was adequate? There was interest in keeping ion implantation a relatively cold process compared to standard diffusion processes for forming p-n junctions at temperatures above 900°C. This interest was kindled by J. Lindhard's discovery [30] of ion channeling in open crystal directions in single-crystal substrates, which resulted in relatively small amounts of target damage, since only a few collision cascades would occur between a channeled ion and the substrate's atoms. This opened up research into single crystal targets, with the goal being to produce lower implantation damage, which required low annealing temperatures to produce high-quality p-n junctions.

Ion range distributions in single-crystal substrates are different from those in amorphous targets as a result of the possibility that ions can channel along open directions, which occur when the ion beam is aligned with low-index crystallographic directions [12]. Ion trajectories in the crystal could then occur along channels or open directions in the lattice in which few encounters with target nuclei would take place. The early ideas on channeling were contributed by Lindhard [30], whose brilliant theoretical calculations showed how to calculate the critical angles for channeling, which would allow ions to enter open channeling directions of a single-crystal substrate. This work was then confirmed experimentally by K. O. Nielsen's group at Aarhus University. While ion channeling received a lot of attention at this time, however, little practical use would ever be made of it, despite the efforts of a few workers who envisioned innovative device structures such as implanted bipolar transistors with deep buried collectors produced by ion channeling. The basic problem was the poor reproducibility of the channeled impurity profiles, which a number of Japanese semiconductor companies would discover only after significant effort.

Based upon the channeling work at Aarhus University, J. A. Davies, who spent a sabbatical at Aarhus, and his group at the Chalk River Nuclear Laboratories published a paper about some of the problems in channeling ions in semiconductors and also how to avoid channeling all together [31]. They found that very thin surface layers of silicon dioxide could drastically affect the channeled-ion profile of 40-keV Xe in a <110> silicon crystal, causing changes in ion penetration depths by a factor of two when a 200-Å oxide film was on the surface. Davies also demonstrated that by tilting the ion beam by 7° off of the normal to a (110) surface, ion channeling could be practically eliminated. These results are shown in Fig. 6. This result would subsequently be used successfully by the majority of the semiconductor industry, who have practiced 7° implantations to the present time in order to control implanted-impurity penetration depths in silicon wafers.

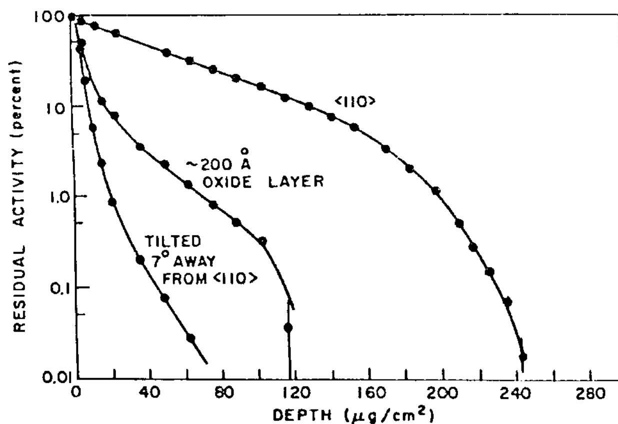


Fig. 6. Experimental illustration of the effect of beam misalignment on the channeling penetration of 40-keV Xe^{125} in <110> Si. For the curve closest to the vertical axis, the crystal was tilted so that the beam entered the silicon at 7° off of the normal direction, which compares with the deepest curve where the beam entered the crystal at 0°. A thin surface oxide film also reduced the channeling effect for a 0° implant (after [31]).

The 1964 Aarhus Conference on Electromagnetic Separators and Their Applications held in Aarhus, Denmark, was a gathering of all the key people working on ion sources, ion beams, mass separation techniques, and applications of ion beams to solid-state physics and nuclear physics. The emphasis of most talks on ion bombardment of semiconductors was on the use of low-energy (20 keV) channeling implants for minimizing substrate damage. Of the 76 talks presented, only two dealt with the engineering applications of ion beam technology to the fabrication of silicon devices. And these two talks actually appeared to be misfits in a conference dominated by basic scientific concepts of radiation damage effects in semiconductors.

D. Ion-Implantation Doping

At the Aarhus Conference, Manchester *et al.* [32] reported on silicon doping by directly implanting P and B to produce electrical junctions. The ion source was a 24-in radius calutron that produced beams of B^+ or P^+ ions. The paper used the phrase "ion implantation," and it revealed a bipolar transistor that had been completely fabricated by electron and ion beam technology. This device, shown in Fig. 7, was processed without exceeding a 200°C substrate temperature, except for a final 700°C anneal for 10 min. The authors claimed also that it took only 2 1/2 min to fabricate 60 such transistors. Extrapolating to the present, with such a process it would take 92 days to fabricate a single Pentium microprocessor chip containing more than 3 million transistors. However, the authors did not reveal whether or not transistor action was ever observed. Nevertheless, the implanted junctions showed reverse breakdown voltages that were a factor of two higher than diffused junctions.

In another applications paper, King, *et al.* [33] of Ion Physics Corporation (IPC), Burlington, MA, described the use of "ion implantation" at energies between 50 and 400 keV for building p-n junction devices such as solar cells, radiation detectors, unipolar field-effect transistors with

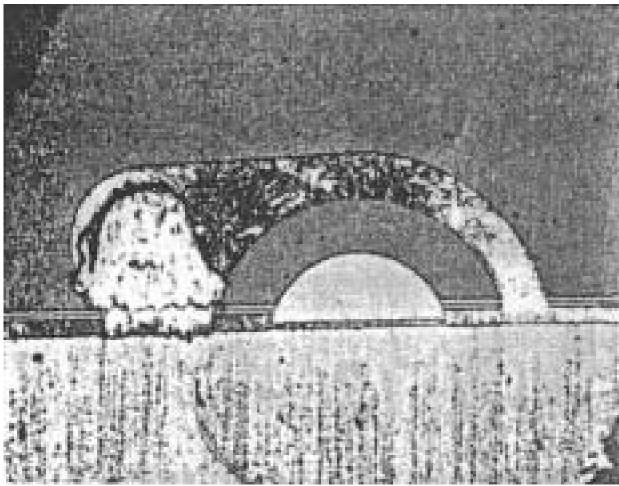


Fig. 7. Cross-section micrograph of one of the first bipolar transistors fabricated by ion-implantation techniques (after [32]).

transconductances greater than 2000 μmho, and bipolar transistors with $\beta > 40$ using double-ion implantation. And this work had been going on since 1962, when King *et al.* reported on the formation of p-n junctions by "ion-implantation doping" at the May Electrochemical Society Meeting. [20] In his 1962 paper, King reported that boron ion-implantation doping was responsible for the formation of p-n junctions, but his audience at that time was probably skeptical, believing that radiation damage was responsible for the conductivity-type conversion. Although transistor I–V characteristics from working devices were reported (see, for example, [34] and Fig. 19 of this paper, which is described in Section V), additional skepticism about IPC's results supposedly arose from some outside workers who were unable to verify IPC's claims of device performance from independent measurements on IPC's devices. IPC reportedly would not disclose additional details of their proprietary annealing process that would allow others to understand why the devices they received were of poor quality. This may have slowed the acceptance by other companies of IPC's unique approach to practical ion-implantation technology.

Despite the skepticism, King correctly reported at the Aarhus Conference that the keys to success in ion implantation were different from those approaches that were described by others at the conference:

1) implants should be performed specifically in non-channeling directions so that use could be made of direct range-energy relationships for implanted ions in noncrystalline targets as developed by Lindhard *et al.* [35] to predict junction depths;
2) implants should be made through passivating surface oxides to reduce sputtering of the silicon;
3) spectroscopically pure ^{11}B and ^{31}P ion beams should be used;
4) after ion implantation, samples must be heated to 700°C to transfer implanted ions to substitutional lattice sites.

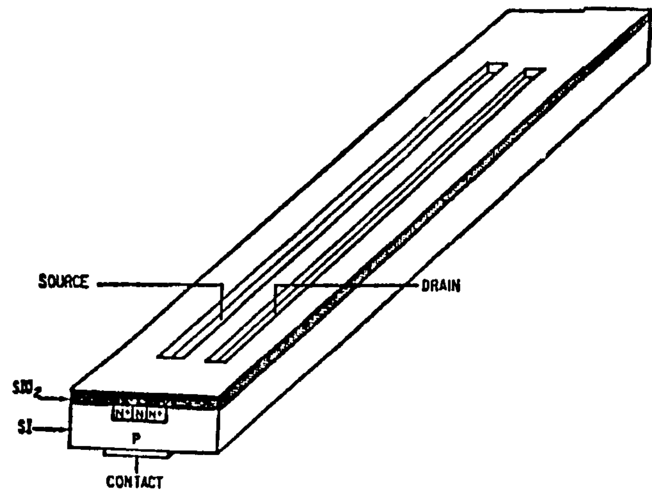


Fig. 8. Drawing of the IPC unipolar ion-implanted transistor from 1965. A one-mil-wide n-type layer was first ion implanted with phosphorus into a p-type substrate through the oxide layer. The source/drain regions were then etched open, and phosphorus was implanted to form n^+ regions (after [36]).

Even though his reported 700°C anneal would be too low to bring about satisfactory damage repair, King's methodology for successful application of ion implantation was on track and showed remarkable insight as to how ion implantation could be successfully used.

On June 28, 1965, *Electronic News* [36] ran a feature article entitled "Ion Implantation Techniques To Effect Changes in Semicons." In this article, the work of King at IPC was reported, and a figure from this article is shown in Fig. 8. "Production rates of thousands of transistors per second" are possible, claimed J. Gale, president of IPC. In addition, junction field-effect transistors produced by ion implantation were promised with "higher frequency responses than those turned out by conventional techniques." Referring to Fig. 8, the higher frequency responses would be a result of closely controlling the distance between the implanted source and drain junctions, resulting in devices of short channel length.

According to results that appeared in May 1966 in a report to the air force [36], IPC's process for fabricating their field-effect transistors included a photoresist mask, which was first applied to a 1000-Å oxide over the silicon and which stopped the beam in those areas where implantation was not required. This was the basic principle described in 1964 by Amadei and Goetzberger [24], who used molybdenum over oxide. Later, due to photoresist contamination problems, IPC would substitute the resist mask for an aluminum implant mask. After the source/drain implants were performed, the aluminum mask was removed so that a 600°C annealing step could be performed to activate the implanted atoms. As we will see below, the removal of the aluminum mask was a key step that precluded IPC from possibly inventing the self-aligned-gate process. If they had used molybdenum instead of aluminum, they would not have had to remove the metal mask, since molybdenum can withstand temperatures well above 600°C. According to the IPC process, source/drain

contact openings were then etched and the contact metals were applied. Since the silicon substrate acted as the gate and depleted the channel toward the surface, there was no need to worry about registering a top gate electrode with respect to the source and drain regions. And, this also led IPC away from the self-aligned-gate transistor. No one at this time had a solution as to how to align a top gate with respect to established source/drain regions, and this apparently led IPC to use the silicon substrate as a gate. However, the solution to this critical piece of the technology puzzle would soon be discovered by several groups within a period of about a year of each other, and this fascinating story will be described in the next section.

III. The Invention of the Self-Aligned Gate MOSFET

A. Limitations of MOS Technology

In 1963, the Fairchild Group, led by C. T. Sah and his colleagues under the direction of G. E. Moore and R. N. Noyce, developed the first commercially viable process for fabricating MOS field-effect transistors (MOSFET's). This milestone was achieved after much research into technology that would stabilize the interface between a thermally grown SiO_2 layer and the silicon surface. As mentioned earlier, one of the keys to controlling interface charge and mobile ion contamination in oxides was scrupulous care and cleanliness in every process step, as well as the gettering of mobile sodium ions, which moved through the oxide under gate voltage biasing [37], [38]. Other key milestones involved the development of both p-channel and n-channel MOSFET's with a wide variety of electrical characteristics [39]. A careful and detailed chronicle of the development of the MOSFET can be found in [40].

The first commercial MOSFET from Fairchild was the F1-100 p-channel enhancement-mode device made by the diffused silicon planar II process. The basic steps of this process involved growth of the gate oxide layer over the silicon, etching the oxide layer through a photoresist mask to form openings down to the silicon surface, diffusing the source/drain regions using a chemical-vapor diffusion source at high temperature, and regrowing oxide and then depositing a metal layer over the regrown oxide. A photoresist masking step was then performed to etch the metal-gate pattern between the source/drain diffused regions as well as to form the metal contacts to those junctions.

The natural and logical process sequence in the early to mid-1960's was to put the gate down after the formation of the source/drain regions by diffusion. The use of aluminum as the preferred metal-gate material (melting point = 660°C) made it impractical for engineers to establish the source/drain regions first, since diffusion temperatures used for source/drain doping were in excess of 900°C. As a result, it was necessary to perform a photolithographic alignment step to place the gate between the source and drain regions. The alignment tolerances for any lithographic step are such that there is an uncertainty in overlaying one feature with respect to another that is approximately equal to one-third of the placed feature's dimension [41]. Thus, the registration of a 10-micrometer-wide metal-gate feature between the established source and drain regions required that the gate overlap the source/drain regions by approximately the uncertainty of the registration (a few micrometers). Such an overlap is illustrated in Fig. 9. The main problem with this approach was that if the gate was too wide relative to the channel region, the resulting gate-to-drain overlap capacitance became quite large for these devices. This capacitance is reflected back to the input of the MOSFET according to Miller's theorem, and the resulting input capacitance is significant in limiting the high-frequency performance of the device. If the gate was too narrow relative to the channel region and did not cover it completely, undesirable ohmic losses were introduced.

B. The Self-Aligned-Gate Invention

The solution to the gate realignment dilemma was discovered by several independent R&D groups around the world. Each effort was, perhaps, driven by the need to solve a different problem, but the end results were similar. In a published note [42] in 1964 and a patent filed June 1, 1964 [43], H. A. Klasens of Philips Corporation in Eindhoven described an improved and simplified method of fabricating a metal-gate, thin-film transistor fabricated such that "the source electrode, the gate electrode and the drain electrode are situated in this sequence in juxtaposition on the same side of the semiconductor layer." This self-alignment scheme was achieved by irradiating a photoresist layer with light while using the gate of the device as a mask. The key contribution of Klasans was that he demonstrated a novel self-aligned-gate process that used the gate in an alignment scheme to control the locations of the source/drain regions automatically. By contrast, in 1966, T. S. te Velde at Philips invented a method of making a field-effect transistor in which the gate acted as a mask against ion bombardment used to form source/drain regions self-aligned to the gate [44]. This work was apparently driven by an interest in applying radiation damage from ion bombardment to transistor fabrication. The semiconductor substrates were cadmium or zinc sulphides or selenides, and the bombarding ions were preferably argon, oxygen, or nitrogen. The ion-bombarded structure is shown in Fig. 10. "As a result of this bombardment strongly conductive surfaces 10 and 11 are formed in the uncovered regions of the cadmium sulphide" [44]. Thus, the next step had been taken whereby instead of light, an ion bombardment was used to self-register the source/drain regions. And the ion bombardment produced conductivity-type changes in the semiconductor as a result of radiation damage.

Meanwhile, other workers were experimenting with methods of creating self-aligned-gate MOSFET's that required doped source/drain regions in a silicon substrate. H. Dill at Hughes Aircraft Company was experimenting with a high-temperature gate material—polycrystalline silicon (melting point = 1410°C). On October 26, 1966, Hughes filed for a patent that described a process in which

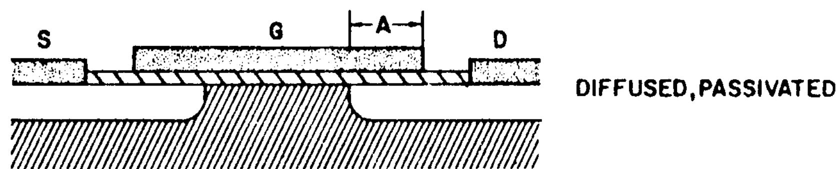
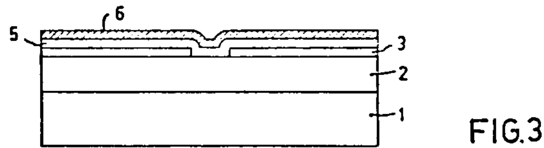
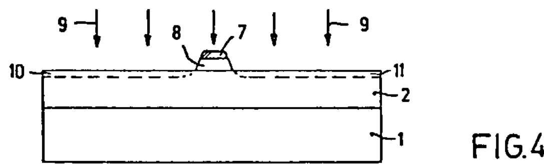


Fig. 9. Cross-section drawing of a standard aluminum-gate MOSFET in the mid-1960's. The metal gate had to be put in place after the high-temperature source/drain diffusion step, which caused the gate to overlap the source/drain regions by an amount A to accommodate uncertainties in the alignment process (after [52]).





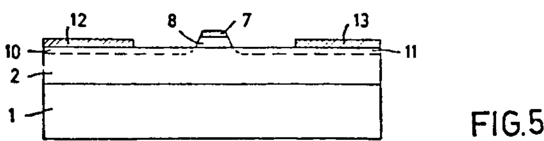


Fig. 10. Cross-section view of Philips' ion-bombarded, self-aligned-gate MOSFET from 1966. The semiconductor substrate was cadmium or zinc sulfides or selenides and the bombarding ions were preferably argon, oxygen, or nitrogen, which induced surface regions 10 and 11 (after [44]).

the polysilicon gate was patterned on a gate oxide first, followed by a high-temperature source/drain diffusion step [45]. This type of process was to become known as a self-aligned-gate process, since the source/drained regions were self-aligned to the gate, which saved one lithographic step in the process flow. Dill's process sequence is shown in Fig. 11.

Meanwhile, in the same laboratory at Hughes Aircraft, R. Bower was the named inventor on another patent [46] filed on October 27, 1966, one day after the Dill patent. Bower was apparently interested in the application of ion implantation for fabricating self-aligned-gate MOSFET's with an aluminum gate at low process temperatures, as described in the specification of Patent 3 472 712 (the '712 patent). Another motivation was to fabricate MOSFET's with reduced Miller capacitance for improved high-frequency performance. The ion-implanted self-aligned-gate process as described in Bower's patent is shown in Fig. 12. The '712 patent teaches that "the gate may be of metal and of aluminum." After gate patterning, "ions of a conductivity-type-determining impurity" are implanted so as to establish source/drain regions "adjacent the region thereof under said insulated-gate electrode member." One of the claimed advantages of the patent was that "the semiconductive body need not be heated to excessive temperatures [i.e., above 550°C] which in other doping processes often deleteriously affects the semiconductor and renders precise control of a device during fabrication tedious and expensive." As we have seen this was characteristic of the mindset of the time among the ion-implantation community, and Bower's work apparently reflected the thinking at Hughes regarding how ion implantation could be successfully used in conjunction with the established aluminum-gate technology for MOSFET fabrication. This position would be maintained for at least the next five years. A 1970 article in *Electronics* [47] would note that Hughes remained a "skeptic" of silicon gates because they "feel they have a better idea" in applying ion implantation to aluminum-gate MOS technology.

Meanwhile, at Bell Labs, R. Kerwin, D. Kline, and J. Sarace were named inventors on a self-aligned-gate patent filed March 27, 1967 [48], five months after the Dill '399 patent was filed. Bell Labs' claimed invention was technically identical to Hughes' Dill patent in that silicon gates were established in order to self-align diffused source/drain regions. Fig. 1 from the Kerwin patent is shown here in Fig. 13. It was inevitable that a court decision would be required to decide who would be awarded priority on the invention date of the self-aligned-gate MOSFET. Also to be figured into the discussion would be the ion-implanted, self-aligned-gate invention of Bower and a fourth invention that had occurred more than one year prior to the other three.

C. The Self-Aligned-Gate Controversy

It is not well known, but even prior to the filing of patent applications on the self-aligned-gate MOSFET by Dill, Bower, or Kerwin, the invention had already been conceived by workers at General Micro-Electronics (GME), Inc., a 1963 Fairchild spinoff company. GME began designing the first large-scale integrated circuits primarily for military use and had a program underway in 1965 on the chemical-vapor deposition of polysilicon for use in silicon-gate MOS technology. In a patent interference hearing that would take place later in 1974 in U.S. District Court in Delaware [49] between the Dill patent 3 544 399 assigned to Hughes [45] and the Watkins patent 3 576 473 assigned to GME [50], the court acknowledged that certain

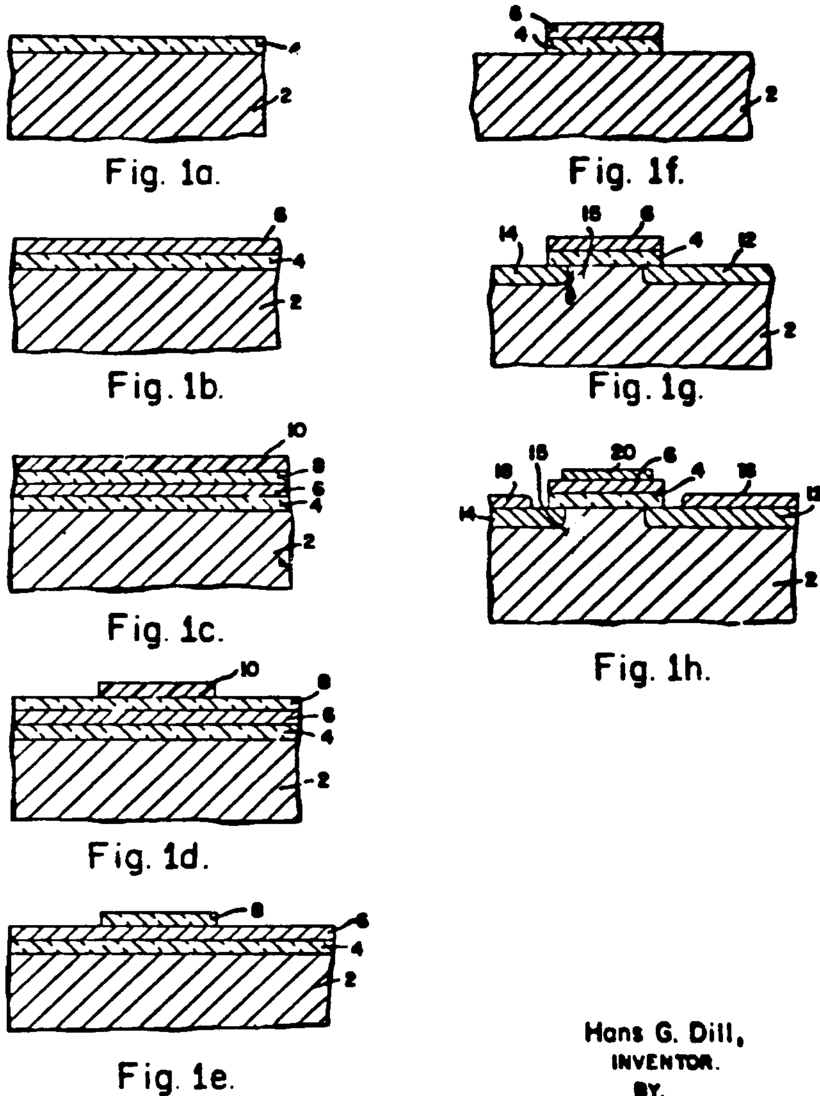


Fig. 11. Cross-section views of the Hughes' self-aligned, silicon-gate MOSFET process showing the gate established prior to the source/drain diffusions (after [45]).

employees at GME conceived the silicon-gate invention by March 1965. One of those inventors was believed to be B. Watkins, who, in a proposal to the air force dated August 9, 1965, disclosed the self-aligned, silicon-gate process in which "polysilicon could be used as a mask to provide for self-aligning or automatic aligning of gates . . . with respect to the source and drain." The sources and drains were to be established by a diffusion technique. Later, in September 1966 (one month prior to the filing of the Hughes' patents), GME would file for the invention of the self-aligned, silicon-gate MOSFET [50].

The court ruled [49] that even though Dill independently conceived of the silicon-gate invention on May 1, 1966 (14 months after GME), GME never constructively reduced the invention to practice. Even GME's patent filing in September 1966 did not constitute a constructive reduction to practice because certain drafting errors in the patent application's drawings described an inoperative device. GME corrected the drafting mistakes and refiled their patent application on November 17, 1966. However, Dill and Hughes were deemed to have reduced their invention to practice on October 26, 1966, when the Dill patent was

Oct. 14, 1969 R. W. BOWER 3,472,712

FIELD-EFFECT DEVICE WITH INSULATED GATE

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Fig. 1a.

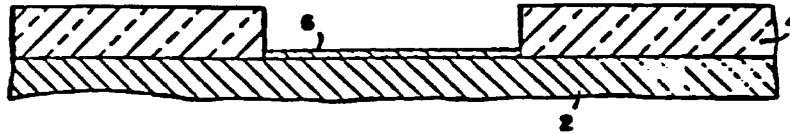


Fig. 1b.

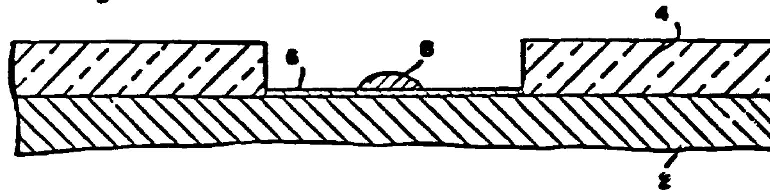


Fig. 1c.

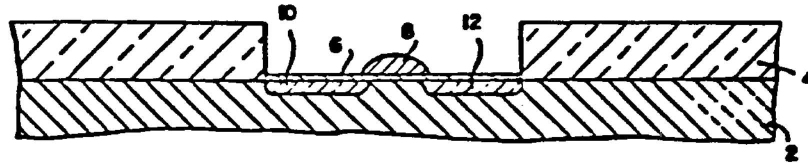


Fig. 1d.

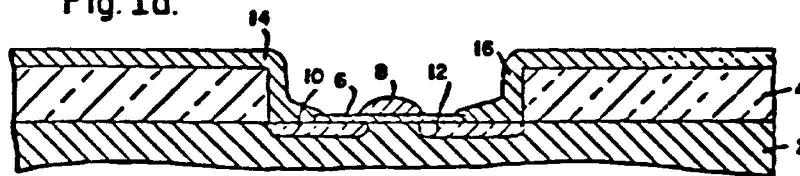
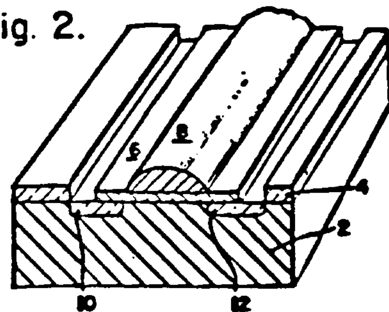


Fig. 2.



Robert W. Bower,
INVENTOR.
BY.
ATTORNEY.

Fig. 12. Cross-section views of the Hughes' ion-implanted, self-aligned, aluminum-gate MOSFET process showing the gate established prior to the source/drain implantations (after [46]).

filed. Thus, while GME was first to conceive, they were last to reduce to practice, and Hughes was awarded the priority invention date [49].

It would also take a patent interference hearing to decide whether Bell Labs' Kerwin patent [48] had the priority invention date over the Dill patent [45]. According to Kerwin's notebook, the process for fabricating self-aligned, silicon-gate MOSFET's was established at Bell Labs in February 1966, and working devices were measured in May 1966, five months before Hughes' reduction to practice. As a result, Bell Labs' invention prevailed.

The ion-implanted versions of the self-aligned-gate inventions had no less controversy. Regarding the Bower '712 [46] and te Velde '030 [44] patents, the two patent disclosures were filed within a few months of each other. Both patents claimed that a gate should be first formed on a semiconductor substrate, which would serve as a mask against impinging ions. Then, the device was subjected to

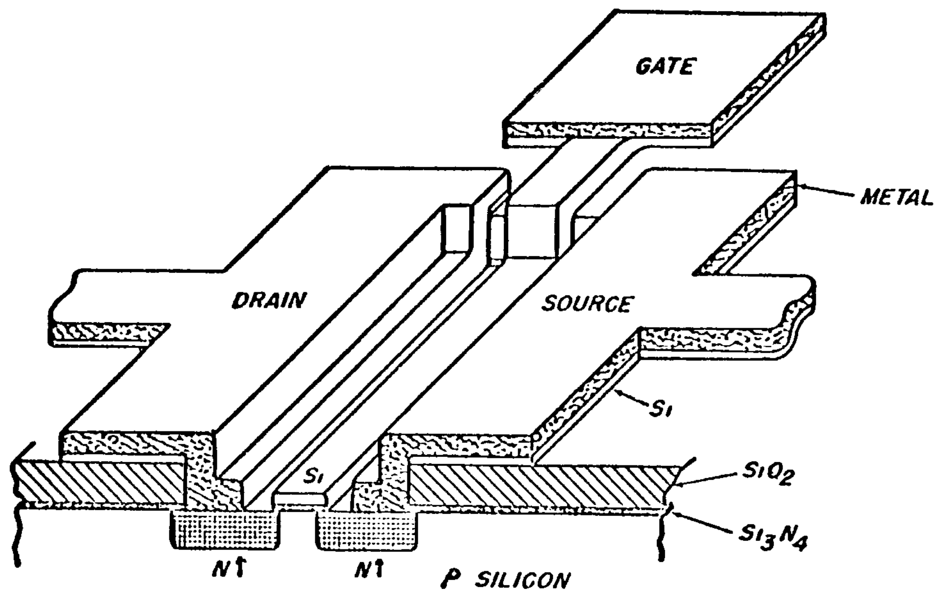


Fig. 13. Cross-section view of Bell Labs' self-aligned, silicon-gate MOSFET structure with the gate established prior to the source/drain diffusions (after [48]).

ion implantation (Bower) or ion bombardment (te Velde) so as to form regions of like conductivity type opposite to the substrate's conductivity type (Bower) or regions of modified conductivity (te Velde). These conducting regions were formed adjacent to the gate (Bower) or on opposite sides of the provided gate (te Velde). The differences in claim interpretation would be key to the determination of priority in the invention of the self-aligned gate. For example, were te Velde's ion-bombarded regions really adjacent to the gate in view of the sloped gate oxide regions, as shown in Fig. 10? And is a modified conductivity region different from a region that has undergone a conductivity-type change? It would be left to a judge in another patent interference proceeding in the mid-1980's to determine these differences and to decide whether the te Velde invention anticipated the Bower invention. The Hughes invention would be ruled valid, which allowed Hughes to begin alleging infringement of its '712 patent [46] against much of the world's semiconductor industry.

D. Making the Ion-Implanted, Self-Aligned-Gate MOSFET Work

Meanwhile, back in the 1960's again, Bower and Dill gave a talk at the 1966 International Electron Devices Meeting (IEDM) in October 1966 [51] on the ion-implanted, self-aligned-gate MOSFET. In their talk, they reiterated the value of using ion implantation in conjunction with low-temperature processing to form devices in which the Miller capacitance was reduced by a factor of 40 over conventionally processed devices. It is of interest to note that in the abstract of their talk, which was available to meeting attendees, it was stated that "if a polycrystalline silicon film replaces the metal gate, conventional diffusion technique can be applied to this technique." Thus, it would appear that Hughes did not put together polysilicon gate technology and ion-implanted, self-aligned-gate technology, which ultimately would have opened the door to the successful high-temperature processing regime that has been the backbone technology of the modern integrated circuit business.

Subsequent publications by Bower *et al.* pointed out the shortcomings of the '712 patent. At the 1967 IEDM, they stated that the self-aligned, aluminum-gate MOSFET had several shortcomings, including high junction leakage, two-step metallization, and contact problems [52]. Here, they introduced a new device structure that was fabricated as shown in Fig. 14, which was also filed as a patent disclosure right after the 1967 IEDM [53] on October 30, 1967. Deep source and drain contact regions were created first in the silicon, a gate oxide was grown, and then the aluminum gate was placed between the spaced-apart diffusions in a noncritical alignment step. The ion-implantation step followed, which created doped source/drain extensions between the edges of the gate and the deep diffusion regions. This device structure allowed for the gate and the metal source/drain contacts to be made simultaneously. In addition, by implanting ions through an oxide layer over the source/drain extensions, a fully passivated device could be formed [54].

Hughes continued to develop the 1967 version of the device into the early 1970's. By 1971, they were fabricating 20-MHz shift registers, multiplex circuits, and a 2048-b read-only memory, all using their offset-gate, ion-implantation technology. However, the desirability of incorporating a higher temperature annealing step after implantation was evident in a 1971 paper [55]. There, Dill and Bower pointed out that the percentage of implanted B that was electrically active after a 545°C anneal actually decreased with increasing implant dose, so that only 30% of the B was electrically active for a dose of 10^{14} ions/cm^2. These results, shown in Fig. 15, resulted in compromised MOSFET performance. However, their studies had shown

United States Patent [11] **3,615,934**

[72] Inventor **Robert W. Bower**
Palos Verdes, Calif.
[21] Appl. No. **678,809**
[22] Filed **Oct. 30, 1967**
[45] Patented **Oct. 26, 1971**
[73] Assignee **Hughes Aircraft Company**
Culver City, Calif.
Continuation-in-part of application Ser. No. 590,033, Oct. 27, 1966, now Patent No. 3,472,712.

[54] **INSULATED-GATE FIELD-EFFECT DEVICE HAVING SOURCE AND DRAIN REGIONS FORMED IN PART BY ION IMPLANTATION AND METHOD OF MAKING SAME**
3 Claims, 10 Drawing Figs.

[52] **U.S. Cl.** **148/186,**
317/235 R, 317/235 B, 317/235 AL, 148/1.5
[51] **Int. Cl.** **H01l 7/44,**
H01l 11/14
[50] **Field of Search** 317/235
(21), 235 (21.1), 235 (24), 235 (40), 235 (48), 235 (48.4), 235 (22.2); 148/1.5

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Primary Examiner—John W. Huckert
Assistant Examiner—Martin H. Edlow
Attorneys—James K. Haskell and W. H. MacAllister, Jr.

ABSTRACT: Field effect device having diffused major source and drain regions spaced from each other on a common surface of a semiconductor body with insulated gate member disposed on same surface and spaced from and between the source and drain regions, and shallow regions formed by ion implantation using the gate member as a mask extending from the periphery of the gate member to the source and drain regions.

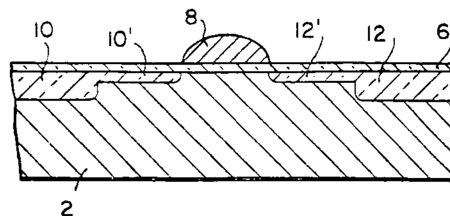


Fig. 14. Cross-section view of Hughes' self-aligned-gate MOSFET with ion-implanted source/drain extension regions 10′ and 12′, which were established after the deep diffusions 10 and 12 and after the gate, 8, was noncritically aligned between 10 and 12 (after [53]).

that an 800°C anneal was required to achieve 100% activation. As a result, Dill and Bower correctly suggested that the aluminum gate be replaced with a high-temperature molybdenum metal gate, whereupon it was possible to achieve ion-implanted source/drain sheet resistances in the 100–200 Ω/square range in conjunction with a high-temperature anneal. By this time, however, work at Fairchild [56] had successfully demonstrated the great promise of polysilicon gate technology in MOSFET fabrication since it enabled the required high-temperature annealing steps for the successful use of ion implantation. Silicon-gate processing also made possible other high-temperature processes such as phosphorus-doped glass reflow for smoothing dielectric surfaces and gettering for removing unwanted metallic impurities from junctions. Thus, metal-gate technology would be discarded by most of the merchant semiconductor manufacturers in favor of silicon-gate processing, although IBM and Texas Instruments would continue to manufacture metal-gate MOS IC's for many years. Nevertheless, silicon-gate technology held much promise at the time. Indeed, in 1968, a group of engineers at Fairchild led by Noyce and Moore left Fairchild to start a new company whose products would be based upon silicon-gate technology. This company would be named Intel Corporation.

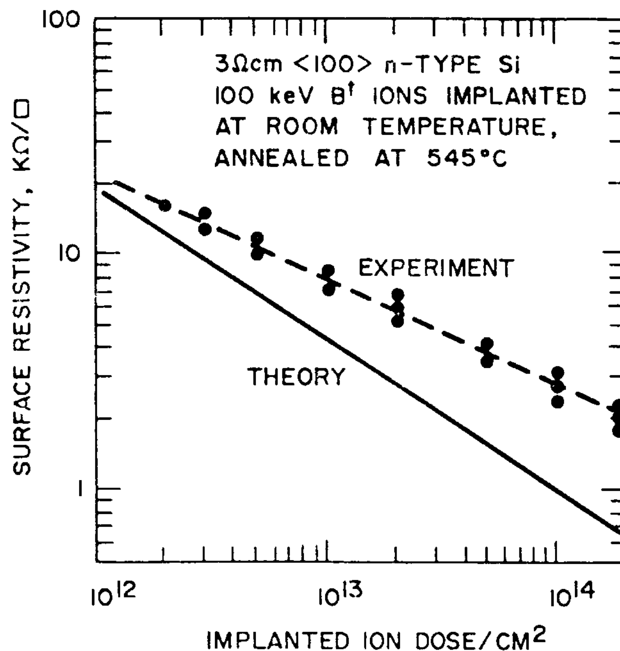


Fig. 15. Resistivity of 100-keV boron-implanted Si as a function of implant dose after a 545° C anneal. These results were apparently responsible for Hughes' decision to switch to a high-temperature metal-gate process, which allowed for 800°C annealing of the self-aligned source/drain implants (after [55]).

Although Hughes' work on self-aligned-gate technology did not evolve into what we know today as self-aligned silicon-gate technology, Bower was correctly recognized for his outstanding work by being elected a Fellow of the IEEE in 1986 "for inventing the self-aligned-gate ion-

implanted MOSFET and for establishing ion implantation to fabricate semiconductor integrated circuits." In 1997, Bower would be inducted into the Inventor's Hall of Fame for the self-aligned-gate MOSFET. At the 1994 IEDM, however, the Bell Labs inventors were awarded the IEEE Jack A. Morton Award "for pioneering work and the basic patent on the self-aligned silicon-gate process, a key element in fabrication of very large scale integrated circuits." It would seem that even today, the issue of who first invented the self-aligned-gate MOSFET is not settled.

Setting aside all of the legal issues, it is clear to this author that the basic concept of establishing the gate prior to forming the source/drain regions of a field-effect transistor was, in fact, coconceived in isolation by each of the groups mentioned above in response to the inventors' particular needs or applications. And the inventors all deserve credit for visualizing a new method that ran counter to prevailing methods of fabrication, regardless of whether the invention used light, bombarding ions, or diffusing dopant impurities. These works clearly established a methodology for the eventual application of ion implantation to self-aligned silicon-gate technology, which would become a core technology for every integrated circuit manufacturer in the world.

E. How High an Annealing Temperature Was Required?

Bell Labs was relatively slow in applying ion implantation to its self-aligned-gate technology. In a 1967 Bell Labs internal memo, which reviewed the results of the 1967 International Conference on Applications of Ion Beams to Semiconductor Technology, held in Grenoble, it was suggested that the clear advantage of ion implantation was low-temperature processing. Since the postimplantation anneals would be lower than what was required for diffusion, this would diminish the introduction of spurious impurities and would decrease wafer processing times to the order of minutes, compared to hours for diffusion. As a result, an ion-implantation group was established under M. Lepselter at Murray Hill, NJ. Some of this group's activities were directed to the study of high-temperature annealing behavior of implanted dopants [57]. This work contributed to the understanding of the use of high annealing temperatures for annealing ion-implantation damage, for creating ion-implanted layers with high electrical activity, and for forming p-n junctions with low reverse-leakage currents [58].

During the time when an ion comes to rest within the silicon lattice, a highly disordered region is formed along its track. An excellent review of what was known about damage production at this time is given by Gibbons in [13]. By the early 1970's, it was becoming clear to a most groups that such forms of damage had to be removed to form viable, ion-implantation-doped devices. However, the dream of low-temperature processing for aluminum-gate technology was still alive. This led researchers at IBM and Hughes to explore high-dose implants that were capable of amorphizing the silicon crystal, i.e., removing any long-range order in the silicon lattice. It was discovered that annealing such an amorphous layer at 550°C produced high electrical activity after the amorphous layer was regrown back to a single-crystal layer [59]–[61]. This result opened investigations into processing ion-implanted devices in the 450–600°C range utilizing room-temperature implants [63]. It was found, however, that the free-carrier lifetimes in these layers were very low, and p-n junctions fabricated under low-temperature conditions showed high junction leakage currents. Most of this work was eventually abandoned as the advantages of high-temperature annealing became obvious. Nevertheless, some workers today are still interested in exploring low-temperature processes for limiting the diffusion of implanted layers in ultrasmall transistors.

The annealing temperature range of 900–1000°C was explored for device applications that required 100% doping efficiency with bulk carrier mobilities. Though implanted profile broadening often occurred in this temperature range, this usually was not of concern in many applications, where control of electrically active dopant impurities was the key requirement. An excellent review of the work in annealing was published in this PROCEEDINGS in 1974 by Lee and Mayer [63].

The main challenge to the successful integration of ion implantation into MOS processes was the recognition of the fact that standard processes had evolved over time empirically after many trial-and-error attempts at fabricating successful devices. As a result, device engineers were reluctant to accept anything new and revolutionary that would perturb a working process. In the words of Bower from 1970, "it is essential to ensure that any application of ion implantation to planar technology maintain the virtues of the process" [64]. The semiconductor industry was introducing additional high-temperature process steps such as phosphorus-glass reflow at 1100°C for smoothing the topography over which aluminum interconnections and contacts would lie and gettering steps for removing metallic impurities from junctions. Thus, it was inevitable that ion implantation would move away from the concept of being a low-temperature process for producing a controlled, as-implanted concentration profile to being a predeposition technology. In this case, a low-energy implantation step was performed to predeposit a controlled number of dopants in the silicon, followed by a high-temperature drive-in step to establish the concentration profile by diffusion. Drive-in temperatures typically were in the 1100–1200°C range. In 1972, Wagner [65] published some of the first work on ion-implanted boron predepositions and drive-ins. Soon afterwards, Bell Labs and Western Electric jointly developed 30-keV, high-dose predeposition ion-implantation machines for use with all low-sheet-resistance applications in ion-implanted device manufacturing. Bell Labs device designers would be practically compelled to use these machines for all high-dose device implants for the next ten years.

For the majority of the merchant semiconductor companies, the introduction and commercial use of the ion-implanted, self-aligned-gate process would not occur until the late 1970's to early 1980's. Constant-field scal-

ing of MOSFET dimensions established by Dennard [66] did not become critical with regard to requiring shallow source/drain regions until the 1980's, so manufacturers continued to use their old, reliable phosphorus diffusion furnaces. In addition, the yield on making aluminum contacts to junctions that were less than 1 μm deep was quite poor at that time due to aluminum spiking that would cause alloyed regions to penetrate junctions.

When it became clear that phosphorus-diffused junctions were simply too deep for device-scaling needs, a number of manufacturers of dynamic random-access memory (Intel, Texas Instruments, IBM, etc.) began investigating arsenic-diffusion sources. Since the handling of toxic arsenic was quite dangerous, most arsenic-diffusion methods were unsafe. However, the evacuated glass-ampoule arsenic source was successfully introduced into manufacturing by a few companies. This source consisted of solid arsenic or one of its compounds that was sealed inside a quartz tube along with the silicon wafers. The assembly was evacuated, and after heating the ampoule to diffusion temperatures, the assembly was then cooled and subsequently broken open to extract the wafers. The shattered quartz would shower particles over the wafers, which greatly complicated processing. As a result, these manufacturers began investigating arsenic ion implantation, not necessarily because it gave better device performance but because it was cleaner and improved device yields. In addition, Fair and Tsai [67] showed that higher levels of electrical activation were possible with arsenic ion-implanted and diffused regions compared to arsenic chemical-source-diffused regions. The latter produced larger concentrations of electrically neutral arsenic-vacancy complexes by virtue of arsenic-incorporation reactions at the silicon surface.

By the early 1980's, high current implanters were readily available with arsenic sources, and much was known about the diffusion of ion-implanted arsenic in silicon. By then, practically the entire industry was using arsenic-implanted source/drains for a lack of any better alternative.

IV. Threshold-Voltage Adjust Implants

In the late 1960's and early 1970's, the acceptance by semiconductor companies of ion implantation as a manufacturing technology was at a critical point. Many key people in the business were convinced that any device could be made better with a combination of diffusion technology and planar processing than with ion implantation. There were only a few successful demonstrations that countered this view, one being the ion-implanted hyperabrupt diode put into manufacturing at Western Electric, Reading, PA, in 1968. Here, ion implantation was used to create a diode with a unique capacitance-voltage characteristic that could not be achieved by diffusion technology. Ion implantation needed to succeed in mainstream, bread-and-butter semiconductor processing, however, and to do this, it needed to demonstrate either that it could outperform existing technology or that it was capable of some unique application that could not be done with existing technology. In addition,

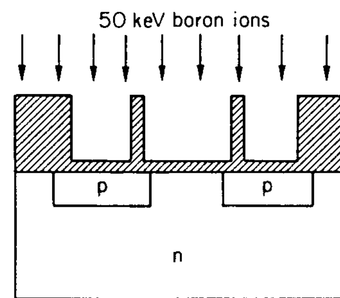


Fig. 16. The concept of channel doping by ion implantation as illustrated around 1972 for a nonself-aligned-gate process at Texas Instruments. A light implant was made through the gate oxide to dope the channel region and set the threshold voltage after the source/drain regions were in place (after [68]).

companies would have to justify the cost of integrating a new technology that brought with it requirements for capital investment, R&D, and process/product engineering costs. No one up to this time had really succeeded in this effort to the extent that the industry would be compelled to use ion implantation. However, one semiconductor manufacturer—namely, MOSTEK—in collaboration with Sprague Electric Company would find that unique application, take the risk, bet the company's future on it, and succeed. And this success would be a turning point in bringing ion-implantation technology into semiconductor factories, where its use would proliferate to additional applications.

This key application of ion implantation was dopant control in the channel regions of MOSFET's. This process allowed the threshold voltage of an MOS transistor to be established prior to, or after, the gate oxide has been grown rather than relying upon the poorly controlled doping levels established in the substrate by crystal growth. The concept is illustrated in Fig. 16 for a p-channel, nonself-aligned-gate device at Texas Instruments circa 1972 [68]. Boron ions implanted into the channel through the gate oxide reduce the magnitude of the substrate charge, causing the negative threshold voltages to be shifted to more positive values. Some of the historical events that led up to the adoption of threshold-voltage implantation are discussed next.

One of the earliest proposals for using "ion implantation" for controlling the conductivity of the channel of a field-effect transistor was made by Electro-Optical Sciences, Pasadena, CA (a subsidiary of Xerox), in a proposal to the air force in May 1964. This company apparently was looking for new applications and funding for their Cs^+ ion beam propulsion system. Therefore, they proposed bombarding an FET channel using ohmic contact electrodes already in place as masks. The device structure is shown in Fig. 17 and represents a self-aligned channel process [69]. The Cs^+ ion bombardment would change the conductivity of the p-type substrate to n-type by radiation damage whereever the silicon was exposed to the beam.

In the mid-1960's, the space-science community became very interested in radiation damage effects in thermally grown, p-channel enhancement MOS devices for radiation-hard applications. MOSFET's were particularly sensitive radiation damage detectors because of the resulting dam-

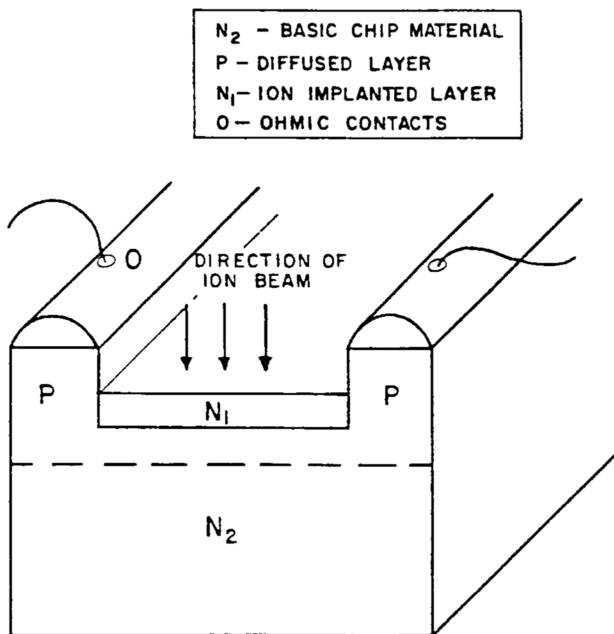


Fig. 17. One of the earliest known examples of changing the conductivity in the channel region of an FET using Cs^+ ion bombardment self-aligned to the ohmic contacts, which had already been established (after [69]).

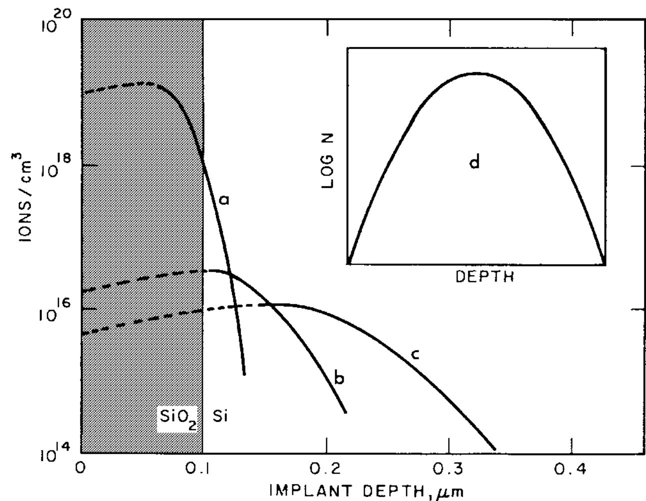


Fig. 18. One-dimensional depth profiles of boron atoms implanted through a 1000-Å oxide layer into silicon. Curve a represents poor threshold-voltage control due to sensitivities to oxide thickness variations. Curve b is placed at the oxide/silicon interface and curve c is a deep implant, both of which are suitable for threshold-voltage adjustments (after [73]).

age produced in the gate oxides and the resulting measurable shifts in threshold voltage during, for example, high-energy electron bombardment. In 1965, Speth [70] at IBM suggested the use of electron beam bombardment for controlling the characteristics of MOS transistors. The bombardment would take place after the device had been fabricated and the gate was placed under positive bias. A stable shift in the threshold voltage was induced due to the electron irradiation, which produced electron-hole pairs in the oxide. Heating the transistor at 200°C for several hours would anneal out the radiation effects.

At Hughes Aircraft, studies were under way to look for ways of decreasing the sensitivity of irradiated oxides to permanent shifts in gate threshold voltages. One technique reported in 1968 involved the ion implantation of aluminum in the oxide, which was believed to increase the trapping of radiation-produced electrons in the oxide [71]. One of the apparent fallouts of this work was the report by Aubuchon in 1969 on the first use of through-oxide ion implantation to set the threshold voltage of MOS transistors [72]. In this demonstration, boron was implanted into the middle of a 1000-Å gate oxide layer with a dose of 10^{14} atoms/cm^2 and an energy of 16 keV. The theoretical implant distribution was indicated by curve a in Fig. 18 [63], [73]. It can be seen that a relatively small percentage of the total dose actually penetrated to the silicon, so that the threshold-voltage shifts observed were found to be extremely sensitive to ion energy and gate oxide thickness. In subsequent studies [74], however, lower doses were implanted with their peak distributions closer to the SiO_2/Si interface, as shown by curves b and c in Fig. 18. This resulted in a significant improvement in controlling threshold voltage shifting and repeatability [63].

Ion implanting through SiO_2 was known to damage the oxide. For successful application as a threshold-voltage adjustment technology, it was necessary to anneal at 400–500°C in order to restore the fixed-oxide charge to its preimplant value. However, for low-energy, high-dose implants, it was observed that a 900°C anneal was required to remove instabilities seen in bias-temperature measurements. These instabilities were probability due to enhanced mobile ion activity near the oxide/silicon interface. Thus, it became known by workers around 1970 that in order to use through-oxide ion implantation successfully, it was necessary to anneal the implanted wafers to bring both the ion distribution in the silicon to full electrical activity and to recover the oxide nearly to its initial quality. Reported results from Hughes in 1972 on high-dose boron implants through oxides supported the observation that annealing temperatures up to 900°C were required to achieve high electrical activity [75].

Work on threshold adjustment using ion implantation was also underway at Mullard Research Laboratories in 1969. Apparently, in order to avoid oxide damage and to accommodate their aluminum-gate process, Beale [76] reported that a low-dose boron implant was performed prior to the 1100°C gate oxidation step. During gate oxidation, the boron diffused to a depth of 0.6 μm. Beale was apparently the first to observe that this same implant could be used to control the spreading of the drain depletion layer toward the source to avoid punch through, a condition that occurs when the source and drain depletion layers come in contact. The selected channel doping in the surface region would allow the substrate doping to be decreased, thus reducing substrate body effects.

The first successful use of the threshold-adjust implant in integrated circuit manufacturing was reported in June 1970 by workers at MOSTEK and their parent company,

Sprague Electric [77]. At that time, MOSTEK was selling several ion-implanted, low-threshold IC's, including a dual 128-b static shift register, a dual 256-b dynamic shift register, and a 2240-b column-output character generator. In the MOSTEK process, only the channel regions were implanted in their nonself-aligned, aluminum-gate process. Annealing occurred before the gates were formed. The work was led by J. MacDougall and K. Manchester of Sprague, who probably understood the physics of threshold-voltage shifting. R. B. Palmer at MOSTEK became a collaborator who presumably appreciated the manufacturing significance of implantation for threshold-voltage shifting as applied to memory-circuit manufacturing. Together, the physics and the application came together. And Palmer and L. J. Sevin are credited with introducing the process into the MOSTEK production line in Texas. It is this author's understanding that MOSTEK could have gone into bankruptcy had the threshold-adjust implant process not worked. Sevin was quoted at the time as saying, "We bet the company on it." However, MOSTEK succeeded and would continue to lead the memory business into the mid-1980's. Most important, from a historical view, a mainstream application of ion implantation had been introduced into manufacturing, and this key event would drive the acceptance of ion implantation into the semiconductor business. Twenty years later, Palmer would go on to become the CEO of Digital Equipment Corporation.

Once ion implantation was available in their factory, MOSTEK also began using ion-implanted channels to form depletion-load transistors, which gave them a significant advantage in an n-channel (N)MOS circuit performance [78]. The advantages of depletion loads in digital circuit design were already known, but it was impractical to make them on the same chip as the enhancement-mode transistors using diffusion processing. Ion implantation solved this problem, which made its commercial use a necessity. At MOSTEK, depletion-load technology was applied to their 4096-b read-only memory chip, which was introduced in the early 1970's.

As a side note, it is interesting to observe that even today, many manufacturers still perform threshold-adjust implants through the gate oxide prior to gate deposition and patterning, relying on the source/drain implant anneal to remove the oxide damage. The alternative method was to implant first and then regrow the gate oxide, avoiding implant damage problems in the oxide. This latter approach was commonly avoided in NMOS technologies in the 1970's, however, since the threshold-implant species was always boron. During a typical 1970's gate oxidation, 500–1200 Å of oxide would be grown, and since boron preferentially segregates into the growing oxide, boron would be depleted from the silicon surface region (MOSFET channel region) in a less than desirable manner. As a result, threshold implants through gate oxides became part of accepted wafer processing practice. Today, however, gate oxides are typically less than 80 Å in thickness, and very little boron depletion occurs during such a small amount of oxide growth. The most successful semiconductor manufacturers have recognized that the threshold implant can now be performed prior to gate oxidation, resulting in higher quality gate oxides. Yields on IC's fabricated this way are usually significantly higher than devices in which the gate oxide is grown first.

V. Bipolar Transistors

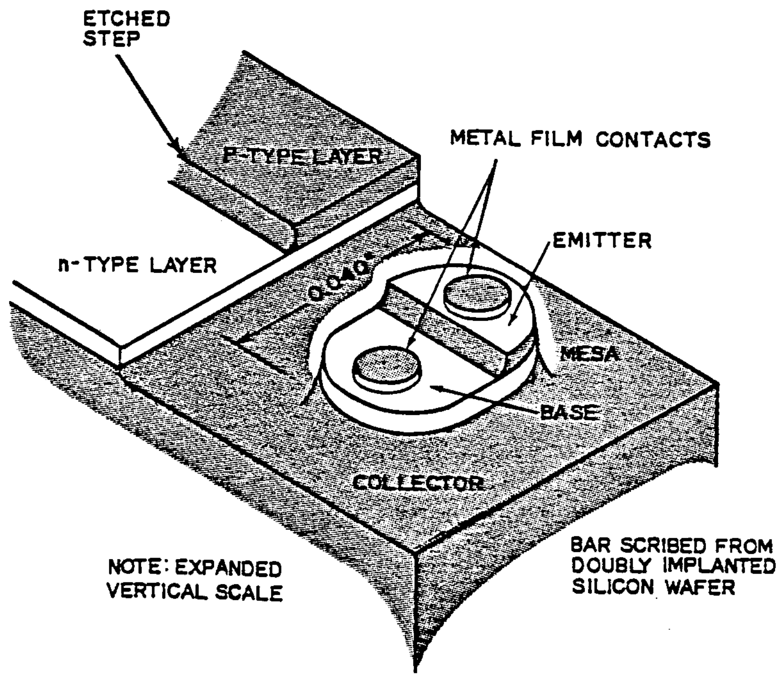
In this section, we note some of the developments in applying ion implantation to the fabrication of bipolar transistors. The time period covered is the early 1960's to the mid-1970's. Although there were many excellent contributions after this period covered in thousands of references, it is beyond the scope of this historical review to recognize even an appreciable fraction of them. We start with some of the early work and conclude with the early introduction of implantation technology into manufacturing.

A. The Early Work

The early work on bipolar transistors was performed on high-frequency n-p-n devices. The use of ion implantation was desirable not so much to reduce cost as to improve performance. Since much of the R&D was being performed on microwave transistors, they became a very good vehicle for experimentation.

The first reported use of ion implantation for fabricating bipolar transistors was reported by Manchester *et al.* [32] and by King *et al.* of IPC in 1965 [33], where both emitters and bases were formed by ion implantation. According to [34], the IPC device was a p-n-p mesa transistor built in 10 ohm-cm p-type silicon. The surface of the wafer was covered with 1000 Å of anodically grown silicon dioxide, through which was implanted a 300-keV phosphorus base layer at a dose of 1.25×10^{15} ion/cm^2. After a 750°C anneal, the emitter implantation was performed using 100-keV boron at a dose of 4.5×10^{15} ions/cm^2. A second 750°C anneal was then performed. The emitter-base junction was observed to be 0.43 μm deep, and the collector-base junction was 0.88 μm deep. Transistor structures were created by etching mesa patterns down through the silicon and then applying thin-film metal contacts, as shown in Fig. 19. Also shown are common-emitter device characteristics, which exhibit transistor action.

The most significant promise of ion implantation applied to bipolar transistors was the ability to control the base doping and thus the reproducibility of the transistor's gain. In addition, control of the implant energy would allow control of the base width, which would then allow control of the transistor's speed. These aspects were first pointed out in 1967 by Kerr and Large at SERL in England [79]. However, it would not be straightforward to apply ion implantation to obtain transistor performance that was comparable to that of double-diffused transistors. This was due primarily to uncertainties in the profile shapes of the ion-implanted impurities, particularly where some channeling of the ions occurred in the low-concentration portions of the profiles.



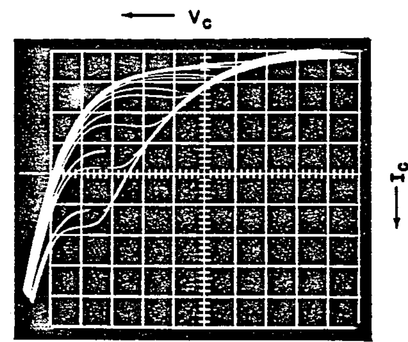


Fig. 19. Drawing of IPC's 1965–1966 prototype p-n-p bipolar transistor obtained by double-ion implantation. This is believed to be the first ion-implanted bipolar transistor. Common-emitter characteristics of these early transistors are also shown (after [34]).

In early 1968, Gusev *et al.* [80] in the Soviet Union fabricated double-implanted p-n-p transistors. The base layer was first implanted with 300-keV P^{+++} ions, and then the silicon was annealed at 1100°C for 2 h. The emitter was implanted with 30-keV B^{+} ions followed by a 900°C, 40-min anneal. The implant doses were either not known or not reported. Devices with gains of 20 and f_t of 350 MHz were reported. However, this performance was not as good as that of comparable double-diffused p-n-p transistors.

For improved high-frequency performance, it was highly desirable to make the depth of the transistor's emitter as shallow as possible to reduce edge emission, which caused a dispersion in base transit times. It was also desirable to form thinner base regions to decrease the emitter-to-collector transit time of injected carriers. If a transistor is fabricated with a very shallow emitter without achieving better control over the net doping in the base regions, a higher unity-gain frequency f_t could be obtained, but this would not necessarily mean that a higher $f_{\max}$ or an improved insertion gain would result, unless the base doping process produced a lower external base resistance. This requirement exceeded the ability of normal diffusion processes to achieve thin, well-controlled bases. Basically, the diffusion process itself had constrained dependencies among the surface concentration of dopants, the junction depth, and the concentration gradient of dopants in the silicon substrate. With ion implantation, one had more flexibility in tailoring these parameters.

In the late 1960's, double-diffused high-frequency n-p-n transistors were fabricated by first establishing a boron-diffused base followed by a phosphorus-diffused emitter. The first ion-implanted devices, made by Kerr and Large [79], had a phosphorus emitter diffused first, followed by an implanted boron base that was then annealed at 800°C. The reversal of steps was necessary to avoid the so-called emitter-push effect caused by the diffusing phosphorus, which induces a cooperative diffusion effect in the boron, resulting in the base's being pushed out ahead of the emitter [81]. The cause of emitter push was not known, and a detailed model of this effect would not be developed until 1976 [82]. As a result, it was not possible to make thin-base n-p-n transistors with existing process sequences. A comparison between the doping profiles achievable with double-diffused and diffused-emitter, implanted-base technologies in 1969 is shown in Fig. 20 [83]. Although a much lower overall base doping was achieved with the ion-implanted base in a shallower device structure, both methods produced approximately the same net active base doping. The disadvantage of this ion-implanted structure was that the external base doping was low (low surface

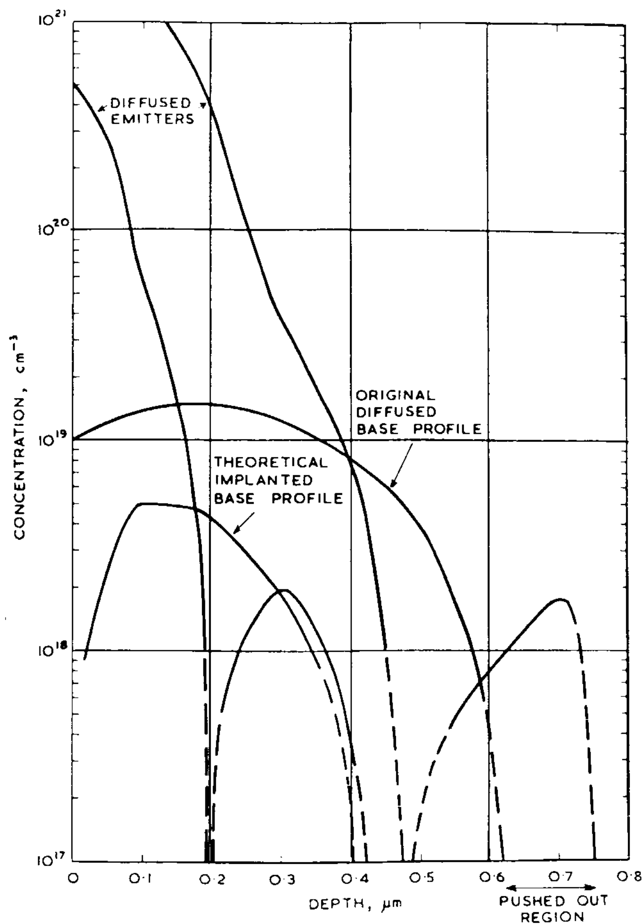
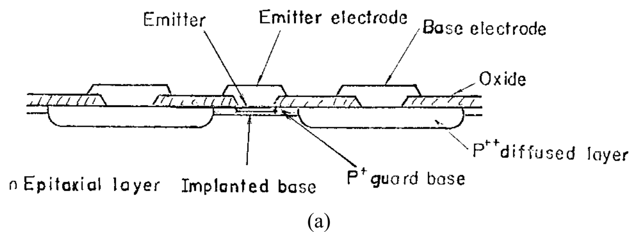
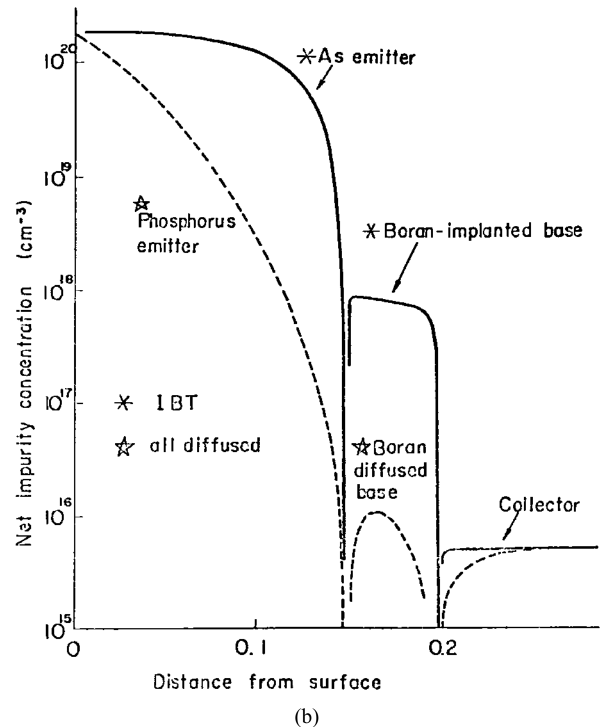


Fig. 20. One-dimensional doping profiles for a double-diffused transistor process (boron base first, followed by a phosphorus-emitter diffusion) compared with a diffused emitter process, in which the boron base is implanted and annealed after the emitter diffusion. The double-diffusion process exhibits the emitter-push effect (after [83]).



(a)



(b)

Fig. 21. (a) The device structure of Toshiba's ion-implanted base microwave bipolar transistor with an arsenic-diffused emitter. (b) The one-dimensional emitter, base, and collector profiles of this transistor. This was the first reported transistor that exceeded the performance of double-diffused microwave transistors (after [85]).

boron concentration), resulting in a large r_b' (external base resistance) for the device. This problem would be solved temporarily by introducing a doped-oxide diffusion into the external base region [76]. The ultimate solution, however, would involve an added ion-implantation step.

B. The Arsenic Emitter

One way to eliminate the emitter-push effect was to substitute arsenic for phosphorus in the emitter-diffusion step. Since arsenic also diffused more slowly than phosphorus and produced more of a "box-like" profile, [84] it was possible to create shallower emitter-base junctions in the range of 1500–3000Å, in which there was no compensation of the base doping by an emitter doping tail. The first group to fabricate a microwave bipolar transistor with a diffused arsenic emitter and ion-implanted base was Fujinuma *et al.* at Toshiba, which was announced at the 1969 IEDM [85]. This work was very significant because it was the first demonstration of the potential of ion implantation to improve transistor performance over what was possible with double-diffusion technology. Toshiba's ion-implanted-base transistors had an f_t of 6 GHz and were low-noise devices. The device structure and the n-p-n profiles obtained in this work are shown in Fig. 21(a) and (b), respectively. The profiles are compared with a double-diffused, phosphorus emitter structure. Shortly thereafter, Fair *et al.* [86] at Bell Labs also produced a similar device, which had superior performance characteristics compared to Bell's standard double-diffused microwave transistors with diffused phosphorus emitters and bases. In the Bell Labs device, the arsenic emitter was diffused first, followed by a 30-keV, 2×10^{14} boron/cm^2 base implant to yield a net base doping of 10^{12}/cm^2. Postimplant annealing was performed at 900°C for 30 min. The devices had low-frequency current gains of 65 and f_t of 7.5 GHz, among the highest ever seen. The emitter-collector leakage were currents less than 2 nA on 90% of the devices. Thus, the new process helped reduce emitter-collector shorts, which were a major yield problem in the standard double-diffused transistor process.

Meanwhile, Hewlett-Packard and Avantek both were having success in the fabrication of microwave transistors. The key to the successful introduction of ion implantation

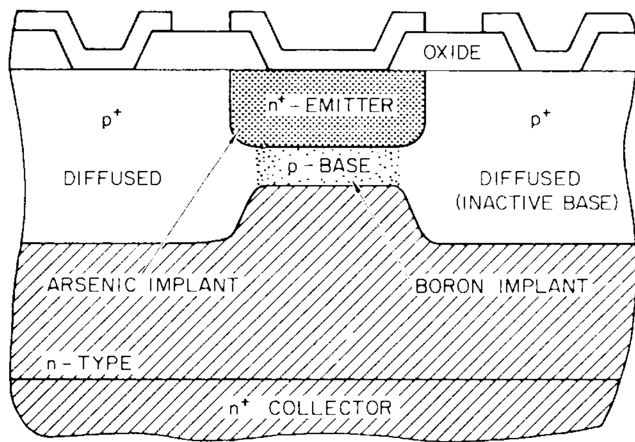


Fig. 22. Cross section of a double-implanted n-p-n transistor from 1972. The external base region was initially formed by a boron diffusion, then the emitter was arsenic implanted and annealed at 1000°C. Last, the active base region was formed by a 200-keV boron implant and annealed at 850°C (after [90]).

for fabricating microwave bipolar transistors was finding a suitable arsenic diffusion source that was reproducible, safe, and produced sufficient arsenic concentrations. Both Toshiba and Bell Labs [87] relied upon an arsenic-doped oxide source that was used in a "washed emitter" process, while IBM used a sealed-ampoule diffusion source described previously. The doped oxide sources were difficult to control and even more difficult to etch away after arsenic predeposition was complete. Texas Instruments viewed the highly toxic arsine gas used in forming the doped oxides as too dangerous for the factory. And the ampoule source showered quartz particles over the wafers during the wafer-extraction procedure.

Encouraged by the success of the diffused-arsenic emitter results and aware of existing arsenic source problems, there was incentive for other workers to begin experimenting with ion-implanted arsenic emitters in the 1972–1974 time frame. If ion implantation could be made to work in this application, there would be no established diffusion method in manufacturing to displace, and introduction of the new technology would be eased. Two approaches were followed: some attempts [88], [89] were based upon the Hughes philosophy of using the low temperature of the ion-implantation doping technique, which would eliminate the "interdependencies of multiple high-temperature diffusions" [64], while others [89], [91] used higher postimplant annealing temperatures (1000°C, 30 min) to drive the emitter profile past the implant-damage region so that the emitter-base junction was located in defect-free silicon. A cross section of the device structure fabricated by Reddi and Yu [90] is shown in Fig. 22.

Low-temperature annealing proved to be unsuccessful in fabricating competitive double-implanted devices. The channeled tail of the emitter implantation, which penetrated the base region, caused uncontrolled base doping compensation, and it was not possible to anneal out the implantation damage in the vicinity of the emitter-base junction at temperatures of 900°C or below. Such damage caused poor minority-carrier lifetimes, which resulted in

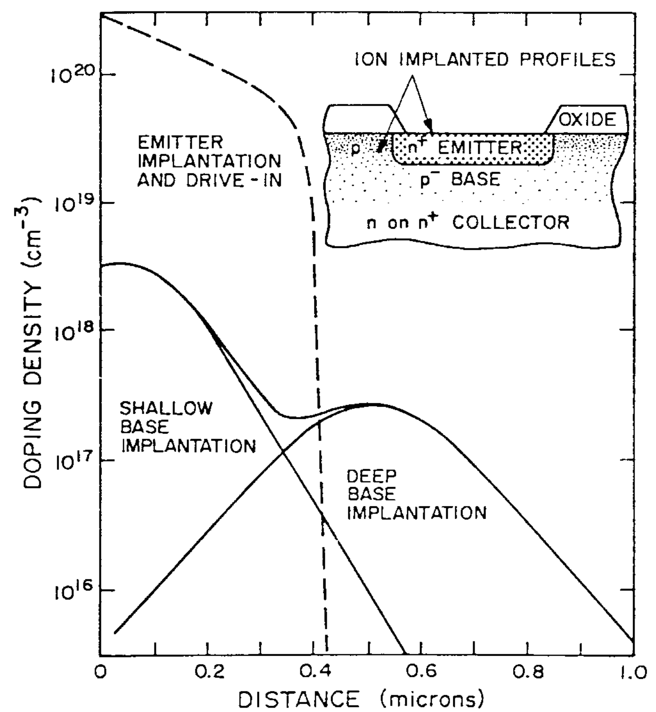


Fig. 23. Carrier concentration profiles of Bell Labs' double-implanted n-p-n transistor from 1972. The processing was similar to that shown in Fig. 21 but the external base was doped by a shallow base implantation step (after [91]).

poor current gain and leaky emitter-base junctions. Thus, it was necessary actually to diffuse the implanted emitter at least a few hundred angstroms to fabricate good transistors. This meant that emitters could be predeposited with a low energy implant and then diffused and activated at high temperature. This method was to become the preferred fabrication approach for many years.

C. Additional Improvements

Additional improvements in the performance of high-frequency bipolar transistors can be attributed to ion implantation. For example, Payne *et al.* [91] simplified Mullard Labs' concept of providing multiple base implants [76] by using only two base implants, one to set the net active base doping and a shallow implant to raise the surface concentration, as shown in Fig. 23. This second implant increased the surface inversion voltage and lowered the external base resistance. Because this process was compatible with bipolar integrated circuit technology, and because the ion-implanted transistors could be made with high performance, reproducibility, and control, this technology was introduced for manufacturing high-speed bipolar IC's at Western Electric, Allentown, PA, in the mid-1970's.

Other improvements came, such as the use of arsenic ion-implanted polysilicon sources for forming shallow, abrupt emitters. Unlike the doped oxide source, the polysilicon source did not have to be removed after the emitter diffusion, but rather it remained as part of the device structure. Improvements in photolithography would bring about the reduction in feature dimensions, which in turn would result

in present-day silicon devices with an f_t of about 35 GHz and an $f_{\max}$ of about 50 GHz. An excellent review of technology advances and performance improvements of bipolar transistors and integrated circuits through the mid-1980's can be found in [92].

VI. Ion-Implanted Integrated Circuits

By 1972, a number of R&D labs were able to start buying their own medium-current ion-implantation systems, such as the production implanter available from Accelerators, Inc. With easy access to machines, the device applications for ion implantation proliferated. At Bell Labs, ion implanters became available at Reading and Allentown, which were the advanced development labs. Members of the technical staff were advised that there would be "no glory" in developing new silicon devices that did not use ion-implantation doping, which was a significant change from earlier Bell Labs management directives. With incentives like this, a plethora of applications emerged at Bell and many other companies, some of which would be critical for use in standard bipolar and MOS integrated circuit processing. Some of these applications are described below.

A. Buried Layers

In bipolar transistors, it was desirable to dope the collector region as high as possible to reduce collector series resistance but also as low as possible to reduce the capacitance of the collector-base junction. Suggestions for using high-energy, channeled implants to create buried collector regions that satisfied both requirements were investigated but were abandoned. This led to the use of diffused buried collectors in silicon substrates over which an epitaxial layer was grown. This method was common in bipolar IC's by 1972. And the advantages of using arsenic over antimony as the buried-layer dopant were also becoming clear, since diffused arsenic produced fewer defects and lower sheet resistance than antimony. The use of ion implantation in forming buried layers was considered, but this high-dose application required a high-current machine. As machines such as the Harwell-Lintott system became available—displacing the Accelerators, Inc., medium-current machines, which were not suitable for the factory—arsenic-implanted buried-layer technology replaced diffused arsenic sources for reasons of safety and control.

B. Integrated Resistors

Ion implantation opened the door to the fabrication of planar resistors. C. M. Kellett, King, and F. W. Martin of IPC filed a patent on January 20, 1966 [93], that described the application of ion implantation to form substitutional dopant impurities for creating precision resistors of a specified resistivity. By ion implanting boron or phosphorus selectively into silicon regions using a patterned silicon dioxide mask, resistor values could be varied either by changing the implant dose or by changing the annealing temperature from 200–750°C. For a given implant dose, the resistivity of the implanted region would decrease with increasing annealing temperatures as more of the implanted interstitial ions became substitutional in the silicon lattice. However, the notion that one could establish a precision resistor process in this way was based on the assumed reproducibility of the damage mechanisms that determined the relative numbers of interstitutional and substitutional implanted doping impurities. Factors such as wafer temperature during ion implantation and dose rates would alter these relationships in unknown ways, making it difficult to control resistor values. The solution was simple: fully activate the implanted dopant impurities at high temperature, placing them all on substitutional lattice sites, and then use dose control and diffusion as the means for determining resistor values and tolerances.

Later work was based upon this simple solution. For example, MacDougall *et al.* [94] relied upon 30-min, 950°C anneals to build ion-implanted, low-area, high-value integrated resistors with good control. In addition, since standard diffusion techniques could only yield a maximum of 200 ohms per square, ion implantation had the potential of attaining 10^4 ohms per square. MacRae reported on the fabrication of ion-implanted, 20-kΩ resistors in 1971, which had a $\pm$3% distribution in their values [95]. Also at Bell Labs, meg-ohm resistors were fabricated with sheet resistances of 120 kΩ per square using an implanted p-layer resistor, which was buried under an implanted n-guard layer [96]. The application for this work was matched resistors for a high input impedance differential preamplifier IC. A match of 0.5% and a magnitude tolerance of $\pm$20% was achieved.

Ion-implanted resistors would not demonstrate the potential of replacing thin-film, precision resistors in high-speed bipolar applications. While in 1972, it was possible to achieve high-value 3σ sheet resistance variations across a wafer of 7–19%, other variations in resistor control such as photolithography and etching would be cumulative. In MOS technology, resistor-transistor logic would yield to ion-implanted depletion-mode NMOS and complementary (C)MOS logic, which did not require resistors except in special applications such as polysilicon load resistors in SRAM memory cells and certain signal-delay circuits.

C. Vertical p-n-p Transistors

In 1972, bipolar IC technology commonly used lateral p-n-p transistors in conjunction with vertical n-p-n transistors. Lateral p-n-p's had relatively low gains that peaked at low currents, with gains falling off rapidly at currents above 500 μA. In addition, they were low-frequency devices. A vertical p-n-p was developed at Bell Labs, Reading, in 1971, which used two boron implants to establish the collector: one as a predeposition source, which was diffused to form the buried p-type collector, and the second made at the surface of the epitaxial layer to compliment the first implant. A phosphorus implant was used to establish the net base doping. This allowed for the fabrication of a complementary p-n-p/n-p-n IC technology that would become the workhorse for telecommunications IC's in the Bell System.

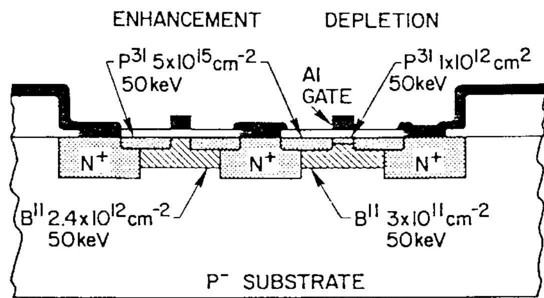


Fig. 24. Cross-section view of a 1-μm gate length IBM MOSFET, which was fabricated with ion-implanted enhancement and depletion devices and an aluminum gate (after [98]).

D. MOS IC Technology

Ion implantation as applied to the development of MOS IC technology spawned many inventive and novel approaches to device fabrication. Most of these inventions, which are too numerous to list, were aimed at either lateral dimensional control or doping density control and included the basic principles embodied in the self-aligned, silicon-gate concept or the threshold-adjust-implant concept, respectively. One early demonstration of a silicon gate, ion-implanted CMOS process was disclosed in an invention by Shappir at Philips filed June 8, 1971 [97]. This invention used ion-implanted threshold adjustment and ion-implanted, self-aligned source/drains. In 1973, Fang *et al.* [98] at IBM combined electron beam lithography with ion-implanted, aluminum-gate technology to demonstrate the first 1-μm enhancement and depletion devices. Low-dose boron and phosphorus implants were used to set the threshold voltages of the enhancement and depletion transistors, respectively, followed by a 970°C, 30-min anneal. The rest of the device was fabricated in much the same way as described by Bower [52], [53], using implanted drain extensions self-aligned to the aluminum gate. The IBM device is illustrated in cross section in Fig. 24.

With the advent of 1-μm MOS technology came the realization that reducing the spacing between the source and drain junctions would lead to undesirable changes in device characteristics such as reduced threshold voltages and punch through. Dennard *et al.* at IBM [66] pointed out that ion implantation could be used to improve the design of small MOSFET's. By implanting a low concentration of dopants in the channel region, it was possible to increase the doping profile selectively under the gate, allowing the use of a lower doping in the substrate to reduce the transistor's body-effect sensitivity. This application was first pointed out by Beale [76] in 1970. The reduced substrate sensitivity allowed the designer to fabricate MOSFET's with thicker gate oxides, which were easier to grow. Second, MOSFET's of small channel length required very shallow source/drains in order to maintain long-channel device behavior. Moderate energy (100 keV) arsenic ion implantation was well suited for this application, accompanied by a modest activation anneal (11 min at 1000°C). A cross-section view of Dennard's ion-implanted device is shown in Fig. 25 and is compared

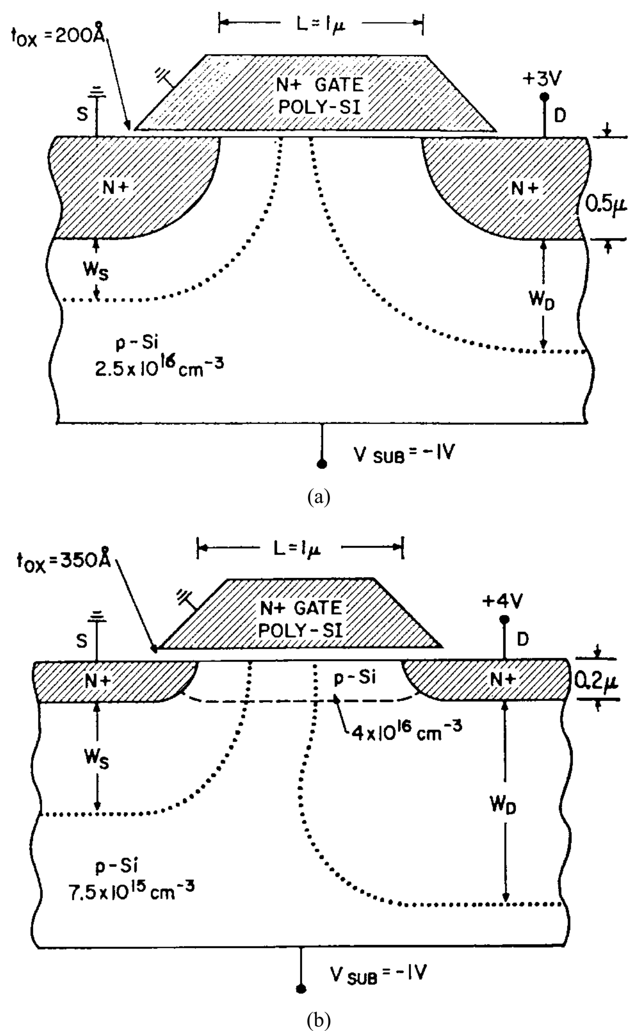


Fig. 25. Detailed cross sections for (a) scaled-down MOSFET structure with diffused source/drains and (b) the corresponding device with arsenic-implanted source/drains and a channel implant (after [66]).

with a diffused device. The shallow source/drains and the surface implant in the channel region combined to give an improved MOSFET whose drain depletion layer extended deeper into the vertical dimension of the substrate, but the lateral extent was curtailed by both the presence of the channel implant and the shallow depth of the drain junction.

Diffused, self-aligned, silicon-gate processing was the prevalent manufacturing technology throughout most of the 1970's among the merchant semiconductor companies. This required that the silicon dioxide covering the source/drain regions be etched away after the formation of the silicon gate so that both the gate and the source/drains could be doped by the subsequent diffusion step. This oxide etching step introduced a reliability problem in that the oxide under the gate itself would also be etched somewhat, leaving behind an undercut region around the perimeter of the gate in which contaminants could be trapped. This contributed to gate-drain shorts, especially if additional layers of polysilicon were to be deposited. One important invention from 1976 that addressed this problem was to reoxidize the silicon and polysilicon so as

to “fill” the undercut with oxide prior to the next process step [99]. However, ion implantation of the source/drain regions removed the necessity of etching the oxide over the source/drain regions, and most manufacturers today still maintain a thin oxide in place rather than removing the oxide after gate patterning.

The reoxidation process also grew oxide on the surfaces of the polysilicon gate, and this feature became the basis for an invention to fix the problem that Bower attempted to address in his ’712 patent in 1966 [46]—vertical alignment of the edges of the source/drain regions with the edges of the gate. In the Bower patent, source/drain implants were self-aligned with the bare edges of the gate to try and achieve “perfect” alignment. It was known at the time, however, that ions penetrated the substrate both in the direction that they were initially traveling (vertical to the silicon surface) and laterally as they underwent scattering with lattice atoms. The lateral “straggle” of an implanted ion could be approximately the same as the vertical straggle. In addition, with silicon-gate technology, any subsequent high-temperature annealing steps would diffuse the dopants even further under the gate. So, to achieve more closely a vertical alignment required that the implant be offset some distance from the edge of the gate. This requirement drove a significant number of inventive ideas, but only one would form the basis for standard modern process technology.

Ryden *et al.* at INMOS [100] used the polyreoxidation step in conjunction with anisotropic etching of that oxide to form side-wall spacers on the gate. These spacers formed an offset space between the edge of the gate and the edge of the source/drain implanted regions, as shown in Fig. 26. The width of the offset was controlled by the oxide thickness and was set by the amount of lateral diffusion that the source/drain implants would experience. Dubbed the “zero-drain-overlap” process, it was allegedly responsible for INMOS’ maintaining its advantage in the fast SRAM business in the mid-1980’s.

In this same time frame, Ogura at IBM [101] invented the lightly doped-drain (LDD) process, which was filed December 17, 1980. To reduce the magnitude of the electric field in the drain-gate region of a MOSFET with gate lengths of 1 μm or less, a light implant was performed prior to the heavy source/drain implant, which created a lightly doped drain extension under the gate. This process differed from the Bower ’934 patent [53], in which the heavily doped source/drains were formed first, followed by a lightly ion-implanted drain extension. A cross section of the device is shown in Fig. 27. Ogura’s LDD implant was aligned to the gate itself, while the source/drain implants were aligned to a regrown oxide on the polysilicon gate. This made it possible to achieve both a shallow source/drain region for purposes of device scaling and a deeper source/drain region that could be easily contacted without metallization-induced junction shorts.

Continued new technological developments in recent years have resulted in an expansion of applications beyond the bounds of conventional implantations performed in the range of 15–200 keV. This range has been extended in energy up to several megaelectronvolts for buried dopant layers and doped “wells” for CMOS devices, as well as down in energy to 500 eV for ultrashallow emitters and source/drains. The range of dopants has extended up to 3×10^{18} ions/cm^2 for applications such as buried dielectric layers and buried epitaxial silicide layers. This has, in turn, driven the development of implantation systems with beam currents up to 100 mA for wafers as large as 300 mm in diameter.

VII. Conclusions

Ion implantation has become an enabling technology that has helped fuel the evolution of the modern integrated transistor. Today, the ion-implantation system, while one of the most complex tools found in modern fabrication facilities, is an indispensable part of a semiconductor manufacturing strategy that is driven by higher and higher levels of control on manufacturing tolerances [1].

The evolution of ion implantation started with the concept of ion bombardment as a radiation-damage effect in the 1950’s. In the 1960’s, engineers began to understand substitutional doping by ion implantation and to see its real potential in device fabrication. In the 1970’s, when critical applications of the technology were realized, ion implanters were put in the hands of many device engineers, who would find more applications and uses of the technology. This is a classic tale of how R&D takes place in the semiconductor industry. Inventions and concepts are most often created within the framework of interest, the mindset of knowledge, and the driving force of necessity. However, a few visionaries such as W. Shockley and those who made fundamental contributions in the 1960’s at Hughes Aircraft Company, Stanford University, Chalk River Nuclear Laboratories, Rockwell, the University of Aarhus, etc. foresaw the real potential of ion implantation in times where seemingly only interest and imagination supported their creativity. Other contributions from IPC, Mullard Labs, Philips, Hughes, GME, SERL, Toshiba, and Bell Labs were made by device-oriented researchers who were interested in trying to find commercial applications for ion implantation. Although excellent work was performed and reported by these groups, no one would really succeed in hitting a home run with ion implantation until the collaboration between Sprague and MOSTEK. The concept of threshold-voltage shifting by implantation had been suggested earlier by others, but no one had used this concept to solve a manufacturing problem. Palmer and Sevin at MOSTEK were introduced to ion implantation at a fortuitous time, when pressing manufacturing problems collided with the right solution. The lesson for all of us in engineering and science is clear: it is fine to embrace the unorthodox ideas that go against the grain of popular opinion or compete with ingrained technology, and one should not discard them until they prove themselves unworkable. But it is even better to apply such ideas to solving real rather than imagined problems. But for the application of ion implantation to such a real problem, the momentum of the past might have carried the development of the silicon transistor down a

United States Patent [19] | [11] **Patent Number:** **4,486,943**
Ryden et al. | [45] **Date of Patent:** **Dec. 11, 1984**

[54] **ZERO DRAIN OVERLAP AND SELF ALIGNED CONTACT METHOD FOR MOS DEVICES**

[75] Inventors: William D. Ryden; Matthew V. Hanson; Gary F. Derbenwick; Alfred P. Gnadinger; James R. Adams, all of Colorado Springs, Colo.

[73] Assignee: Inmos Corporation, Colorado Springs, Colo.

[21] Appl. No.: 588,000

[22] Filed: Mar. 12, 1984

Related U.S. Application Data

[63] Continuation of Ser. No. 331,474, Dec. 16, 1981, abandoned.

[51] Int. Cl.³ H01L 21/265
[52] U.S. Cl. .... 29/571; 29/576 B; 29/578; 29/591; 148/1.5; 156/643; 357/23
[58] Field of Search .... 29/571, 576 B, 577 C, 29/578, 589, 591; 148/1.5, 188; 156/643; 357/23 G, 23 S, 49, 51, 59

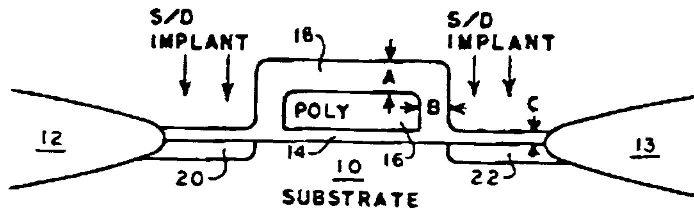


Fig. 26. Cross section of the INMOS zero-overlap MOSFET, which used anisotropic etching of differentially thermally grown oxide on the polysilicon gate to form an implant mask on the sides of the gate. A source/drain implant would then be offset from the gate edges, and high-temperature diffusion was used to diffuse the source/drains laterally into substantial alignment with the gate (after [100]).

United States Patent [19] | [11] 4,366,613
Ogura et al. | [45] Jan. 4, 1983

[54] METHOD OF FABRICATING AN MOS DYNAMIC RAM WITH LIGHTLY DOPED DRAIN

[75] Inventors: Seiki Ogura, Hopewell Junction; Paul J. Tsang, Poughkeepsie, both of N.Y.

[73] Assignee: IBM Corporation, Armonk, N.Y.

[21] Appl. No.: 217,497

[22] Filed: Dec. 17, 1980

[51] Int. Cl.³ H01L 21/26
[52] U.S. Cl. .... 29/571; 29/576 B; 29/577 C; 148/187
[58] Field of Search .... 29/571, 576 B, 577 C; 148/1.5, 187, 188; 357/23 VT

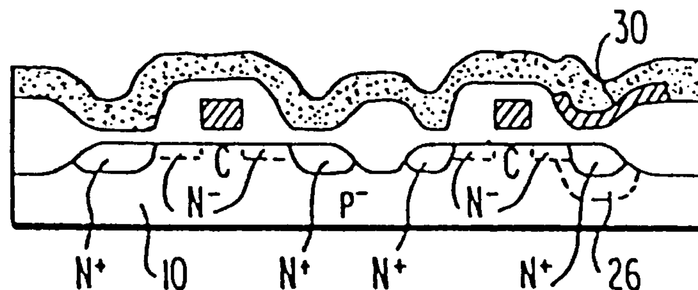


Fig. 27. Cross section of IBM's LDD ion-implanted MOSFET from 1980. The lightly doped n^- regions are implanted after the polysilicon gate is formed and the heavily doped n^+ regions are aligned to the sides of a thick oxide that covers the gate (after [101]).

different path with, perhaps, less successful results at worst and time-delayed improvements at best.

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The author wishes to acknowledge his former colleagues and management at Bell Laboratories, especially L. E. Miller, who enabled him to do some early work on the application of ion implantation to semiconductor device manufacturing technology. This rich and formative experience created the basis for many of his thoughts in this historical review. He also wishes to recognize the reviewers of this paper for their excellent comments, which provided him with course corrections and added insight into key historical events that helped shape the field of silicon microelectronics and ion-implantation technology. Last, it has not been his intention to trivialize the contributions of those who received little or no recognition in this paper. To this end, he encourages the interested reader to gain the additional perspectives found in the reviews by Gibbons [12], [13], Lee and Mayer [63], and Sah [40], all published in this PROCEEDINGS.

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