A 0.46-mm$^2$ 4-dB NF Unified Receiver Front-End for Full-Band Mobile TV in 65-nm CMOS

Pui-In Mak$^1$ and Rui P. Martins$^{1,2}$

1 – State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China
2 – Instituto Superior Técnico, TU of Lisbon, Portugal
E-mails: {pimak, rmartins}@umac.mo

Abstract

This paper describes a unified receiver front-end (RFE) for full-band mobile TV. The performances are advanced in threefold: 1) a gain-boosting current-balancing wideband balun-LNA shows low noise figure (NF), high IIP2 and wideband output balancing concurrently; 2) a current-reuse mixer-lowpass filter (LPF) merges quadrature/harmonic-rejection mixing and 3$^{rd}$-order current-mode post filtering in one block, enhancing linearity and noise just where both are demanding, while saving power and area; 3) a direct injection-locked 4-/8-phase local oscillator (LO) generator involving no frequency division relaxes the master LO frequency. Fabricated in a 65-nm CMOS process, the RFE exhibits 4-dB NF, 35-dB voltage gain and +32/−3.4-dBm out-of-channel IIP2/IIP3 while dissipating 43 to 55 mW. The die area is 0.46 mm$^2$.

Keywords

Balun, CMOS, low-noise amplifier, lowpass filter, local oscillator, mixer, multi-phase, mobile TV, receiver, radio frequency front-end

I. Introduction

Wideband circuits facilitate compact realization of multi-standard radios in expensive nm-length CMOS processes. This paper describes a wideband receiver front-end (RFE) for full-band mobile TV supporting the VHF-III (174 to 248 MHz), UHF (470 to 862 MHz) and L (1.4 to 1.7 GHz) bands. These three bands are where most mobile-TV standards such as terrestrial–digital multimedia broadcasting (T-DMB), integrated services digital broad-casting–terrestrial (ISDB-T),
digital video broadcasting–handheld (DVB-H) and digital multimedia broadcasting–terrestrial (DMB-T) are resided. In order to meet the stringent RF specifications of mobile TV that have been extensively discussed in [1, 2], while avoiding external baluns or multiple narrowband radios commonly found in prior arts, three circuit techniques are enforced [3]. Their backgrounds are introduced as follows.

A wideband balun low-noise amplifier (LNA) can nullify external passive baluns. In addition to the obvious goals of low noise figure (NF), high IIP3 and input impedance match, IIP2 and output balancing are the additional concerns of wideband balun-LNAs. One classical topology is the common-gate (CG) common-source (CS) balun-LNA [4], which employs noise canceling with admittance scaling to achieve low NF. The admittance scaling implies imbalanced loads and bias currents between the CG and CS branches, degrading the IIP2 (+20 dBm). Unbalanced loads also call for output buffers to interface with the mixers to reduce the output gain-phase imbalance. A more recent CG-CS balun-LNA employs IM2 cancellation enhancing the IIP2 by 8 dB [5], but the NF is relatively degraded and the problem of weak output balancing remains unsolved. In this work, an alternative balun-LNA is introduced. It combines gain-boosting (to lower NF) and current-mode balancing (to improve IIP2 and wideband output balancing) concurrently in one block. Output buffers are avoided and variable gain control is embedded via emerging the balun-LNA with a passive attenuator (ATT).

**Harmonic mixing and wideband intermodulation** are critical concerns of wideband RFEs. The former is due to the hard switching nature of most MOS mixers, i.e., the unfiltered in-band blockers located at the harmonics of the LO become the co-channel interferers after downconversion. The latter is due to the potential co-existence of large amount of interferers throughout the passband, rising up the dynamic range requirement of the RFE. In the state-of-the-art, external pre-filtering is still the most reliable way to minimize the harmonic mixing and wideband intermodulation [6]. With adequate pre-filtering, the linearity of the RFE will be mainly justified by the out-of-channel IIP3/IIP2, given that the neighbor TV channels can be 40 to 45 dB higher than the desired one. In this work, a polyphase switch-$g_m$ mixer with selectable harmonic rejection (HR) feature is combined with a 3$^\text{rd}$-order non-OpAmp lowpass filter (LPF) for current-mode post filtering, enhancing the out-of-channel linearity while saving power and area. The
improved on-chip HR ratios relax the rejection profile of the SAW filters, and reduce noise and interference folding in the downconversion.

The last issue that this work will deal with is the generation of a multi-phase LO for the polyphase mixers. The key pitfall of the well-known frequency division method is the necessity of a high master LO frequency \( f_{LO} \), complicating the design of the phase locked-loop (PLL) and voltage-controlled oscillator (VCO). For instance, the frequency range \( \leq 0.9 \) GHz of a wideband RFE with HR [7] is limited by the \( f_{LO} \) (7.2 GHz). In this work, a direct injection-locked 4-/8-phase LO generator (LOG) is proposed. Involving no frequency division the LOG directly lowers the minimum operating frequency of the PLL and VCO.

The paper is organized as follows. Section II introduces the proposed RFE architecture. The conventional and proposed balun-LNAs are studied and discussed in Section III. Sections IV and V describe the proposed current-reuse mixer-LPF and the direct injection-locked 4-/8-phase LOG, respectively. In section VI, experimental results will be shown and the paper ends with conclusions.

![Fig. 1 Proposed full-band mobile-TV RFE.](image)

**II. RFE Architecture**

Figure 1 shows the proposed RFE architecture. Three external SAW filters are expected for band selection as shown in Fig. 2. The integrated part is led by a wideband balun-LNA, which is composed of a gain-control ATT, a single-to-differential gain stage (S2D) and a differential current balancer (DCB). The DCB is tailored to correct the gain-phase imbalance in the current domain, improving wideband output balancing and IIP2 concurrently. The balun-LNA is ac-coupled to the
mixers (not shown) to isolate their bias, and prevent the balun-LNA’s even-order distortion products and 1/f noise from leaking to the baseband (BB).

The I/Q mixers have two operation modes. For the VHF-III and UHF bands, the mixer cells with gain ratios of 1 : √2 : 1 driven by an 8-phase LO [8] perform HR mixing, relaxing the profile of the SAW filter (see Fig. 2) and reducing noise and interference folding. For the L band, the mixer cells are parallelized and the LO is switched to 4 phases as the LO harmonics are located far beyond the frequency range of the SAW filters.

Moving most analog-BB functions to the digital domain allows power and area savings in nm-length processes. Dual practical analog-to-digital converters potentially allow the analog BB to be simply dual 3rd-order LPFs [2]. Additionally, in order to further the power and area reduction, the two BB LPFs are merged with the I/Q mixers.

The 4/8-phase LO is synthesized via a direct injection-locked topology such that the master LO frequency (LOin) generated by the PLL+VCO can be minimized. This LOG scheme particularly suits this application, as the problem of VCO pulling is irrelevant here in the absence of power amplifier.

### III. Wideband Balun-LNAs

#### A. The Noise-Canceling Balun-LNA [4]

Figure 3 depicts the well-known noise-canceling balun-LNA [4]. The S2D uses a CG amplifier (M₁) to generate an in-phase output. The source of M₁ is dc-grounded via an external big inductor.
$L_{\text{ext}}$ to widen the impedance-matching bandwidth (BW). Neglecting the channel-length modulation the impedance-match transconductance of $M_1$ ($g_{m1}$) is 20 mS given that $R_{\text{in}} = 1/g_{m1}$. The S2D uses $M_2$ (CS amplifier) to generate the anti-phase output, and assists noise and distortion canceling of $M_1$. To minimize the noise contribution of $M_2$, $g_{m2}$ should be several times higher than that of $M_1$ (e.g., $g_{m2} = 4g_{m1} = 80$ mS). An imbalance load (i.e., $R_{\text{CS}} = R_{\text{CG}}/4$) cannot ensure wideband balanced outputs when driving balanced loads $C_L$ (e.g., due to the mixers). This fact, in addition to the mismatch of bias currents between the CS and CG branches, contributes to a low intrinsic IIP2 and output balancing precision while making the circuit more sensitive to the supply ($V_{\text{DD}}$) noise. Extra output buffers are also required to minimize the output imbalances that otherwise increase the even-order distortion and dc-offset of the mixer. Last but not least, it is not straightforward to realize a high-linearity low-gain mode in this balun-LNA in case of high power input, i.e., the balun function cannot be simply bypassed, whereas tuning of $R_{\text{CG}}$ and $R_{\text{CS}}$ does not improve the linearity of itself much, and may strong affect other metrics such as NF and IIP3.

![Diagram](image)

**Fig. 3** The conventional CG-CS noise-canceling balun-LNA [4].

### B. Proposed Balun-LNA

The S2D — The principle of the S2D is described first in **Fig. 4(a)-(c)**. An ac-coupled gain stage ($g_{mx}$) enhances the gain of the CS branch [**Fig. 4(b)**], avoiding scaling-up of $g_{m2}$ respect to $g_{m1}$ as in the conventional one [**Fig. 4(a)**]. Moreover, the gain generated by $M_2$ is re-used to enhance the gain of the CG branch by creating a loop gain $(1+A)$ around $M_1$, where $A=|v_{o1n}/v_{in}|$ [**Fig. 4(c)**]. This
act not only boosts the gain and lowers the noise of $M_3$, but also reduces the minimum $I_{DC}$ for input impedance match. In order to save the component count, $g_{mx}$ is realized as an inverter amplifier ($M_3$ and $M_4$) with resistive feedback $R_{fb}$, handily biases $M_1$-$M_2$ and itself. Comparing with the conventional S2D, the bias is simplified, and only one capacitor $C_2$ and one resistor $R_{fb}$ are newly added ($M_3$-$M_4$ can be counted as parts of $M_2$).

Fig. 4  Generation of the proposed S2D: (a) the conventional. (b) AC-coupled gain boosting avoids mismatch of $I_{DC}$. (c) (Final topology) Gain-boosting the CG via the CS, where the gain-boost stage ($g_m$) is a self-biased inverter amplifier ($M_3$ and $M_4$).

The DCB – A balanced load is critical to achieve wideband output balancing. In this work, the balancing is performed in the current domain by inserting a DCB between the S2D and the load, as shown in Fig. 5. The DCB acts as a differential current-control current source with unity gain, forcing $i_{sig+} = -i_{sig-} = i_{sig}$. In principle, a cascode amplifier ($M_5$-$M_6$) with cross-coupled capacitors ($C_3$-$C_4$) might realize the DCB. However, accounting for the finite output resistance of $M_5$-$M_6$, a double-cascode amplifier ($M_5$-$M_8$, $C_3$-$C_6$) is adopted to ensure precise wideband output balancing.
The DCB also benefits the S2D in twofold: 1) the condition \( i_{\text{sig}^+} = -i_{\text{sig}^-} = i_{\text{sig}} \) helps mapping the loop gain of the CG branch to the gain given by the CS branch, yielding \( 1 + A = 1 + \frac{g_{\text{m2}}}{g_{\text{m1}}} \), which is a definable ratio insensitive to process if the channel-length modulation of M1-M4 is neglected. 2) The DCB improves the balun-LNA’s reverse isolation and linearity by lowering the swing at \( v_{o1p} \) and \( v_{o1n} \), where distortion arising from the nonlinear output resistance of \( M_1-M_4 \) can be minimized.

The overhead of the DCB is that it consumes more voltage headroom than a typical cascode stage. In this work, we employ the dual-voltage supplies (1.2 and 2.5 V) offered by the process to enlarge the voltage headroom and assist performance optimization as in [1, 2]. The 2.5-V supply offers more voltage headroom to boost gain and dynamic range concurrently [9]. Moreover, more functions can be performed in the current domain by cascading them, leading to a wider RF BW, better linearity and area savings (i.e., no ac-coupling capacitors between blocks). Nevertheless, high-voltage design with thin-oxide MOS requires node-voltage trajectory checks to ensure no device is under overstressed at all time [9]. In this work, a voltage-conscious bias scheme with extensive simulations meets the reliability guidelines given by the foundry.

Fig. 5 The S2D combined with the DCB. Noting that two voltage supplies (\( V_{DD25} = 2.5 \text{ V} \) and \( V_{DD12} = 1.2 \text{ V} \)) are exploited.
Combining the S2D and DCB, the single-to-differential voltage gain $A_{v,\text{diff}}$ and input impedance $Z_{\text{in}}$ of the balun-LNA can be obtained

$$A_{v,\text{diff}} = \frac{v_{o3p} - v_{o3n}}{v_{\text{in}}} = 2g_{m1}(1 + A)\left(\frac{R_L}{sC_L}\right)$$

and

$$Z_{\text{in}} = \frac{1}{g_{m1}(1 + A)}\left(\frac{1}{sL_{\text{ext}}} + \frac{1}{sC_{\text{in}}}ight)$$

respectively. $A_{v,\text{diff}}$ is limited by $Z_{\text{in}}$ via $g_{m1}$. A strict input impedance match is, however, surplus in practice [10]. The acceptable input reflection coefficient magnitude $\Gamma_{\text{in}}$ can be determined as

$$|\Gamma_{\text{in}}| = \left|\frac{Z_{\text{in}} - R_S}{Z_{\text{in}} + R_S}\right| \leq 0.32$$

It corresponds to a $S_{11}$ value of $< -10$ dB. Accordingly, the tolerable $Z_{\text{in}}$ for $R_S = 50$ $\Omega$ ranges from 26 to 97 $\Omega$. In this work, $Z_{\text{in}}$ is set to 33 $\Omega$ ($g_{m1} = 7.5$ mS and $A = 3$) to enhance $A_{v,\text{diff}}$ and lower NF, while yielding $S_{11} < -13$ dB. The tradeoff is that the impedance matching BW is smaller comparing with strict 50-Ω matching.

![Diagram of the balun-LNA with ATT](image)

**Fig. 6** 1 ATT for coarse gain control using an nMOS-only resistive network.

**The ATT** – The balun-LNA is preceded by a passive ATT for coarse gain control as depicted in **Fig. 6**. It is a triode-biased nMOS-only resistive network. It exploits *signal reflection* and *voltage dividers* to realize the desired attenuation levels. By turning ON either $S_{\text{bypass}}$, $S_1$, $S_2$ or $S_3$, an 18-dB gain-
control range with a step size of around 6 dB is obtained as described in Fig. 7. Operating near the ground (due to the presence of $L_{\text{ext}}$), each nMOS enjoys a large $V_{GS}$ of around 1.2 V to ensure a wide RF BW and high linearity. At the maximum gain, the ATT is bypassed with $S_{\text{bypass}}$; it features a 1.8-$\Omega$ on-resistance ($r_{\text{ON}}$) with an acceptable device size of 200/0.06. The combined $R'_{\text{in}}$ varies between 34.8 $\Omega$ (ATT bypassed) and 55 $\Omega$ (with the ATT). Both values yield $S_{11}<-13$ dB. The initial – 2.2-dB attenuation at the highest gain is induced by the reflection and division between $r_{\text{on}}$ and $R_{\text{in}}$ (i.e., $-2.2$ dB = 20 log $\{1 - (R_{S} - R'_{\text{in}})/(R_{S} + R'_{\text{in}})\} \cdot R_{\text{in}} / (r_{\text{on}} + R_{\text{in}})$).

![Fig. 7 Equivalent circuit of the MOS-only ATT in each gain step.](image)

All MOS switches are operated in triode region with an ON-resistance value that is either $R_{\text{IN}}$ or $2R_{\text{IN}}$. The size of the former is obtained according to

$$\frac{\text{NMOS Switch}}{1} = \frac{1}{\mu C_{OX} \frac{W_{\text{SW}}}{L_{\text{SW}}}(V_{GS,\text{SW}} - V_{\text{TH}})}$$

$$= \frac{1}{\frac{1}{2} \mu C_{OX} \frac{W_{\text{M1}}}{L_{\text{M1}}}(V_{GS,\text{M1}} - V_{\text{TH}})(1 + A)}$$

$$= \frac{R_{\text{in}}}{g_{m1}}$$

(4)
On the left $V_{GS,sw} = V_{DD12}$ since all switched are switched [OFF, ON] by $[0, V_{DD12}]$. On the right $V_{GS,sw} = V_{DD12}/2$, which is set by the self-biased topology of $g_{mx}$ [see Fig. 4(c)]. In the employed process, $V_{DD12}$ is around $4 \times$ of the device’s threshold voltage $V_{TH}$. Accordingly, an aspect ratio of $W_{m1}/W_{SW} = 3/2$ can be obtained by assuming $A = 3$ and $L_{SW} = L_{M1}$. A similar concept applies for the MOS switch with $2R_{in}$ ON-resistance.

There is dc current passing through the ATT. Considering the impedance back to the ATT (labeled as $R_y$), the equivalent resistance at each attenuation step varies between 1.8 to 61.28 $\Omega$. The source of $M_2$, thus, employs an ATT replica to track this variation (Fig. 6), matching the bias currents of the CG and CS branches against gain change.

**Noise Analysis and Performance Optimization** – The NF of the balun-LNA is analyzed based on the simplified noise model shown in Fig. 8. For simplicity, channel-length modulation is neglected and $M_s$ represents $M_2//M_3//M_4$. The transconductance $g_{ms}$ of $M_s$ therefore representing $g_{m2} + g_{m3} + g_{m4}$. $\alpha$ and $\gamma$ showed in Fig. 8 are the process- and bias-dependent parameters of the devices, respectively. The differential output noise voltages due to each source are given by

\[
\begin{align*}
\nu^2_{n,Rs,\text{diff out}} &= |V_{n,Rs}g_{ms}R_L|^2 \\
\nu^2_{n,M1,\text{diff out}} &= |I_{n,M1} \left[ g_{m1}\left(\frac{1+A'}{2}\right)R_S - 1 + \frac{g_{ms}R_S}{2} \right] g_{ms}R_L|^2 \\
\nu^2_{n,Ms,\text{diff out}} &= |I_{n,M1} \frac{2R_L}{1+g_{ms}R_S}|^2 \\
\nu^2_{n,M5,\text{diff out}} &= |I_{n,M5} \left[ \frac{g_{m1}\left(1+A'\right)}{g_{m1}\left(1+A'\right)+\frac{1}{R_S}} - \frac{1}{2} \right] R_L|^2 \\
\nu^2_{n,M7,\text{diff out}} &= 0 \\
\nu^2_{n,RL,\text{diff out}} &= |I_{n,R_L} R_L|^2
\end{align*}
\]

where the loop gain around the CG branch is re-defined as $1+A'$ to match the set assumption in this
Section. With \( g_{m1} = g_{m2} \), \( 1 + A' \) is related with a \( g_m \) ratio as given by

\[
1 + A' = 1 + \frac{g_{m3} + g_{m4}}{g_{m1}}
\]

(11)

Fig. 8 Simplified noise model of the proposed balun-LNA. \( \gamma \) is the excess channel thermal noise coefficient. \( \alpha \) is \( g_m/g_{d0} \) with \( g_m \) the device transconductance and \( g_{d0} \) the zero-bias channel conductance.

The \( NF \) of the balun-LNA can be calculated by dividing the total output noise power due to all devices by the noise power of \( R_S \),

\[
NF = 1 + \frac{v_{n,M1,\text{diffout}}^2 + v_{n,Ms,\text{diffout}}^2 + 2v_{n,M5,\text{diffout}}^2 + 2v_{n,M7,\text{diffout}}^2 + 2v_{n,RL,\text{diffout}}^2}{v_{n,\text{Rs,diffout}}^2}
\]

(12)

If the input impedance matching is exact \( (R_{in} = R_S) \), we can set \( g_{m1}(1 + A') = g_{ms} = 1/R_S \) to simplify (12) as,

\[
NF = 1 + \frac{\gamma}{\alpha} + \frac{2R_S}{R_L}
\]

(13)

This \( NF \) expression is the same as the CG-CS noise-canceling balun-LNA without admittance scaling [11]. For a conservative value of \( \gamma/\alpha = 4/3 \), the \( NF \) is more than 3 dB. In this work, \( R_{in} = 33 \, \Omega \) is set to lower the \( NF \). The factual \( NF \) can be computed via (12).
A 2.5-V supply facilitates the use of a higher $R_L$ to increase the RF gain. The optimum range that can balance IIP2, IIP3 and NF is found to be within 340 to 570 Ω under a 150-fF load as shown in Fig 9. In this region, the NF is <2.8 dB and the IIP2/IIP3 is >+45/+3 dBm. The final chosen $R_L$ is 410 Ω for a maximum intrinsic IIP2, which indeed is fairly stable with respect to $R_L$. The in-band NF justified at boundaries of the desired BW (0.17 and 1.7 GHz) has a difference < 0.1 dB.

![Simulated IIP2, IIP3 and NF with respect to $R_L$.](image)

Fig. 9 Simulated IIP2, IIP3 and NF with respect to $R_L$. The optimum window of $R_L$ is highlighted.

![Automatic Overdrive Protection for $M_1$-$M_4$](image)

Fig. 10 A simple scheme for overdrive protection (the notations are required to Fig. 5).

**Startup Consideration** — Mixed-voltage circuits require the concern of start-up/power-down conditions [12]. As depicted in Fig. 10, in case $V_{DD,12}$ has a delay in start-up with respect to $V_{DD25}$, $M_1$-$M_4$ are in the cutoff region overstressed by $V_{DD25}$. One way of resolving this is to add two small-size thick-oxide PMOS transistors $M_{pt1}$ and $M_{pt2}$ to $v_{o1p}$ and $v_{o1n}$, respectively. With them, the dc
voltages at $v_{o1p}$ and $v_{o1n}$ can be controlled to be within $V_{DD12}$ when $M_1$-$M_4$ are still in cutoff region. Once $V_{DD12}$ ramps successfully, $M_{p1}$ and $M_{p2}$ are automatically turned down. A similar operation holds in power-down condition when $V_{DD12}$ is removed before $V_{DD25}$.

**Differential Balancing** – The progression of gain and phase balancing within the balun-LNA are assessed as shown in Fig. 11(a) and (d), respectively. The gain-phase imbalance are corrected progressively from $[v_{o1p}, v_{o1n}]$ to $[v_{o2p}, v_{o2n}]$, and eventually to $[v_{o3p}, v_{o3n}]$. These results also justify the reason of using a double-cascode structure in the DCB. The in-band gain and phase mismatches are <0.037 dB and <1.87°, respectively. From 0.1 to 10 GHz, the former is still acceptably small (<0.2 dB), whereas the latter is limited at the low frequency side (<3.5°) due to the highpass characteristic of $C_3$-$C_6$ (2 pF) that cannot be oversized due to the add-on parasitics.

![Gain and phase balancing (a) and (b) progress inside the balun-LNA](image)

**Fig. 11** Gain (a) and phase (b) balancing progress inside the balun-LNA.

![Simulated balun-LNA's output gain responses respect to RF$_{in}$, V$_{DD12}$, V$_{DD25}$ and V$_{SS12}$](image)

**Fig. 12** Simulated balun-LNA's output gain responses respect to $RF_{in}$, $V_{DD12}$, $V_{DD25}$ and $V_{SS12}$.

**Sensitivity to Supply and Ground Noises** – The effect of supply and ground noises are worth to assess as the balun-LNA is an unbalanced circuit. As shown in Fig. 12, thanks to a symmetrical $R_L$,
the power-supply rejection ratio (PSRR) with respect to $V_{DD25}$ is $> 48.1$ dB. However, the PSRRs with respect to $V_{DD12}$ and $V_{SS12}$ are just $13.5$ and $12.75$ dB, respectively. These results justify the essential of multiple pads for reducing the bondwire inductance, and ample decoupling capacitors between $V_{DD12}$ and $V_{SS12}$ in the final implementation.

Simulated Performances against Gain Control – Accounting the package effect with 3.5-nH bondwire inductance and 1-pF input parasitic capacitance due to the bondpad and ESD protection circuitry, the simulated NF and S11 against the coarse gain control are shown in Fig. 13(a) and (b), respectively. The in-band NF ranges from 2.5 to 20 dB whereas S11 $<-10$ dB is achieved up to 4 GHz. The linearity metrics at different gain steps are shown in Fig. 14. The *intrinsic* IIP2 is fairly stable, ranging from +45 to +59 dBm, whereas the IIP3 ranges from +5 to +17 dBm. A summary of performance with comparison to the prior arts [4, 5] is given in Table I. Thanks to the dual supplies
(\(V_{DD12}\) and \(V_{DD25}\)), a high voltage gain of 25.6 dB comes with an output –3-dB BW of around 3 GHz at 0.15-pF load, while achieving a high IIP3 of +5.6 dBm. The gain imbalance is reduced by an order of magnitude comparing with [4]. We acknowledge that the comparison is for reference only as the metrics of the proposed balun-LNA are from post-layout simulation (PLS), which the others are from measurements. Nevertheless, the results are consistent with the measurement results of the entire RFE (in Section VI).

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>NF (dB)</td>
<td>2.2 to 2.7</td>
<td>3.5</td>
<td>3.5 to 4.5</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>+5.64</td>
<td>0</td>
<td>+2.5</td>
</tr>
<tr>
<td>IIP2(dBm)</td>
<td>+4.8 to +59</td>
<td>+20</td>
<td>+28 to +35</td>
</tr>
<tr>
<td>Gain Imbalance (dB)</td>
<td>0.037</td>
<td>&lt;0.7 up to 5.2GHz</td>
<td>?</td>
</tr>
<tr>
<td>Phase Imbalance (deg)</td>
<td>1.87</td>
<td>2</td>
<td>?</td>
</tr>
<tr>
<td>RF Gain range (dB)</td>
<td>18</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Diff. Voltage Gain (dB)</td>
<td>25.6</td>
<td>13 - 15.6</td>
<td>27</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>11.6</td>
<td>21</td>
<td>7.8</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2 &amp; 2.5</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Bandwidth (GHz)</td>
<td>0.1 to 2.9 @ 0.15pF load</td>
<td>0.2 to 5.2 @ ? Load</td>
<td>0.17 to 0.89 @ 0.3pF Load</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
</tr>
</tbody>
</table>

IV. I/Q Mixers and LPFs

A. Circuit Description

In typical receivers, the mixer and LPF are in cascade and are interfaced in the voltage domain. Thus, the out-of-channel interferers are amplified at the output of the mixer prior to filtering. Here, we use a current-mode LPF to interface with the mixer, resulting in current reuse and filtering prior to amplification. The I-V conversion is performed at the BB. Figure 15(a) shows the I-channel of the I/Q mixer-LPF. A polyphase double-balanced topology lowers the LO-to-BB leakage and even-order distortion while rejecting the 3\(^{rd}\) and 5\(^{th}\) harmonics of the LO. The mixer core is based on a switched-\(g_m\) cell [13], which is favored against the Gilbert cell in terms of operating voltage and LO amplitude requirement. Moreover, the LO path induces only common-mode noise at the outputs.
that can be rejected differentially. $M_{m1}$-$M_{m4}$ use a large $V_{GS}$ and source degeneration to linearize the $V$-$I$ conversion and mixing.

![Diagram of proposed current-reuse I/Q mixer-LPF topology.](image)

Fig. 15  (a) Proposed current-reuse I/Q mixer-LPF topology.

The LO buffers realized as CMOS inverters use cross-connected weak latches to minimize the duty-cycle distortion. Small LO buffer’s ON-resistance reduces the RF-to-LO coupling since $M_{m1}$-$M_{m4}$ can be well-grounded when they are in ON state. Assuming a square-wave like LO, the conversion gain ($CG$) in 4-phase and 8-phase operations are given by

$$CG_{4p}(s) = c g_{m, eff} \left(2 + \sqrt{2} \right) \left( \frac{R_{BB}}{s C_{BB}} \right) H_{Biq}(s)$$

(14)

and

$$CG_{8p}(s) = c g_{m, eff} \left(2 \sqrt{2} \right) \left( \frac{R_{BB}}{s C_{BB}} \right) H_{Biq}(s)$$

(15)

where $c = 2/\pi$, accounting that only the 1$^{st}$ harmonic of the LO contributes to the gain. $g_{m, eff}$ denotes the effective transconductance of $M_{m1}$-$M_{m4}$ after resistive degeneration. $CG_{4p}(s)$ intrinsically shows 1.6-dB higher gain than $CG_{8p}(s)$ since the polyphase paths in the 4-phase mode
are directly parallelized. This gain difference is indeed helpful as the L band that uses a 4-phase LO is located much close to the –3dB cutoff frequency of the balun-LNA, where more gain droop exists.

Prior to the final I-V conversion at the load, a current-reuse Biquad [14] is added for current-mode filtering [Fig. 15(b)]. Its gain response $H_{\text{Biq}}(s)$, Q and cutoff frequency $\omega_0$ are given by,

$$H_{\text{Biq}}(s) = \frac{i_{\text{out}}(s)}{i_{\text{in}}(s)} = \frac{g_{\text{mf}}^2}{C_{f1}C_{f2}}$$

$(s^2 + s \frac{g_{\text{mf}}}{C_{f1}} + \frac{g_{\text{mf}}^2}{C_{f1}C_{f2}})$

(16)

$$Q = \frac{C_{f1}}{\sqrt{C_{f2}}}$$

(17)

$$\omega_0 = \frac{g_{\text{mf}}}{\sqrt{C_{f1}C_{f2}}}$$

(18)

This Biquad exhibits several advantages: 1) though it is not synthesized with Op-Amps, the Q of the complex pole pair is insensitive to process; 2) there is no passband loss as the current gain at dc is unity; 3) a constant-Q BW control can be achieved with $C_1$ and $C_2$ tuned together; 4) the Biquad exhibits a zero in the noise transfer function of $M_{f1}$-$M_{f4}$ (to be described later), resulting in in-band noise reduction. This property breaks the fundamental $kT/C$ limit as in the classic LPFs that the noise behavior should follow the LPF’s profile; 5) high linearity is achieved since filtering is performed in the current mode, while $C_{f1}$ filters out the high-frequency signals prior they reach the active elements ($M_{f1}$-$M_{f4}$); 6) the noise and linearity are tradable with the cutoff frequency. A higher cutoff rejects more the in-band noise because of the zero exhibited at dc.

These good noise and linearity properties render it a good choice for wireless receivers. Here, by integrating it with the mixer having a real pole load [$R_{88}$/$(1/sC_{88})$], a 3rd-order LPF can be constructed without extra bias currents, $V$-$I$ and I-$V$ converters that dominate the NF [14]. The BB output common-mode voltage is controlled via a common-mode feedback circuit around $M_{L1}$-$M_{L2}$. The targeted cutoff frequency is 12 MHz to balance the NF and selectivity. An automatic cutoff tuning is beyond the scope of this work, but it should be included in the next version to overcome the variation due to process and temperature. A constant-Q BW tuning can be achieved by joint-
adjusting $C_{f1}$, $C_{f2}$ and $C_{BB}$. $M_{f1}$-$M_{f4}$ are realized as thick-oxide MOS with a big device size to minimize NF and reduce channel-length modulation. The latter is essential for an accurate filtering profile.

The protection circuit depicted in Fig. 10 is also applied here at $v_{o1p,BB}$ and $v_{o1n,BB}$ to prevent $M_{m1}$-$M_{m4}$ (thin-oxide devices) from being overstress during the start-up/power-down condition.

\[ H_{Biq}(s) \]

Fig. 16 Noise model of the current-reuse mixer-LPF.

B. Noise Analysis

The simplified noise model of the mixer-LPF is shown in Fig. 16. Similar to the noise analysis in Section III, it can be derived that the single-side band (SSB) NF is given by
where \( C_{BB} \) is omitted and the noise due to the degeneration resistors are ignored to simplify the expression. The first three terms of (19) are originated from the switched-\( g_m \) mixer the same as those derived in [13]. The last two terms are due to the Biquad, both are noise-shaped by an in-band zero as expected.

\[
NF_{SSB,\text{MixLPF}}(s) = \frac{1}{c^2} + \frac{2\gamma_{m,eff}}{g_{m,eff} R_{sc}^2} + \frac{2}{R_{BB}} \frac{2}{R_{sc} c^2 g_{m,eff}^2 H_{\text{Biq}}(s)} + 2\gamma_{mf} \left( \frac{s C_{I_2}}{s C_{I_2} + g_{mf}} \right)^2 + \frac{R_{sc} c^2 g_{m,eff}^2 H_{\text{Biq}}(s)}{\text{LPF contribution}}
\]

\[
(19)
\]

\[
NF_{SSB,\text{MixLPF}}(s) = \frac{1}{c^2} + \frac{2\gamma_{m,eff}}{g_{m,eff} R_{sc}^2} + \frac{2}{R_{BB}} \frac{2}{R_{sc} c^2 g_{m,eff}^2 H_{\text{Biq}}(s)} + 2\gamma_{mf} \left( \frac{s C_{I_2}}{s C_{I_2} + g_{mf}} \right)^2 + \frac{R_{sc} c^2 g_{m,eff}^2 H_{\text{Biq}}(s)}{\text{LPF contribution}}
\]

C. Simulation Results

The filtering characteristic of the mixer-LPF is plotted in Fig. 17. Although the filter works in cascode, the results are similar to those that are in cascade, i.e., the stopband rejection and passband gain increase jointly and progressively. To increase the robustness of the mixer-LPF to process variation and mismatch, a replica-based bias circuit (not shown) is employed. In Monte-
Carlo simulations, the –3-dB cutoff frequency shows a mean of 12.9 MHz with a fairly stable σ of 0.636 MHz as plotted in Fig. 18. The passband gain variation is from 8.6 to 12.2 dB. The 60-dB/dec stopband attenuation is achieved. Other key performances metrics are summarized in Table II.

![Diagram showing Monte Carlo simulation of the mixer-LPF's BB gain responses.](image)

**Fig. 18** 100-time Monte-Carlo simulation of the mixer-LPF's BB gain responses.

**Table II**

Current-reuse mixer-LPF performance summary.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3dB Cutoff (MHz) (Monte Carlo Simulation)</td>
<td>Mean 12.9</td>
</tr>
<tr>
<td></td>
<td>σ 0.636</td>
</tr>
<tr>
<td>LPF Stopband Profile (dB)</td>
<td>60/decade</td>
</tr>
<tr>
<td>Conversion Gain (dB)</td>
<td>10.5</td>
</tr>
<tr>
<td>DSB NF (dB)</td>
<td>15.2</td>
</tr>
<tr>
<td>Out-of-Channel IIP3 (dBm)</td>
<td>+15.7</td>
</tr>
<tr>
<td>Input Capacitance (fF)</td>
<td>43</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>9.8</td>
</tr>
</tbody>
</table>

* 2 tones at [fLO+20MHz, fLO+31MHz]
IMD₃ @ 9MHz, IMD₂ @ 11MHz after mixing
V. Multi-phase LOG

A. State-of-the-art

Multiphase LOGs have been extensively studied in both wireless and wireline applications. Solution based an inverter-based ring-VCO [15] is compact and has wide-range tunability, but the phase noise is still poor for most high-tier wireless systems. Lowering the phase noise promotes the use of coupled LC-VCOs [16]. The overhead is the associated inductors which will occupy lots of chip area. Delay-locked loop (DLL) offers another way to realize a multiphase LOG [17]. Regrettably, since it is based on delay units, the phase-noise performance is heavily depended on the number of output phases required. Currently, the most common solution is LC-VCO plus frequency dividers [7]. For instance, a quadri-phase LO can be generated via a divide-by-2 circuit. This division implies that the associated PLL and VCO have to operate at a doubled frequency of the output. Thus, the design complexity dramatically rises with the number of phases required, not yet mentioning the power, phase noise and phase error overheads. Moreover, the PLL and VCO will be more sensitive to parasitic capacitances, implying narrower locking and tuning ranges, respectively.

B. Open Loop Multi-Phase LO Generator (conventional and proposed)

Recently, an open-loop quadri-phase clock generator for wireline applications was proposed to surmount these constraints [18]. Unlike the active polyphase filter entailing both inverters and capacitors [19], each phase corrector involves only inverters constructed as a ring oscillator with interpolation for multi-phase outputs, resulting in much compact area. The phase precision can be improved by cascading multiple phase correctors in an open-loop way. A master LO direct injection-locks the chain and defines the steady-state frequency. The tuning range depends on the master LO and the lock range of the phase correctors; both can be optimized via proper sizing the associated inverters. The prime advantages of this method are its simplicity (i.e., open loop and inverter only), wideband, no power-hungry buffer and the independence of the number of output phases to the operation frequency of the circuit itself and its driving source. The achieved frequency range in [18] for a quadri-phase output is 0.37 to 2.5 GHz, but the phase error is limited to 5°.
Here, the proposed 4-/8-phase LOG extends such a concept, narrowing the coverage of the LOG by using three chains of 4-/8-phase correctors individually optimized for a narrower BW. As such, and through circuit-level optimization, the phase error can be within 1° (simulation), being more suitable for wireless applications.

![Diagram](image.png)

**Fig. 19** A direct Injection-locked 4-/8-phase LOG.

![Diagram](image.png)

**Fig. 20** The 8-phase path of the LOG: (a) architecture and operating principles, and (b) schematic of each 8PC.

The block schematic of the proposed 4-/8-phase LOG is depicted in **Fig. 19**. It is based on 2 chains of 8-phase corrector (8PC) and 1 chain of 4-phase corrector (4PC); each is dedicated to a specific mobile-TV band for minimum phase error. Selectors, with a logic arrangement feature, allocate the correct clock signals to the mixers in receiving each band. The injection signal LO_in might cover the desired bands by using a 1.27-to-1.92-GHz PLL+VCO [20] (not integrated in this work) with selectable output division ratios (1, 2, 3, 6 and 8). This LO plan corresponds to 3.8x
relaxation of the PLL+VCO’s maximum operation frequency when comparing it with [7]. Note that, here, the required division ratios are flexible (i.e., not necessarily a multiple of 2) as they are unrelated to the phases of LO_out. In the L band, the PLL+VCO works at the same frequency as the RF.

C. Circuit Implementation and Simulation Results

Only the circuit implementation of the 8-phase path is presented as the 4-phase one can be considered as its subset extensively analyzed in [21]. As shown in Fig. 20(a), LO_in drives a chain of all-digital 8PC to progressively improve the phase precision of the 8-phase LO_out. A high-level algorithm has been developed in MATLAB to optimize the device size, number of stage and frequency range using a linearized model [21]. At the transistor level, each 8PC comprises 32 inverters classified into 2 types and 3 sets as depicted in Fig. 20(b). L-type features a larger device size than S-type for optimizing the phase correctability of each 8PC. Set A is to interpolate the intermediate phases. Set B is to suppress the self-oscillation frequency and thereby enlarging the locking range. Set C is for injection lock and direct stage-to-stage cascading. All inverters are realized as thin-oxide MOS to save dynamic power.

The phase precision of the LOG is mainly determined by the transistor intrinsic RC value which is sensitive to the parasitics. The LOG must be laid out and extracted to tune out this effect. In post-layout simulation (PLS), the phase error for 8-phase output is optimized to be <1° for the VHF-III and UHF bands. This precision fairly meets our target of HR ratio of 33 dB, even under a possible gain mismatch up to 5%. For the 4-phase output, the phase error is controlled to be less than 1.5° for the L band, which corresponds to an image rejection ratio of around 38 dB for a possible gain mismatch up to 2.5%.

The phase error degradation is mainly derived from different parasitic capacitances associated with different nodes. The power dissipation in PLS ranges from 4 to 13 mW for frequency from 0.17 to 1.7 GHz, which increase not more than 8% comparing with the schematic simulations.

Similar to ring oscillators, the robustness of the phase corrector can be improved by adopting a supply regulator and a bandgap reference to cope with the voltage and temperature variations, respectively [22, 23]. Simulations show that the supply regulator should show less than 80-mV fluctuation such that the phase noise of the multi-phased LO will not be degraded by more than 1-dB at 1-MHz frequency offset.
VI. Measurement Results

Prototypes of the RFE were fabricated in a 1.2/2.5-V 65-nm CMOS process. The chip micrograph is shown in Fig. 21. The die area is 0.46 mm². A production socket was employed to facilitate statistical tests of multiple samples under the fixture and environment. The I/O pads given by the foundry pass 2-kV Human body Mode (HBM) ESD tests but add roughly 1-pF parasitic capacitance, which have been taken into account in the design phase. Particular attention has been paid to the layouts of the LOG and 8PC. Dummy pre-fill, and optimal place and route minimize parasitic mismatches that can lead to systematic phase error.

A. The RFE

The RFE measures 35±1-dB voltage gain, 4±0.2-dB NF and 43-to-55-mW power consumption over the desired bands [Fig. 22(a)]. The BB gain responses show 60-dB/dec rejection and an untuned cutoff of around 12 MHz [Fig. 22(b)]. This outsized cutoff should be made tunable in practice, according to the demanded channel’s BW. The key distortion specification is justified by the out-of-channel linearity metrics [1]. With two tones applied at [fLO+20 MHz, fLO+31 MHz], the RFE measures an IIP2/IIP3 of +32/-3.4 dBm at the highest gain, and +35/+11 dBm at the lowest gain [Fig. 22(c)]. The measured HRR3/HRR5 is 35/39 dB, aligning with that achieved in a typical HR mixer [8]. Note that to increase the data accuracy; the IIP2/HRR3/HRR5 is averaged from 12 samples with σ of 3.9/1.8/2.4 dB. The worst S11 is close to −10 dB [Fig. 22(d)], which is degraded comparing with the simulations [Fig. 13(b)]. The bondwire, test socket and PCB parasitics should
account for the discrepancy. The $S_{11}$ curves are consistent to the designed values of 34.8 $\Omega$ at high gain mode (without ATT) and 55 $\Omega$ at low gain modes (with ATT).

Based on transient measurements, we can justify that the BB differential outputs [Fig. 23(a)] and I/Q outputs [Fig. 23(b)] are of high-precision balancing, less than 0.5 dB gain and 1.2° phase errors in downconverting a single RF tone from 205 MHz to 1 MHz.
B. The LOG

The performance of the LOG in each band was characterized using a signal generator as LO_in. The phase noise measures a 10-dB/dec roll-off profile [Fig. 24(a)-(c)], which is well below that achieved in [1] which uses a practical PLL+VCO as LO_in. Thus, the phase noise induced by the LOG should be tolerable when the PLL+VCO is present.

The injection-locking characteristic of the LOG is assessed. With LO_in activated, LO_out tracks LO_in at 205 MHz and the dynamic range is >60 dB [Fig. 25(a)]. Note that the 2nd-6th harmonics will be suppressed by the differential I/Q mixer with HR. When LO_in is deactivated [Fig. 25(b)], LO_out is free-running at its natural oscillation frequency (around 240 MHz). The phase noise is degraded and noticeable spurious tones appear throughout the spectrum. These results demonstrated that a high-purity multi-phase LO can be achieved without frequency division.

![Graphs showing phase noise and injection-locking characteristic](image)

Fig. 24 Measured phase noise of the LOG in each band comparing with the data given in [1]. (a) 8-phase at 205 MHz. (b) 8-phase at 655 MHz and (c) 4-phase at 1.55 GHz.

![Graphs showing frequency spectrum](image)

Fig. 25 Measured injection-locking characteristic of the LOG at 205 MHz. (b) Injection-locked at 205 MHz. (c) free-running at around 240 MHz.
C. Performance Comparison

Benchmarking with the state-of-the-art wideband RFEs that attain 4-dB NF [7, 24] in Table III, this work succeeds in extending the operating BW and BB selectivity with comparable power, while reducing the external parts, chip area and fLO that can ease the design of the PLL and VCO. We note that the on-chip HRR can be furthered by incorporating with the 2-stage HR technique [7]. Though the pre-gain pre-filtering technique [24] also can enhance the HRR and lower the power, it involves hard tradeoffs in impedance match, IIP3 and consistency of in-band performances.

Table III
Performance summary and comparison with the state-of-the-art wideband RFEs.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation Frequency fRF (GHz)</td>
<td>0.17 to 1.7</td>
<td>0.4 to 0.9</td>
<td>0.3 to 0.8</td>
</tr>
<tr>
<td>Required Master LO Frequency fLO (GHz)</td>
<td>fLO = fRF (4 and 8 Phases)</td>
<td>fLO = 8 fRF (8 Phases)</td>
<td>fLO = 4 fRF (8 Phases)</td>
</tr>
<tr>
<td>Maximum Gain (dB)</td>
<td>35</td>
<td>34</td>
<td>22 to 28 a</td>
</tr>
<tr>
<td>RF Gain Control (dB)</td>
<td>17 to 35</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>External Components</td>
<td>1 Inductor</td>
<td>2 Inductors and 1 Balun</td>
<td>2 Inductors</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.46</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>BB Filter Order</td>
<td>3rd-Order LPF (1 biquad + 1 real)</td>
<td>2nd-order LPF (2 real poles)</td>
<td>1st-order IIR LPF (minor channel selectivity)</td>
</tr>
<tr>
<td>Power (mW) @ fRF (GHz)</td>
<td>55 @ 1.7 Matched</td>
<td>60 @ 0.9 Matched</td>
<td>18 @ 0.8</td>
</tr>
<tr>
<td>Input Impedance Matching</td>
<td>4 [Spec: 4] *</td>
<td>4</td>
<td>0.8 to 4.3 a</td>
</tr>
<tr>
<td>DSB NF (dB)</td>
<td>-3.4 [Spec: -5] *</td>
<td>3.5</td>
<td>-14 to -9 g</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>32 [Spec: 27] * (Balun LNA)</td>
<td>46</td>
<td>38 to 49 a (Balun LNA)</td>
</tr>
<tr>
<td>IIP2 (dBm)</td>
<td>35</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>HRR3 (dB)</td>
<td>39</td>
<td>64</td>
<td>60</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2 and 2.5</td>
<td>1.2</td>
<td>1.2</td>
</tr>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
<td>65nm CMOS</td>
</tr>
</tbody>
</table>

VII. Conclusions

This paper reports a 65-nm CMOS full-band mobile-TV RFE composed by a gain-boosting current-balancing balun-LNA, dual current-reuse mixer-LPFs and a direct injection-locked 4-/8-phase LOG. External parts and repeated RF circuitry are minimized and the required master LO frequency is relaxed. The achieved performances are comparable with the state-of-the-art
wideband RFEs. The RFE enjoys the availability of dual voltage supplies, thin- and thick-oxide devices, to enhance the performances while maintaining device reliability via voltage-conscious bias. The fabricated prototypes met the key specifications of mobile TV with a small die area of just 0.46 mm².

Acknowledgment

The work was funded by the Research Committee of University of Macau (UM) and Macao Science and Technology Development Fund (FDCT). We thank K.-F. Un (UM) for technical assistance.

References


