A low-cost built-in self-test for CP-PLL based on TDC

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Abstract: To ensure qualification of charge-pump locked-loop (CP-PLL), a complete built-in self-test (BIST) scheme should provide functions of measurement of the clock jitter and detection of faults in CP-PLL. This paper proposes a low cost BIST structure providing both the faults detected and timing jitter measured. The structure based on the proposed time-to-digital converter (TDC), which has high resolution and most blocks of TDC are based on the existing blocks in CP-PLL, reduces the test cost and area overhead. The circuit has been designed and simulated in TSMC 0.13 µm CMOS process. The simulation results show that the resolution is about 0.9865 ps and the fault coverage is 98.33%.

Keywords: BIST, CP-PLL, jitter measurement, fault coverage

Classification: Integrated circuits

References

1 Introduction

CP-PLL is a mixed-signal block widely used to generate timing or reference signals in the system on chip. Its test requirements directly translate into inflated product cost. This provides strong motivation in finding a low-cost test solution for volume production test.

Some conventional low cost Built-in self-test (BIST) designs for CP-PLL are introduced in [1, 2, 3, 4, 5]. In [1, 3, 4], a defect oriented test (DOT) way is used for detecting the faults in CP-PLL. While the method is easily implemented and has little area overhead, it lacks the jitter measurement. However, Jitter measurement is critical to ensure the correct performance of a PLL-based system. Because CP-PLL jitter will yield data loss in communication systems or computation errors in high speed computer systems. The method used in [2, 5] measured the clock jitter of CP-PLL, but it can’t ensure a fault-free CP-PLL. Faults in a PLL can affect the characteristics of the CP-PLL or even most performance of the IC.

Moreover, jitter measurement circuits are revisited to clarify the difference between our proposed circuit and conventional circuits [6, 7, 8, 9]. In [6], a self-referenced clock technique with one T delay was successfully applied to period jitter measurements rather than timing jitter measurements. In [7], a digital controlled delay chain is used to measure the phase offset on chip. However, the frequency of ring oscillator needs to be measured to calculate the time step. The mismatch ratio of two paths is not measured either. A reference-clock-free, high-time-resolution on-chip timing jitter measurement circuit proposed in [8]. To improve time resolution, requires amplifying the time difference between the rising edges of the non-delayed and NT-delayed clocks. Thus, an additional cascaded time difference amplifier (TDA) is needed. The technique reported in [9] does not require an external reference clock but instead uses a delayed version of the test clock to extract timing jitter by accumulating its period jitter. All in all, they are efficient methods for jitter measurement. But they can’t provide faults detected functions for CP-PLL. If the PLL can’t work normally due to the structural faults, these methods will be invalid.

Based on our previous work presented in [4], in which an efficient DOT way is proposed, this paper presents a BIST performing both the faults detected and timing jitter measured based on TDC. The proposed TDC has high resolution and most blocks of BIST are based on the existing blocks in CP-PLL. The combination of structural faults test and function test ensure the qualification of CP-PLL.

2 Proposed BIST architecture

Fig. 1a shows the conventional TDC method. Fig. 1b shows the BIST structure or the proposed TDC, in which a signal process unit, MUX1, MUX2 and a counter are added to an existing CP-PLL. The CP-PLL is composed of phase frequency detector (PFD), charge pump (CP), low pass filter (LF), voltage-controlled oscillator (VCO), and divide-by-N (DBN). MUX1 and
MUX2 are added in the CP-PLL design stage. Time delay caused by MUXs is about 10 ps level. Thus the additional delay created by the MUXs can be incorporated in the original loop characteristics. Fig. 1c introduces the signal process block diagram. The control unit provides five signals: charge test signal (char), discharge test signal (dis_char), the signal which controls the operation mode, the cal signal which calibrates the measurement resolution and the reset signal which disables the counter after a fixed time. The counter evaluates the fault or jitter at the data output. This structure only needs a minor modification of the digital part.

As shown in Fig. 1b, the TDC is mainly composed of the CP-PLL under test. However, unlike the TDC employed a multi-phase VCO generating phase and the system clock in [10], the proposed TDC is mainly composed of the CP-PLL under test which can use any types of VCO. The CP-PLL convert the phase difference ($\Delta T$) into a frequency variation ($\Delta f$). So it can measure timing jitter using only one path without matching the two delay chains. And the reference clock of the CP-PLL can also be used for TDC. Thus, there’s no need for another reference clock. In Fig. 1a, the conventional TDC method for CP-PLL, when the jitter becomes sufficiently small to be in the dead zone of the XOR gate, or when the phase offset is larger than the jitter, it does not function. But the proposed novel TDC structure can detect the jitter on the order of picoseconds or in the presence of a large phase offset.
And as the CP-PLL under test is one part of TDC, the most advantage of the proposed TDC is that it can provide both timing jitter measured and the faults detected to ensure qualification of CP-PLL.

Two clocks Ref.clk and Test.clk with some phase difference $\Delta T$ are given to the signal process unit. PFD detect the phase difference. CP and LF convert the phase difference into a voltage variation ($\Delta V$)

$$\Delta V = \frac{I_{CP}}{C_{LF}} \cdot \Delta T \quad (1)$$

Where $I_{CP}$ is the current magnitude of CP. $C_{LF}$ is the capacitance of LF. Then the frequency of VCO is changed from $f_{vco0}$ to $f_{vco1}$. The frequency $\Delta f$ variation of the DBN output is

$$\Delta f = \frac{f_{vco1} - f_{vco0}}{N} = \frac{K_{VCO}\Delta V}{N} \quad (2)$$

Where $N$ is the factor of DBN, and $K_{VCO}$ is the gain of VCO.

The counter counts the DBN clock edges in time $T_c$ to measure the frequency. If $N_{c1}$ and $N_{c0}$ are the count value in $T_c$ when the DBN frequency is $f_1$ and $f_0$, then the frequency variation and the count difference $\Delta N$ are related as follows:

$$\Delta N = N_{c1} - N_{c0} = (f_1 - f_0)T_c = \Delta fT_c \quad (3)$$

Equations (1), (2) and (3) yield the relationship between the count difference $\Delta N$ and the phase difference $\Delta T$

$$\Delta N = \frac{I_{CP}}{C_{LF}} \cdot \frac{K_{VCO}}{N} \cdot T_c \cdot \Delta T \quad (4)$$

Obviously, the count difference $\Delta N$ is dependent on all of the parameters associated with the CP-PLL and in consequence will reveal any fault associated with these structures. In paper, we will build a structural faults model used in [11], to demonstrate the effectiveness of BIST technique. The structural faults include: gate-to-drain short (GDS), gate-to-source short (GSS), gate-open (GO), drain-to-source short (DSS), drain-open (DO), source-open (SO), capacitance-short (CS), Resistor-short (RS), resistor-open (RO).

Equations (1), (2) and (3) also yield the relationship between $\Delta T$ and $\Delta N$

$$\Delta T = \frac{N \cdot C_{LF}}{I_{CP} \cdot K_{VCO} \cdot T_c} \cdot \Delta N, \quad \Delta N \geq 1 \quad (5)$$

$$\Delta N = 1 \Rightarrow \Delta T_{min} = \frac{N \cdot C_{LF}}{I_{CP} \cdot K_{VCO} \cdot T_c} \quad (6)$$

As shown in (5) (6), the count difference yields the phase difference. The parameter $\Delta T_{min}$ represents the measurement resolution.

### 3 Circuit operations

Table I lists the operations of the proposed BIST structure. The structure uses two operating modes: test mode for testing and normal mode for clock generation.

To clarify the basis of the proposed BIST structure, Fig. 2 illustrates the
test procedure. It includes three steps: step1) structural faults test; step2) jitter measurement; step3) normal mode. The CP-PLL which only passes the step1 can come to step2, then only passes the step2 can come to step3.

<table>
<thead>
<tr>
<th>Test mode</th>
<th>Structural faults test</th>
<th>Jitter Measurement</th>
<th>Normal mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Charge-test</td>
<td>Discharge-test</td>
<td>Calibrate</td>
</tr>
<tr>
<td>Test</td>
<td>Char</td>
<td>Dis_char</td>
<td>Cal</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

### Table I. Operations of the proposed BIST structure

**3.1 Structural faults test**

The proposed BIST structure uses CP as a stimulus generator and employs the counter as measuring devices for testing the deviation of the oscillation frequency. The output thus is a pure digital value, increasing the reliability of the test output. The charge-test and discharge-test operations are addressed here by choosing appropriate MUXs signals from the signal process unit. As described in (4), the count value variation indicates a faulty circuit in the loop. Notably, if the test time $T_c$ is too short, a slight deviation of the oscillation frequency may not be indicated for $\Delta N < 1$. However, with growth of $T_c$, the deviation of the oscillation frequency could be accumulated and be detected after a few microseconds. Finally, reset signal can act as a scan clock to scan out the values at the output of the counter for testing evaluation. The

**Fig. 2.** Test procedure of the proposed BIST structure

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final output $N_c$ depends on clock signal reset and the number of observation points. It shows the timing diagram of the structural faults test operation in Fig. 3.

![Timing Diagram](image)

**Fig. 3.** The timing diagram of structural faults test

### 3.2 Jitter measurement

In the jitter measurement mode, the BIST process repeats two steps—CP-PLL tracking and counting. The tracking step is the lock-in process of the CP-PLL. When there is a time difference $\Delta T$ between reference clock and feedback clock, the CP-PLL stops working immediately. In counting step, the CP-PLL as one part of TDC detects the $\Delta T$. The frequency of VCO varies with the change of output voltage of LF and the counter counts the number of pulses from the DBN output. The durations of tracking step should be longer than lock-in time of the CP-PLL and the settling time of the LF. The duration of counting is equal to $T_c$ in (5).

The parameter $T_c$ should be carefully designed, because it determines the measurement resolution $\Delta T_{\text{min}}$. The range of $T_c$ can be decided by the specifications of CP-PLL, as shown in (6).

The specifications of CP-PLL used in the paper are shown in Table II. Supposed $\Delta T_{\text{min}} < 1$ ps, then

$$\Delta T_{\text{min}} = \frac{64 \times 110 \times 10^{-12}}{120 \times 10^{-6} \times 130 \times 10^6} < 1 \times 10^{-12} \Rightarrow T_c > 0.4513 \text{ s} \quad (7)$$

For longer $T_c$, $\Delta T_{\text{min}}$ is higher, but the test time also increases. Here $T_c$ is designed to 0.5 s.

The measurement resolution $\Delta T_{\text{min}}$ of TDC in (6) must be firstly calibrated. When signal cal is set to logic 0, the phase difference between input clocks equals to 0. The value of the counter $N_0$ is recorded. When signal cal is set to logic 1, then using the clock period of reference clock $T_{\text{ref}}$ yields an

<table>
<thead>
<tr>
<th>Table II. CP-PLL specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CP}$</td>
</tr>
<tr>
<td>120 (µA)</td>
</tr>
</tbody>
</table>
accurate pulse width to calibrate the TDC. The phase difference \( T_{\text{ref}} \) changes the voltage of the LF and the frequency of the VCO. The count \( N_{\text{test}} \) of the counter can be obtained. The count \( N_0 \) and \( N_{\text{test}} \) are not a fixed value for the frequency of VCO varies. It is known as the period jitter. Repeating the calibration process a particular number of times produces a histogram of different \( N_{\text{test}} \) and \( N_0 \). Then

\[
T_{\text{ref}} = \Delta T_{\min}(\overline{N_{\text{test}}} - \overline{N_0}) \Rightarrow \Delta T_{\min} = \frac{T_{\text{ref}}}{\overline{N_{\text{test}}} - \overline{N_0}}
\] (8)

Where number \( \overline{N_{\text{test}}} \) is the average value of \( N_{\text{test}} \), \( \overline{N_0} \) is the average value of \( N_0 \).

3.3 Normal mode

In normal mode, the MUX1, MUX2 select the input and feedback signals of the CP-PLL to be bypassed. The CP-PLL is used for clock generation. This mode is only available for qualified CP-PLL which passes test.

4 Simulation and performance comparison

The proposed BIST structure for CP-PLL has been designed and simulated using TSMC 0.13 µm CMOS technology. The operating frequency of the PLL is 1.6 GHz. The reference clock operates at 25 MHz. A HSPICE simulator was used in this paper to evaluate the efficiency of our low-cost test strategy.

During charge-test operation and discharge-test operation, four observation points are chosen \((T_c = 1 \text{ us}, 4 \text{ us}, 9 \text{ us}, \text{ and } 13 \text{ us})\) for testing evaluation respectively where the value of \( N_c \) is equal to “26, 101, 226, 326,” and “25, 100, 225, 325,” in the fault-free case. The final test outputs are listed in Table III according to the fault model assumptions in Part II. The total number of structural faults in the CP-PLL is 717. According to the simulation results, 705 faults can be detected and the fault coverage for the proposed architecture comes out to be 98.33% \((705/717 \times 100\%)\).

In jitter measure mode, the measurement time \( T_c \) is designed to be 0.5 second. The average count \( \overline{N_0} \) and \( \overline{N_{\text{test}}} \) are calculated at 48160 and 23171, then

\[
\Delta T_{\min} = \frac{4 \times 10^{-8}}{23171 - (48160 - 2^{10})} = 0.9865 \text{ ps/count}
\] (9)

Each output value of the BIST in the jitter measure mode represents the phase difference between the reference clock and the feedback clock. Since \( \Delta T_{\min} \) was calibrated, the jitter magnitude can be determined by simply multiplying the output values of the BIST by 0.9865. The Fig. 4 shows the PDF histogram of jitter (rms: 8.1159 ps) and jitter measured results (rms: 9.0828 ps) using the proposed circuit. The measurement error is 11.91%. The

<table>
<thead>
<tr>
<th>Fault Types</th>
<th>GDS</th>
<th>GSS</th>
<th>GO</th>
<th>DSS</th>
<th>DO</th>
<th>SO</th>
<th>RS</th>
<th>CS</th>
<th>RO</th>
<th>all</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault Coverage (%)</td>
<td>100</td>
<td>95.1</td>
<td>92.8</td>
<td>96.9</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>100</td>
<td>98.33</td>
</tr>
</tbody>
</table>
p-p jitter and the rms jitter of the PLL measured by the BIST circuit in this case are 46 ps and 17.25 ps.

The summary of the comparisons with other techniques is presented in Table IV. The proposed CP-PLL BIST structure has a little influence on the circuit performance. The locking times for the CP-PLL with and without the added BIST circuits are 5 us and 5.2 us respectively. The BIST circuit can perform both the faults detected and jitter measured of the CP-PLL, which only needs a counter, some DFFs and MUXs for low cost. But the measurement time is too long for the high resolution and unfortunately, it can’t diagnose the type of faults in this paper. That’s our future work.

### Table IV. Comparison with other PLL testing techniques

<table>
<thead>
<tr>
<th>Reference</th>
<th>[1]</th>
<th>[2]</th>
<th>[3]</th>
<th>[4]</th>
<th>[5]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Testing scheme</td>
<td>Defect Oriented</td>
<td>Time-to-voltage Oriented</td>
<td>Defect Oriented</td>
<td>TDC</td>
<td>Defect Oriented +TDC</td>
<td></td>
</tr>
<tr>
<td>Loading Problem</td>
<td>Solved</td>
<td>Solved</td>
<td>Solved</td>
<td>Solved</td>
<td>Solved</td>
<td>Solved</td>
</tr>
<tr>
<td>Loop Type</td>
<td>Broken</td>
<td>Not broken</td>
<td>Broken</td>
<td>Broken</td>
<td>Broken</td>
<td>Broken</td>
</tr>
<tr>
<td>Cost</td>
<td>Low</td>
<td>Little high</td>
<td>Low</td>
<td>low</td>
<td>low</td>
<td>Low</td>
</tr>
<tr>
<td>Jitter measured</td>
<td>N/</td>
<td>Y/</td>
<td>N/</td>
<td>N/</td>
<td>Y/</td>
<td>Y/</td>
</tr>
<tr>
<td>/resolution</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1.17 ps</td>
<td>0.9865 ps</td>
</tr>
<tr>
<td>Fault detected/</td>
<td>Y/</td>
<td>—</td>
<td>Y/</td>
<td>Y/</td>
<td>N/</td>
<td>Y/</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>96.5%</td>
<td>—</td>
<td>97.9%</td>
<td>98.18%</td>
<td>—</td>
<td>98.33%</td>
</tr>
</tbody>
</table>

*Y* represents measured results.

## 5 Conclusion

This paper introduces a low-cost BIST structure for CP-PLL based on TDC. The proposed TDC has high resolution and most of TDC blocks are based on the existing blocks in CP-PLL. It provides both jitter measured and faults detected to ensure qualification of the CP-PLL. It has a little influence on CP-PLL performance. The simulation results show that the resolution is about...
0.9865 ps and the fault coverage is 98.33%. The BIST circuit is implemented in TSMC 0.13 µm CMOS process.

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