VCS
Functional Verification Choice of Leading SoC Design Teams

Overview
Industry-leading designers of today’s most advanced designs rely on the Synopsys VCS® functional verification solution for their verification environments. In fact, a high majority of designs at 32nm and below are verified with VCS. Used by a majority of the world’s top 20 semiconductor companies as their primary verification solution, VCS provides high performance simulation engines, constraint solver engines, Native Testbench (NTB) support, broad SystemVerilog support, verification planning, coverage analysis and closure, and an integrated debug environment.

VCS has continually pioneered numerous industry-first innovations, and is now poised to meet the challenges and complexity of today’s SoCs. With features such as such as constrained random testbench, SoC optimized compile flow, coverage, assertions, planning and management, VCS has the flexibility and capabilities that are critical for today’s SoC design and verification teams’ success.

VCS offers industry-leading performance and capacity, complemented by a complete collection of advanced methodology-aware testbench and constraint debug features, bug-finding, coverage, planning and assertion technologies. VCS’ multicore technology delivers a 2x verification speed-up and cuts down verification time by running the design, testbench, assertions, coverage and debug in parallel on machines with multiple cores (see Figure 1). VCS’ Partition Compile flow allows users to achieve up to 10 times faster compile turnaround time by only recompiling code that has changed. VCS also supplies a comprehensive suite of diagnostic tools, including simulation memory and time profiling, interactive constraint debugging, smart logging, and more to help users quickly analyze issues. VCS with native low power simulation and UPF support, delivers innovative voltage-aware verification techniques to find bugs in modern low power designs with integrated debug and high performance. With its built-in debug and visualization environment; support for all popular design and verification languages, including Verilog, VHDL, SystemVerilog, OpenVera™, and SystemC™; and the VMM, OVM, and UVM™ methodologies, VCS helps users develop high-quality designs.

Figure 1: Multicore support
High-Performance, Full-Featured, Native Testbench and Industry-Leading Systemverilog Support

VCS’ Native Testbench (NTB) technology provides built-in natively-compiled support for full-featured SystemVerilog and OpenVera testbenches, including object-oriented, constrained-random stimulus and functional coverage capabilities. VCS’ industry-leading, high-performance constraint solver technology is powered by multiple solver engines that simultaneously analyze all user specified constraints to rapidly generate high-quality random stimulus that verifies corner case behavior. The constraint solver engines will find a solution to user constraints, if one exists, minimizing constraint conflicts and maximizing verification productivity.

VCS further expands its capabilities with Echo constraint expression convergence technology. Echo automatically generates stimuli to efficiently cover the testbench constraint space, significantly reducing the manual effort needed to verify large numbers of functional scenarios. Echo is a perfect fit for all teams using SystemVerilog testbenches with random constraints.

VCS also provides a rich set of engines for reducing compile turnaround time and runtime, including pre-compiled IP support targeted at IP integration, Partition Compile to isolate portions of the testbench that are not changing during development cycles, dynamic reconfiguration to compile for a target and select which model is used at runtime, and save and restore functionality to save common states and apply them to subsequent runs reducing simulation time. Combined, these tools offer the most comprehensive set of solutions to maximize simulation efficiency and reduce turnaround time.

Multicore Support

VCS’ multicore technology allows users to cut verification time for long-running tests. It offers two robust use models: design-level parallelism (DLP) and application-level parallelism (ALP). DLP enables users to concurrently simulate multiple instances of a core, several partitions of a large design, or a combination of the two. ALP allows users to run testbenches, assertions, coverage, and debugging concurrently on multiple cores. The combination of DLP and ALP optimizes VCS’ performance over multicore CPUs. VCS’ multicore technology also supports design-level auto-partitioning, Fast Signal Database (FSDB) parallel dumping, and switching activity interchange format (SAIF) parallel dumping.

Comprehensive Coverage

VCS provides high-performance, built-in coverage technology to measure verification completeness. Comprehensive coverage includes code coverage, functional coverage and assertion coverage as well as user-defined metrics. Unified coverage aggregates all aspects of coverage in a common database, thereby allowing powerful queries and useful unified report generation. The unified coverage database offers 2x to 5x improvement in merge times and up to 2x reduction in disk space usage, which is critical for large regression environments (see Figure 2).

Complete Assertion Technologies

The native assertion technology in VCS enables an efficient methodology for deploying design-for-verification (DFV) techniques. The built-in support of SystemVerilog and OpenVera assertions allows designers to easily adopt DFV and find more bugs quickly. A rich assertion-checker library and a unique library of Assertion IP make it even easier to deploy assertions across teams and improve verification quality. The assertions serve both simulation and formal property verification environments.

Figure 2: Unified coverage
Advanced Debugging and Visualization Environment

VCS includes the Discovery Visualization Environment (DVE), an advanced, full-featured debug and visualization environment (see Figure 3). DVE has been specifically architected to work with all of the advanced bug-finding technology in VCS and shares a common look and feel with other Synopsys graphical-based analysis tools. DVE enables easy access to design and verification data along with an intuitive drag-and-drop or menu-and-icon driven environment.

Transaction-level debug is seamlessly integrated into DVE, allowing users to analyze and debug transactions in both list view and waveform view. Its debug capabilities include: tracing drivers, waveform compare, schematic views, path schematics, and support for the highly efficient Synopsys compact VCD+ binary dump format. It also provides elegant mixed-HDL (SystemVerilog, VHDL and Verilog) and SystemC/C++ language debugging windows, along with next-generation assertion tracing capabilities, that help automate the manual tracing of relevant signals and sequences. DVE further provides powerful capabilities for SystemVerilog testbench debug (including UVM, VMM and UVM methodologies) with several key features, including methodology-aware debug panes, object and component hierarchy browsers, and detailed constraint debug and constraint conflict resolution (see Figure 4).

TCL support is provided for interaction or batch control and skin/menu customization. Unified command language support provides a common set of commands for all tools, languages and environments, making it easy to deploy new technology across design teams.

VCS Planning and Management Package

VCS provides a scalable and integrated planning, management, and analysis package for metric-driven verification. Through the use of a centralized database and common planning format, the VCS Planning and Management Package acts like a project’s “GPS”: tracking coverage and test data in order to correlate results with project goals and resources, so teams know where they are in the verification process and where they have allocated resources.
VCS offers a plan authoring and management tool, the Verification Planner, which imports plans, and back annotates coverage metrics and tracked statistics onto these plans. Verification Planner has been fully integrated with the Discovery Visualization Environment (DVE) Coverage GUI allowing drag-and-drop style plan editing. Through the DVE Coverage GUI, users can visualize structural, assertion and functional coverage. Verification Planner’s plan format is interoperable with VCS’ automated UVM-compliant RALGEN utility, and our Discovery VIP built-in coverage plans, allowing users to seamlessly integrate register and protocol verification into their overall verification plan. Verification Planner’s robust ecosystem allows VCS users to quickly track projects across a wide range of tools.

VCS also provides an integrated management solution, the Execution Manager, which helps balance the tools and techniques that drive projects toward closure. Execution Manager provides a Web-based UI providing test filtering, on-the-fly visibility, real-time regression monitoring, debug triage and regression trend charting. Execution Manager provides an extensible infrastructure allowing home-grown scripting to be integrated without manual maintenance. Through this flow, Execution Manager provides flexible automated infrastructure management improving time to coverage closure, and enhancing the ability of geographically diverse teams to coordinate their efforts and accurately estimate schedules.

Finally VCS’ powerful Unified Report Generator (URG) enables fast grading, merging, test correlation and filtering of coverage data. URG also allows users to create detailed trend analysis reports of plan data over time. URG and DVE use a common database format so customers have the choice of viewing data either interactively or statically as HTML reports. Complex analysis such as adaptive exclusion can be executed using this integrated approach. URG is the most powerful report management and analysis engine on the market.

Together, the integrated VCS Verification Planning and Management Package allows customers to plan, analyze, and manage coverage and verification project data in order to drive projects to completion effectively. The combined solution is the most robust and extensible flow in the industry with deep integration into UVM, Discovery VIP and low power flows (see Figure 5).

Support for Accellera UVM, VMM, and OVM

VCS’ powerful testbench engines are complemented by support for VMM, OVM 2.1.1, and the Accellera UVM methodologies. With these methodologies, users adopt industry best practices to get the optimum results from VCS. In addition, the VMM methodology provides a number of applications, such as Register Abstraction Layer (RAL) and others, to cut down on the time it takes to set up a powerful verification environment.

VCS’ support for Accellera UVM also includes access to the VMM/UVM interoperability kit, which enables the use of VMM with UVM and vice versa. VCS also provides a rich set of template generators for UVM, VMM, and the Register Abstraction Layer as well as wrappers for automatic TLM connectivity. All methodology applications, a detailed reference manual and examples are provided with the VCS solution.

Figure 5: DVE Coverage GUI detail pane synchronized with main planner pane
**Diagnostic Tools**

VCS provides a broad suite of diagnostic tools to help customers resolve issues quickly. From profiling to smart log capabilities integrated with DVE, the VCS Diagnostic tool suite saves engineers time (see Figure 6). Runtime failure diagnostics, loop reports, timescale dialogues, switch summaries, and sanity checks are currently implemented with more functionality planned. The VCS Diagnostic tool suite improves turnaround time when issues occur.

**Native Low Power Simulation**

MVSIM native low power (LP) provides VCS with comprehensive native low power verification and debug capabilities. VCS native low power simulation maintains VCS’ ease-of-use and adoption for low power design by allowing VCS to directly read UPF low power design intent, offers minimal degradation in performance and capacity versus non-LP VCS simulation, enables easy LP debug by enabling advanced LP features in DVE, and provides excellent support for LP assertions and coverage for methodology-driven verification flows (see Figure 7).

**Synopsys Verification IP**

Discovery™ Verification IP (VIP) is architected to address the challenge of verifying today’s highly sophisticated and complex bus protocols. Built upon the proven VIPER Architecture, Discovery VIP is written entirely in SystemVerilog and natively supports UVM, VMM and OVM. It includes built-in coverage, sequences and integrated coverage plans that work with the VCS coverage IDE and planning flow. With faster bring-up time, greater performance, better debug, and shorter time to coverage, Discovery VIP is ideal for verifying the most complex protocols and SoC designs. VCS is further optimized for best performance, capacity, debug and coverage features with Synopsys’ Verification IP.

For more information about VCS, please visit:  
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