Radiation-Induced Soft Error Analysis of SRAMs in SOI FinFET Technology: A Device to Circuit Approach

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ABSTRACT

This paper presents a comprehensive analysis of radiation-induced soft errors of SRAMs designed in SOI FinFET technology. For this purpose, we propose a cross layer approach starting from a 3D simulation of particle interactions in FinFET structures up to circuit level analysis by considering the layout of the memory array. This approach enables us to consider the effect of different factors such as supply voltage and process variation on Soft Error Rate (SER) of FinFET SRAM memory arrays. Our analysis shows that proton-induced soft errors are becoming important and comparable to the SER induced by alpha-particles especially for low supply voltages (low power applications). Moreover, we observe that the ratio of Multiple Bit Upset (MBU) to Single Event Upset (SEU) is higher than that of proton.

1. INTRODUCTION

Further scaling of the planar bulk CMOS technology beyond 22nm is expected to be difficult due to short channel effects [1]. To overcome the scaling limits of this conventional CMOS technology, the Fin Field Effect Transistor (FinFET) is one of the most promising candidates [2, 3]. This is due to the fact that FinFET exhibits superior immunity to short channel effects. Moreover, the effect of process variation on FinFET device performance is less compared with conventional bulk devices [4, 5]. FinFETs can be fabricated as a bulk device or on silicon-on-insulator (SOI). However, FinFET has been mainly fabricated on SOI [6, 7] due to lower junction capacitance, higher mobility, and voltage gain with reduced mismatch compared to bulk devices [8].

One of the most important issues which has to be studied carefully in these structures is the effect of radiation-induced soft errors. Although the radiation effect is well studied for conventional bulk CMOS technologies, there are few studies on FinFET technology. The previous studies can be categorized into two groups:

1) Device level studies [9, 10, 11, 12, 13]: In [9], the behavior of three different multi-gate transistor structures (Double gate, FinFET and All-Around MOSFET) under heavy ion irradiation is analyzed using 3-D device simulations. A 3-D TCAD device model is used in [10] to describe the I-V characteristic of SOI FinFET transistors and their transient response to radiation. In [11], the critical charge and single event upset sensitivities of SRAM cells in bulk and SOI FinFET technologies are obtained and compared using TCAD simulations. The Neutron-induced charge collection is estimated and compared for bulk FinFET and conventional CMOS using a mixed-mode 3-D TCAD in [12]. Authors in [13] present a model to estimate the transient charge collection induced by energetic particles for the SOI FinFET technology.

2) Circuit level studies [14, 15, 16]: The critical charge of a SRAM cell, a simple inverter and a logic chain is obtained for bulk CMOS and FinFET technologies in [14]. The authors used a double exponential current source model [17] to estimate the Soft Error Rate (SER) at a node. In [16], different FinFET technologies are studied using a 3-D TCAD tool to obtain the minimum radiation dose required to flip SRAM cells.

All the aforementioned studies either focus on device or circuit level. The studies at device level are more accurate. However, due to the high runtime of these techniques, it is intractable to apply them in order to obtain the results at circuit level. On the other hand, the circuit level studies, suffer from a lack of information at the device level. In [15], sea-level SER is investigated for three different structures of FinFET (Si, III-V and III-V tunnel FET) technologies considering device and circuit level. In that paper, first, the transient current profile is evaluated using device simulations. Then, according to the critical charge extraction, the electrical and latching window masking effects are studied. The focus of that work was only on the neutron-induced soft error of circuits designed in bulk FinFET technology. They reported SER of a single SRAM cell and there is no information about the contribution of Single Event Upset (SEU) and Multiple Bit Upset (MBU) rates of SRAM arrays. Moreover, the effect of process variation is not considered in their investigation.

Another approach, orthogonal to the simulation-based studies mentioned above, is to perform radiation experiments to obtain SER for FinFET technology. The authors in [18] reported on measured radiation-induced SER of memory and logic devices in a 22nm bulk Tri-gate technology. In [19], the charge collection is investigated for bulk PMOS FinFETs using wafer Two-Photon Absorption (TPA) experiments.

In this work, we perform a comprehensive analysis of radiation-induced soft errors in SOI FinFET technology in order to obtain SEU as well as MBU rates in SRAM-based memory arrays. In order to estimate failure rates, a cross layer approach, which combines simulations at three different levels, is used: 1) 3-D analysis of particle passage through Fin structure, 2) SRAM cell characterization, and 3) 3-D memory array layout analysis. First, the number of electrons generated by the passage of particles through the matter is obtained. Afterwards, using the number of generated electrons, the SER of SRAM cells is estimated using circuit level
simulations considering the location of different transistors in the layout of the memory. We use a hierarchical approach to be able to perform this three-level analysis with a reasonable runtime. The effect of process variation and supply voltage are considered in the SER analysis. Moreover, the contributions of MBU and SEU to the total SER are obtained. Since this work was performed in a collaboration with IBM, the focus of this work is on SOI FinFET technology, however, we plan to extend this analysis for other FinFET topologies in our future work.

Simulation results show that the proton-induced SER is comparable to SER due to alpha-particles, especially at lower supply voltages. Moreover, MBU to SEU ratio is higher for alpha-particle radiation compared to proton radiation. In addition, we show that neglecting the effect of process variation leads to an underestimation of SER.

The paper is organized as follows: In Section 2 the overall flow of this work is presented. The interactions of different particles with device material are described in Section 3. The effect of transient current (generated from interaction of particles and the material) on SRAM cells is described in Section 4. Next, in Section 5, the methodology to obtain the SER is explained considering the placement of the transistors in the circuit layout. Simulation results are presented in Section 6. Finally, Section 7 concludes the paper.

2. OVERALL FLOW

In this section, the flow of SER estimation is described (see Figure 1). When a particle strikes the memory array, it affects some of the transistors inside the memory layout leading to the generation of electron-hole pairs inside those transistors. The generated electron-hole pairs inside the affected transistors lead to parasitic transient current pulses which can eventually flip the state of the SRAM cells. In order to obtain the transient current pulses, two steps have to be performed:

1. A Monte Carlo (MC) simulation of the interaction of the particle and the 3-D material structure needs to be performed to obtain the number of generated electron-hole pairs for different particles energies and the results are stored in look-up tables (LUTs).
2. The number of generated electron-hole pairs has to be converted to a transient current pulse.

All the aforementioned device level steps will be described in Section 3.

The next step is to convert the transient current pulses to the Probability Of Failure (POF) of individual SRAM cells considering process variation. For this purpose, SPICE simulations are performed for different transient current pulse magnitudes to obtain POF for each case and the corresponding data is stored in POF LUTs. The details of these steps are explained in Section 4. An MC 3-D simulation is performed using the transient current and POF LUTs to obtain SEU/MBU rates of SRAM-based memory array. This step is detailed in Section 5.

3. 3-D ANALYSIS OF PARTICLE STRIKE WITH FIN STRUCTURE

3.1 Radiation at ground level

Radiation at ground level causing soft errors comes from different sources. In general, there are two major types of sources:

1) Atmospheric radiations: When a primary cosmic ray (e.g. protons, electrons, photons) enters the atmosphere, it interacts with the molecules of the air leading to the generation of high energy secondary particles (e.g. neutron, hadrons). The neutron is one of the most important ground level radiation sources affecting circuits, leading to the generation of soft errors. Neutrons are not charged and as a result their interactions with materials do not directly create electron-hole pairs. However, their interactions with material lead to the creation of secondary ionizing particles via "indirect ionization" mechanism. The interaction of generated secondary particles and material in turn leads to the generation of electron-hole pairs. Direct ionization from low energy protons is another source of soft errors which has become important for technologies beyond 65 nm [20, 21, 22]. Figure 2(a) shows proton spectrum at ground level [23].

2) Terrestrial radiations: Alpha-particles are the only terrestrial radiations which cause soft errors in current technologies. An alpha-particle consists of two protons and two neutrons (identical to the helium nuclei). $^{235}U$, $^{233}U$, and $^{232}Th$ are the main sources which emit alpha-particles with an energy range of less than 10 MeV (see Figure 2(b)). In this work, it is assumed that the overall alpha particle emission rate is equal to 0.001 $\alpha/h cm^2$ [25].

3.2 Interaction of particles and material

When a particle strikes the device structure, it either directly or indirectly interacts with the atoms in the device structure leading to ionization of the device material. In other words, due to a particle strike, some portion of the particle energy is transmitted to the electrons of struck atoms which eventually leads to the generation of electron-hole pairs along the particle path. For every 3.6 eV of particle energy lost in silicon, an electron-hole pair is generated.

In this work, the Geant4 toolkit [26, 27] is used to simulate the interaction of particles and devices. Geant4 is a platform for Monte-Carlo simulation of the passage of particles through the material. In this work, the target material is the 3-D structure of a single
3. Radiation-induced parasitic transient current pulse

When a particle hits a transistor, some electron-hole pairs are generated. These charges can be transported in the device leading to a parasitic current which in turn can affect the device. In general, the devices containing a reversed p-n junction are sensitive to the particle strikes. This is due to the fact that these types of devices have a strong electric field in the depletion layer of the p-n junction which can lead to a collection of deposited charge as a transient current pulse. The shape of the generated parasitic current is strongly dependent of the technology and can be obtained by 3-D simulations of the device. However, in this work, we consider a simplistic model for the parasitic current which is explained in the following.

Normally the parasitic current is generated due to two different mechanisms:

1) Diffusion: If the particle hits the substrate of the transistor, the generated charges are collected by sensitive nodes due to the diffusion of the carriers. However, in SOI FinFET technology, the diffusion current can be neglected due to the Buried Oxide (BOX) between the substrate and Fin (see Figure 3(a)).

2) Drift: If the particle passes through the sensitive area between source and drain of the transistor (Fin), the generated electron-hole pairs are collected due to the electric field between source and drain (drift mechanism) and create a parasitic current. In order to model this type of current in SOI FinFET technology, different factors have to be considered:

- **Particle passage time** ($\tau_p$): It is defined as the time which takes for the particle to pass through the Fin.

\[
\tau_p = \frac{w_{Fin}}{v_p}
\]

where $v_p$ is the speed of the particle and $w_{Fin}$ is the width of Fin. $\tau_p$ is less than 1 fs (femto second) for alpha particle. For proton, $\tau_p$ is approximately 10 times smaller than that of alpha-particle.

- **Transit time** ($\tau$): It is defined as the average time required for an electron to travel between source and drain.

\[
\tau = \frac{l_{Fin}^2}{\mu_e V_{ds}}
\]

where $l_{Fin}$ is the length of Fin, $\mu_e$ is the electron mobility and $V_{ds}$ is the voltage between drain and source (which is equal to $V_{dd}$ for sensitive transistors). The transit time ($\tau$) for the transistor shown in Figure 3(a) with a supply voltage equal to 1V is more than 10 fs. Since $\tau$ is much larger than $\tau_p$, we can assume that when the particle passes through the Fin, all electron-hole pairs are generated at the same time and start being collected due to the drift mechanism.

- **Recombination time** ($\tau_r$): It determines the rate of the electron-hole recombination. $\tau_r$ ranges from 1ns to 1ms in Si, which is much larger than $\tau$. Therefore, we can assume that the recombination of the electron-hole pairs is negligible at these dimensions and the electron-hole pairs are collected before a major recombination happens.

Considering all aforementioned parameters and their relations, we model the parasitic current as a current pulse (see Figure 3(b)) with a width equal to $\tau$ and an amplitude equal to:

\[
I = \frac{Q}{\tau} = \frac{n_e \cdot e}{\tau}
\]

where $n_e$ is the number of electron-hole pairs generated in the Fin and $e$ is the charge of a single electron.

4. SRAM CELL SOFT ERROR CHARACTERIZATION

In this section, we briefly describe how to obtain the radiation-induced Probability Of Failure (POF) of a single SRAM cell considering process variation. For this purpose, we consider a 6T SRAM cell designed with SOI FinFET technology as shown in Figure 5.

As mentioned in Section 3.3, transistors containing a reversed p-n junction are sensitive to particle strikes. In other words, the sensitive transistors to radiation in an SRAM cell are the ones which are in OFF state with $V_{ds} = V_{dd}$ (transistors shown with red-bold lines in Figure 5(a)). If one or multiple of these sensitive transistors are struck with a particle, parasitic current pulses are generated in these transistors which may eventually lead to a change in the state of the SRAM cell.

POF of an SRAM cell is a function of the current pulse magnitude, the supply voltage and the number of struck transistors. If process variation is neglected, the POF for a given strike scenario
becomes a deterministic binary value in which ‘0’ means the parasitic current pulse does not lead to a flip, and ‘1’ means that the parasitic transient current causes the SRAM cell to flip. For the case in which process variation is considered, POF of the struck SRAM cell for a particular current pulse magnitude becomes a probability value between 0 and 1 ([0, 1]). In this case, to obtain POF, we consider the threshold voltage variation by performing 1000 MC simulations based on accurate SPICE simulations using the current model described in Section 3.3. These POFs are obtained for different supply voltages, current pulse magnitudes, and all possible combinations of current pulses (for I1, I2, I3 and/or any combination of these three currents in Figure 5(a) and then stored in LUTs.

We performed some experiments to find out the effect of transient current pulse shape on POF obtained from SRAM cell characterization. The SPICE simulation results show that POFs have no sensitivity to the current pulse width. In other words, two current pulses with different pulse widths but similar charge (area under the I-t curve) cause the same POF of the SRAM cell. Moreover, we obtained the POF results applying a triangular current shape with different current pulse widths. The results show that although the effect of particular current pulse shape (triangular vs rectangular) is more than the current pulse width, it is still negligible. In other words, the most important parameter for SPICE simulation is the generated charge (the area under the current pulse curve).

5. 3-D MEMORY ARRAY ANALYSIS

In this section, the methodology to estimate the SER for the entire SRAM array is explained. Since a single particle strike can hit multiple Fins (in different cells), we obtain SEU as well as MBU rates by taking the SRAM array layout into consideration. Figure 6 shows the overall flow to obtain the SER of SRAM-based memory array for SOI FinFET technology. The flow to obtain electron-hole pairs/current LUTs is explained in previous sections. In this section we mainly focus on the 3-D MC simulation of the layout (the middle part of the flow shown in Figure 6).

5.1 POF due to a particle strike with a particular energy range

In order to estimate the overall SER due to particle strike, we first need to perform an MC simulation to obtain POF of different cells due to the strike of a particle with a particular energy. The steps of obtaining the POFs of different cells for a simple 2 x 2 SRAM array which is shown in Figure 7 are explained as follows:

1. A random particle with a random direction and position is generated. Based on the angle and the direction of the generated particle, the struck Fins (transistors) can be found by a simple 3-D analysis considering the 3-D layout of SRAM array and the position of Fins/transistors inside the layout.

2. In the next step, the number of generated electron-hole pairs for the affected transistors is obtained from LUTs (using Geant4 as explained in Section 3.2) according to the particle energy.

3. If the affected transistors are the sensitive ones in the SRAM cell (\{m2, m3\} in cell1 and \{m5\} in cell2), the number of electron-hole pairs are converted to the parasitic current pulse as explained in Section 3.2 (see Figure 7).

4. POFs of SRAM cells are obtained according to their parasitic current pulses using SPICE LUTs (obtained using the approach explained in Section 4).

5. The total POF as well as POF of SEU and MBU are computed for SRAM array as a function of cell POFs, as shown below:

\[
P_{\text{tot}} = 1 - \prod_{i} \left(1 - POF_i\right) 
\]

\[
P_{\text{SEU}} = \sum_{i} \left[ POF_i \prod_{j \neq i} (1 - POF_j) \right] 
\]

\[
P_{\text{MBU}} = P_{\text{tot}} - P_{\text{SEU}} 
\]

6. Steps 1-5 are performed iteratively for particles with the same energy range and different random directions and positions. For a particle with a particular energy range, the overall POFs.
(POF_{tot}, POF_{SEU}, and POF_{MBU}) of SRAM array are obtained by the averaging over all iterations.

5.2 Failure In Time (FIT) rate calculation

After obtaining the POF of different particles with different energy ranges, the next step is to obtain the Failure In Time (FIT) rate of the memory array. In order to obtain FIT rate, the following equation is used:

$$\text{SER}(\text{FIT}) = \int POF(E) \cdot \text{Flux}(E) \cdot Lx \cdot Ly \cdot dE$$  \hspace{1cm} (7)

In this equation, POF is the probability of failure of the particle at a particular energy, E, which is obtained as explained in Section 5.1. Flux is the flux of the particle which can be obtained according to Figure 2. Lx and Ly are the dimensions of the memory array. Since it is not possible to obtain POF over all energy ranges, we need to discretize the energy spectrum of the particle to different ranges. Therefore, Equation 7 can be rewritten as follows:

$$\text{SER}(\text{FIT}) = \sum POF(E) \cdot \text{IntFlux}(E) \cdot Lx \cdot Ly$$  \hspace{1cm} (8)

where E is the representative energy of each range and IntFlux(E) is the integral flux of the particle at that range.

6. SIMULATION RESULTS

In this section, the simulation results are presented. The geant4 toolkit is used in this work to build electron-hole pairs LUTs. A 14 nm SOI FinFET technology library [29] is used for SPICE simulations. After obtaining the number of electron-hole pairs and POFLUTs, a 3-D MC simulation (10 Million iterations) is performed as described in Section 5 to estimate SEU and MBU rates for a 9×9 SRAM array with a layout which is shown in Figure 5(b). The device parameters are obtained from [28]. It should be noted that the runtime of the entire process for a 9×9 memory array for 10 Million MC simulations is around 2 hours. Such an array size is large enough to obtain a realistic ratio for MBU vs. SEU and there is no need to explicitly consider larger arrays. The simulation results are presented in the following. All presented results in this section are normalized.

POF of different particles at different energy ranges.

Figure 8 shows the total POF of the SRAM-based memory array with $V_{dd} = 0.7V$ and $V_{dd} = 0.8V$ due to alpha-particle and proton strike. For this experiment, we assume that the particle definitely hits the layout of the memory array under investigation. As shown in this figure, the POF due to alpha-particle is much larger than that of proton, as more electron-hole pairs are generated by alpha-particles (see Figure 4). Moreover, POF decreases for both particles for higher particle energies, since, according to Figure 4, for higher particle energies less electron-hole pairs are generated. In addition, the POF increases with decreasing $V_{dd}$ for both particle types. This is due to the fact that SRAM cells are more sensitive to the soft error at lower supply voltages. In other words, some particles which have no effect on SRAM cells with higher supply voltages, may flip the SRAM cell value at lower supply voltages.

Overall FIT rate of memory array.

Figure 9 shows the total SER due to proton and alpha-particle strike for various supply voltage values. As shown in this figure, the overall SER increases by decreasing the supply voltage. Moreover, the results show that the SER due to proton radiation is comparable to that of alpha-particle for $V_{dd} = 0.7$. Although the POF due to proton strike is much smaller than that for alpha particle, the overall SERs of proton and alpha particles are comparable at lower supply voltages ($V_{dd} = 0.7$) due to the higher flux of protons at ground level. The proton-induced SER decreases with an extremely higher rate for larger supply voltages compared to alpha-particle-induced SER. This implies that proton-induced soft error is important especially for low power applications (lower $V_{dd}$).

SEU vs. MBU.

Figure 10 shows the MBU to SEU ratio for alpha and proton particles. As shown in this figure, MBU/SEU ratio of protons (less than 2%) is much smaller than that of alpha-particles (6-7%). This is due to the fact that SEU rate is proportional to $POF^1$ while MBU is proportional to $POF^n$ ($n > 1$). As a result, since the proton-induced POF of SRAM cells is much smaller than that induced by alpha-particles, the difference between MBU rate of alpha particle and protons is much larger than the difference between SEU rates of these particles. Moreover, alpha-induced MBU/SEU ratio has
almost the same value for different supply voltages while this ratio decreases with increasing $V_{dd}$ for protons. This is rooted in the fact that POF is less sensitive to $V_{dd}$ for alpha particles (according to Figure 8) especially in the range of energies which is important at sea level (less than 10Mev). However, the sensitivity to $V_{dd}$ is much higher for protons. The other reason is that the mass of alpha particles is four times bigger than that of protons, therefore, at the same speed the kinetic energy of alpha particles is four times bigger than that of protons.

Effect of process variation.

Figure 11 shows the total SER due to alpha-particle strike for two cases:

1. Neglecting process variation: For this case, SPICE simulations are run for the nominal case. The outputs of the simulations for different current pulses (i.e. each simulation case) are binary values: ‘1’ (for the BIT flip) and ‘0’ (no flip). The overall POFs are obtained by averaging over all these binary values for 10 million iterations.

2. Considering process variation: In this case, as explained in the flow, the process variation is considered in SPICE simulations and probabilistic POF values (between 0.0 and 1.0) are reported for different parasitic currents (i.e. each simulation case).

As shown in this figure, neglecting the effect of process variation leads to an underestimation of SER (up to 45%). The simulation results also show the same trend for proton-induced SER.

7. CONCLUSIONS AND FUTURE WORK

In this paper, the SER of SRAM-based memory in SOI FinFET technology is investigated using a cross layer approach. In our approach we used information from device level (interaction of particles and materials), circuit-level cell characterization, and array-level 3D simulations. This study can be summarized as:

1. SER is higher for lower supply voltages.
2. SER due to proton strike is comparable to that for alpha-particle strike at very low supply voltages (low power applications).
3. MBU/SEU ratio is relatively higher for alpha radiation compared to that for protons.
4. Neglecting the effect of process variation leads to an underestimation of SER.

It should be noted that in this work, we only considered the SER due to proton and alpha-particle radiations which cause direct ionization in material. The study of neutron radiation SER, which causes indirect ionization of materials, is our future work.

8. REFERENCES