A Direct-Conversion Mixer with a DC-offset Cancellation for WLAN

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Abstract—This paper presents a 5GHz double-balanced mixer with DC-offset cancellation circuit for direct-conversion receiver compliant with IEEE 802.11a wireless LAN standard. The analog feedback loop is used to eliminate the DC-offset at the output of the double-balanced mixer. The test results show that the mixer with DC-offset cancellation circuit has voltage conversion gain of 9.5dB at 5.15GHz, noise figure of 13.5dB, IIP3 of 7.6 dBm, 1.73mV DC-offset voltage and 67mW power with 3.3 V power supply. The DC-offset cancellation circuit has less than 0.1mm² additional area and 0.3mW added power dissipation. The direct conversion WLAN receiver has been implemented in a 0.35um SiGe BiCMOS technology.

I. INTRODUCTION

Wireless communications remain an important area of research and development, fueled by the emerging of wireless local area networks (WLAN) and the third generation W-CDMA technology[1]-[8]. In order to get more features and less cost at RF front sections, the choice of a suitable receiver implementation requires a careful study of the system specifications. Superheterodyne architecture is a traditional receiver patented in 1917 by Edwin Armstrong [9], which offers the best performance in most wireless system applications. Nevertheless, the architecture requires passive filter components mostly because of the intermediate-frequency (IF) and image-reject, which have to be high quality factors and often employ surface acoustic wave (SAW) filter at off-chip [2].

Direct-conversion receivers shown in Fig.1 have attracted a great deal of attention over the past a few years. In actual direct conversion systems, the LO frequency is in the middle of the RF spectrum under consideration. The higher frequency components at the output can be easily removed by active or passive low-pass filter at the baseband. By eliminating IF stages and the image-reject requirement of the front-end filters, direct-conversion architecture can significantly improve on-chip integration of the receiver. However, this architecture creates additional performance criteria such as DC-offsets, second order intermodulations (IM2), in-band local oscillator (LO) radiation and flicker noise that are not presented in a heterodyne counterpart.

As shown in Fig.1, LO leakage exists from the LO port to the LNA input, mixer input, the antenna and a finite amount of feedthrough because of substrate coupling and bond wire coupling [3]. One of the most challenges of these performance criteria is the effective cancellation of DC-offsets. This paper describes a solution of DC-offset cancellation in a 5GHz direct-conversion receiver.

In direct-conversion receiver, the down-converted spectrum is centered at 0Hz if information contains DC-offset, the SNR will be degraded. In fact, the offset may be larger than the signal and much larger than thermal or flicker noise. A down-converted signal may have an amplitude of a few hundred microvolts while the DC-offset may be in the range of millivolts, which will degrade the following stages [5].

There are two common DC-offset cancellation solutions: (1) AC coupling (high pass filter) [6]. (2) Digital cancellation with DAC sampling [7]. By the means of AC coupling, a very low corner frequency of the high pass filter is required, indicating large capacitors, which is not suitable for integration. Digital solution including DAC will complicate the design and increase the power dissipation.

The work of this paper focuses on mixer compliant with IEEE 802.11a wireless LAN standard, which eliminates DC-offset in the mixer output by analog feedback loops mentioned firstly by P. Lafferriere[5], whose design has a little lack for not being completely implemented. Section II presents mixer and DC-offset cancellation circuit topology. Section III shows the experimental results. Section IV summarized the work.

II. CIRCUIT TOPOLOGY

A. Topology preview

A full direct-conversion receiver topology is illustrated in Fig.1. In this solution, the mixer is the primary block, and the DC-offset circuit occurs in the baseband section following the mixer.
B. Mixer design

The circuit schematic of the mixer is shown in Fig. 2, which is a typical Gilbert cell with single-ended input and differential output. Inductor $L_e$ is used as emitter degeneration to increase the linearity of the mixer while consuming little voltage headroom. As mentioned in [8], when LO is ideal square wave, mixer's voltage gain

$$A_v = \frac{2}{\pi} \frac{R_c}{r_e + j\omega L_e}$$

where $R_c$ is the load resistance and $r_e$ is the emitter resistance of $Q_5$ or $Q_6$. Since mixer's IIP3 is proportional to $\omega G_{m_e} L_e$, $L_e$ should be carefully chosen to compromise between the gain and IIP3. Noise matching is achieved by sizing $I_e$, selecting transistors size and operating the RF transistors at the current density required for minimum noise figure. Combining with the matching network, $I_e$ also achieves simultaneous noise and power matching [8].

Since the current in the quad switching transistors is decided by RF transistors below, the current density for peak $f_T$ is achieved by sizing the transistors. In this design, they are 1/6 of the RF transistors. LO signals are applied to the base of the quad transistors through buffers, so that their amplitude can be kept large enough for completely switching. $L_f$ and $C_f$ are tuned on the LO+RF frequency to get rid of the unwanted sideband. The LC tank tuned on the second RF harmonic, acts as an ac current source in the emitter of the input transistor pair [7].

C. DC-offset cancellation circuit

According to [10], in which the analysis of the DC component has been presented. The DC term in IF of mixer depends on the collector resistor mismatch, the value of tail current and the amplitude modulation component.

To eliminate the DC-offset voltages, The feedback networks including common mode (CM) and differential mode (DM) feedback loops have been used. Parallelled with the resistor loads $R_{zf}$, a pair of PFETs are employed to shunt the output current of the mixer under the control of feedback loop, as shown in Fig. 2. The output voltage is adjusted by the shunted current, which must have enough tolerance to severely restricted DC-offset voltage. This current is set at about 20% of total mixer’s collector current in this design.
In the common-mode feedback loop, the common-mode output voltage is compared with a reference voltage. The comparison voltage controls the gate of the PFETs in order to stabilize the common-mode voltage at the mixer output. The mixer load DC point is be stabilized by the way, to reduce the DC-offset voltage. The schematic topology is shown in Fig.3.

In the Gilbert-cell based mixer, differential-mode DC-offset is predominant at the output. The DM feedback loop is restricted, not only by the baseband signal spectral, but also the noise contributing to the whole receiver. Therefore, the DM DC-offset correction loop amplifier must fulfill 3 requirements:

- The loop must have sufficient gain at DC to provide adequate DC-offset reduction.
- The equivalent output noise of the circuit must be low enough to avoid degrading the mixer noise figure remarkably.
- The loop must have gain low enough near the lower corner frequency of the sub channel (at frequencies above 150kHz in this case) where the desired signal is not attenuated significantly.

Following these requests, the differential-mode loop is a low pass filter with high gain and low cut off frequency. The schematic of the loop is shown in Fig.4.

The first stage illustrated in Fig.4 utilizes bipolar transistors in the feedback amplifier, which have higher gain and lower noise than MOSFETs. However, in the second stage, a pair of MOSFETs is placed, which generates a Miller Multiplication with high input impedance. The two stages loop amplifiers are loaded by PMOS current sources. The total impedance seen at the output is equal to \( r_{o1}/(r_{o2}+r_{o3}) \), and the gain is given by:

\[
Gain = -g_m (r_{o3} // r_{o2}) \tag{2}
\]

The gain of first stage is 40.3dB at 0Hz, the phase margin is equal to 130\(^\circ\). Without the Miller capacitor, bandwidth of the amplifier is about 7MHz, and the second stage gain is 45dB.

The second stage gain is similar to the first stage, which allows the Miller effect to generate an effective capacitance at the inter-stage of amplifier. The Miller effective capacitance is mostly equal to the product of the compensation capacitance and the second stage gain.

\[
C_{Miller} = Gain \times C \tag{3}
\]

The configuration is a Miller Integrator with 2pF capacitor which is small enough to be integrated on chip, and the actual effective input capacitance is about 1nF. It is hard to fabricate a capacitor of 1nF since the capacitor is an area-consuming component. The curve illustrated in Fig.4 shows the AC response of the differential feedback-loop, which is close to the ideal model of former requests. With the Miller capacitor, the feedback loop has gain low enough at 150 kHz, which offers corner frequency enough low for 802.11a standard. In Fig.3, the \( R_1 \) and \( R_2 \) are a couple pair with emitter degeneration to adjust the gain.

### III. EXPERIMENTAL RESULTS

![Figure 5 Measured Frequency Response of the DM feedback-loop](image)

![Figure 7 Measured Input 1dB Compression Point](image)

![Figure 8 Measured Conversion Voltage Gain](image)

Fig.6 gives the mixer output spectrum at input RF frequency 5.15GHz and LO frequency 5.2GHz. Fig.7 shows the 1dB compression point with the same RF and LO frequency above and with the load 50\(\Omega\). The figure shows
the 1dB compression point is -2dBm, which is slightly less than the simulated result (-1.5dBm). In fact, the next stage has an input resistance larger than 50Ω, together with the non-perfect input matching, which will result in the 1dB compression point lower than test result. Fig. 8 shows the conversion voltage gain versus the input signal frequency. The measured result, already computed with a large read resistance, is smaller than simulation, which might be the influence of the input matching and parasitical components of the circuit. The measured frequency response of DC-offset cancellation the feedback loop is close to the simulation result, which is illustrated in Fig 5. The DC-offset voltage is less than 2 mV at mixer IF output after a pair of capacitors.

![DC-offset cancellation](image)

**Figure 9** Die photograph of the chip

**IV. CONCLUSION**

A 5GHz direct-conversion mixer with DC-offset cancellation circuit is presented in this paper. It was implemented in 0.35μm SiGe BiCMOS technology. A die photograph of the chip is shown in Fig. 6, which has an area of 0.65mm×0.53mm. It draws 21.3mA current with 3.3-V supply and provides a conversion voltage gain about 9.5dB, noise figure 13.5dB, and IIP3 70dBm. The DC-offset cancellation circuit has less than 0.1mm² additional area and 0.3mW added power dissipation. The circuit of this solution is easy for realization, and has little influence on the performance of the receiver.

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**REFERENCES**


