A Nonrecursive Digital Calibration Technique for Joint Elimination of Transmitter and Receiver I/Q Imbalances With Minimized Add-On Hardware

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Abstract—A nonrecursive digital calibration technique, namely, local oscillator (LO) switching, is proposed for jointly eliminating transmitter (TX) and receiver (RX) I/Q imbalances in one combined process. The add-on analog parts are limited to a set of source followers (0.00228 mm$^2$) and metal–oxide–semiconductor (MOS) switches (0.00017 mm$^2$) for reusing the 90° phase shift property of the reference LO, avoiding the sinusoidal test tone, loop-back detector, high-speed analog-to-digital converter, and 2-D iterative search algorithm, mostly required in the prior art. A 65-nm complementary MOS transceiver, which is codesigned with a field-programmable-gate-array-based coordinate rotation digital computer algorithm, measures a 10-dB improvement in the image rejection ratio of both the TX (27.8 → 37.2 dB) and the RX (31.2 → 42 dB). The required digital circuitry for the algorithm is also assessed and simulated.

Index Terms—Algorithm, calibration, coordinate rotation digital computer (CORDIC), I/Q imbalance, local oscillator (LO), receiver (RX), transceiver, transmitter (TX).

I. INTRODUCTION

QUADRATURE modulation is fundamental in nearly all wireless transceivers for its high spectral efficiency; however, mismatches of components and the physical layout can always lead to gain and phase mismatches between the I and Q signals [1], [2]. The resultant image effect can significantly degrade the error vector magnitude (EVM), particularly for very dense signal constellations, such as 16-quadrature amplitude modulation (QAM) and 64-QAM [3]. Since I/Q imbalances can happen in the receiver (RX), the transmitter (TX), and the local oscillator (LO), the desired calibration algorithm should be able to correct them with minimum add-on hardware for better cost and area efficiencies.

A number of techniques have been reported to deal with the I/Q-imbalance problem. Examples are the loop-back detector with a recursive algorithm [4], [5], a 2-D iterative search algorithm [6], [7], and a blind estimation algorithm [8], [9]. The first two are still demanding in hardware and computation, inducing a long calibration time and would be power and area hungry in its implementation. For the third, although no training sequence is entailed, the estimation process still involves heavy computation (e.g., inverse matrix) and can suffer from the instability issue in the recursive loop. This brief introduces a nonrecursive digital calibration technique for joint correction of RX and TX I/Q imbalances under a reference LO. The technique is named LO switching. The add-on analog parts are limited to a set of source followers and metal–oxide–semiconductor (MOS) switches. The latter is to employ the 90° phase shift property of the LO available in most quadrature transceivers, generating adequate conditions to estimate the I/Q-imbalance parameters nonrecursively. The experimental verification is based on a 65-nm complementary MOS (CMOS) transceiver chip codesigned with a coordinate rotation digital computer (CORDIC) algorithm [10] implemented in the field-programmable gate array (FPGA).

Section II overviews the system codesign, including the transceiver chip and the calibration algorithm implemented in the FPGA. Section III describes the principle of the algorithm, highlighting its joint estimation capability for both TX and RX I/Q imbalances in a combined process. The measurement results are given in Section IV. Section V concludes this brief.

II. TRANSCEIVER–FPGA SYSTEM CODESIGN

A. Transceiver Chip (Fig. 1, Right)

Fig. 1 shows the block schematic of the system. In the calibration mode, the RF output from the TX mixers is looped back to the RX via the TX–RX switch, such that the calibration process can be moved to the digital domain, reusing the existing hardware while, more importantly, linking up together the I/Q imbalances of both the RX and the TX for joint calibration. The integrated TX consists of two first-order passive-RC low-pass filters (LPFs) for reconstructing the I and Q inputs generated by the off-chip digital-to-analog converters (DACs). After I/Q
(1.27–1.94 GHz), such that the worst RC variations can still be tolerated.

At the circuit level, before driving the four-phase LO to the I/Q passive mixers, logic operation is applied to transform them from sine-LO into a set of 25% duty cycle square-LO with guard intervals, avoiding I/Q crosstalk, while saturating the LO amplitude to improve gain balancing. The circuit details are omitted here due to the space limit.

B. FPGA (Fig. 1, Left)

For the TX digital baseband, the imbalanced baseband output can be modeled as \( x_{tx,imb}(t) = I_{tx,imb} + jQ_{tx,imb} \), such that

\[
\begin{bmatrix}
I_{tx,imb} \\
Q_{tx,imb}
\end{bmatrix} = \begin{bmatrix}
1 & \alpha \\
0 & \cos \theta
\end{bmatrix} \begin{bmatrix}
I_{tx} \\
Q_{tx}
\end{bmatrix}
\]

where the gain and phase imbalances are represented by \( \alpha \) and \( \theta \), respectively. Similarly, for the RX, the imbalanced baseband output is given by

\[
\begin{bmatrix}
I_{rx,imb} \\
Q_{rx,imb}
\end{bmatrix} = \begin{bmatrix}
\beta & 0 \\
\sin \xi & \cos \xi
\end{bmatrix} \begin{bmatrix}
I_{rx,ideal} \\
Q_{rx,ideal}
\end{bmatrix}
\]

where the gain and phase imbalances are represented by \( \beta \) and \( \xi \), respectively. \( I_{rx,ideal} \) and \( Q_{rx,ideal} \) refer to the downconverted output with an ideal RF input with no I/Q imbalance. Such an RF model is used as the basis for the following estimation process. With a reference LO mixed with the digital baseband signals, we obtain the RF signal as

\[
s_{RF} = (I_{tx} + \alpha \sin \theta Q_{tx}) \cos \omega t + \alpha \cos \theta Q_{tx} \sin \omega t.
\]

The precompensation of the TX and the postcompensation of the RX are operated by directly inversing the baseband system model between the TX and the RX, in which both matrices can be represented as

\[
\begin{bmatrix}
I_{tx,pre} \\
Q_{tx,pre}
\end{bmatrix} = \begin{bmatrix}
1 & -\tan \theta \\
0 & \sec \theta / \alpha
\end{bmatrix} \begin{bmatrix}
I_{tx} \\
Q_{tx}
\end{bmatrix}
\]

Compensation for TX

\[
\begin{bmatrix}
I_{rx,post} \\
Q_{rx,post}
\end{bmatrix} = \begin{bmatrix}
1 & 0 \\
-\tan \xi & \sec \xi / \beta
\end{bmatrix} \begin{bmatrix}
I_{rx} \\
Q_{rx}
\end{bmatrix}
\]

Compensation for RX

III. PROPOSED LO SWITCHING I/Q-IMBALANCE CALIBRATION

The I/Q imbalance model is shown in Fig. 3(a). The overall gains of the TX and the RX are denoted by \( A \) and \( B \), respectively, and the overall phase shift passing through them is denoted by \( \varphi \). The outputs for the TX baseband are \( I_{tx} \) and \( Q_{tx} \), and the inputs for the RX baseband are \( I_{rx} \) and \( Q_{rx} \). As shown in Fig. 3(a), if a dc training signal is sent from \( I_{tx} \) and \( Q_{tx} \) separately into the system, only four equations are available to estimate the wanted I/Q-imbalance parameters. Consequently, only the conventional least mean squares method can be applied, which is slow [11], [12] and has limited accuracy [12]. The LO switching technique presented here has the objective of
finding more independent equations. The procedure is twofold: 1) transmit a dc training signal from \( I_\text{tx} \) and \( Q_\text{tx} \) to the system; and 2) switch the LO such that an extra 90° phase shift can be set between the two input channels, offering more equations to solve the desired I/Q-imbalance parameters. Specifically, if a dc training signal with amplitude \( c \) at \( I_\text{tx} \) and \( Q_\text{tx} \) is separately injected into the I/Q imbalance model, the output signals can be represented as:

\[
\text{The output signal through Path 1}
\]

\[
I_{\text{rx, Path1}} = \text{LPF}\{cA \cos(\omega t)B \cos(\omega t + \phi)\} = \frac{cAB}{2} \cos \phi.
\] (6)

\[
\text{The output signal through Path 2}
\]

\[
Q_{\text{rx, Path2}} = \text{LPF}\{cA \cos(\omega t)\beta B \sin(\omega t + \phi + \xi)\} = \frac{c\beta AB}{2} \sin(\phi + \xi).
\] (7)

\[
\text{The output signal through Path 3}
\]

\[
I_{\text{rx, Path3}} = \text{LPF}\{c\alpha A \sin(\omega t + \phi)B \cos(\omega t + \phi)\} = \frac{c\alpha AB}{2} \sin(\theta - \phi).
\] (8)

Then, considering Fig. 3(b), the phase of the LO is switched for a phase shift of 90°. In this case, if we transmit a dc training signal at \( I_\text{tx} \) and \( Q_\text{tx} \), the output signals can be represented as:

\[
\text{The output signal through Path 4}
\]

\[
I_{\text{rx, Path4}} = \text{LPF}\{cA \sin(\omega t + \phi)B \cos(\omega t + \phi)\} = -\frac{cAB}{2} \sin \phi.
\] (9)

\[
\text{The output signal through Path 5}
\]

\[
Q_{\text{rx, Path5}} = \text{LPF}\{cA \sin(\omega t)\beta B \sin(\omega t + \phi + \xi)\} = \frac{c\beta AB}{2} \cos(\phi + \xi).
\] (10)

\[
\text{The output signal through Path 6}
\]

\[
I_{\text{rx, Path6}} = \text{LPF}\{c\alpha A \cos(\omega t + \theta)B \cos(\omega t + \phi)\} = \frac{c\alpha AB}{2} \cos(\theta - \phi).
\] (11)

Thus, the overall gain \( G = AB/2 \) and the overall phase shift \( \phi \) can be computed as:

\[
G = \sqrt{(I_{\text{rx, Path1}}/c)^2 + (I_{\text{rx, Path4}}/c)^2}
\] (12)

\[
\phi = \tan^{-1}(I_{\text{rx, Path4}}/I_{\text{rx, Path1}}).
\] (13)

Finally, the gain and phase mismatches of the TX and the RX are solved, leading to:

\[
\alpha = G^{-1} \sqrt{(I_{\text{rx, Path6}}/c)^2 + (I_{\text{rx, Path3}}/c)^2}
\] (14)

\[
\theta = \tan^{-1}(I_{\text{rx, Path3}}/I_{\text{rx, Path6}}) + \phi
\] (15)

\[
\beta = G^{-1} \sqrt{(Q_{\text{rx, Path2}}/c)^2 + (Q_{\text{rx, Path5}}/c)^2}
\] (16)

\[
\xi = \tan^{-1}(Q_{\text{rx, Path2}}/Q_{\text{rx, Path5}}) - \phi.
\] (17)

The feasibility of the above algorithm can be limited by 1) the numerical estimation accuracy and 2) the LO’s gain and phase errors. For the former, Verilog simulations show a maximum gain error of \( 8 \times 10^{-4} \) and a phase error of \( \pm 0.1° \) in number estimation under 10^5 time runs, which correspond to an IRR of 65 dB. Thus, the former should not be the limiting factor for most transceivers.

For the latter, we can consider a nonideal LO as \( \text{LO} = \gamma e^{i\omega t + \eta} \), where \( \gamma (\eta) \) denotes the LO gain (phase) error. The achievable IRR in the TX with respect to that of the LO is plotted in Fig. 4. They are linearly related. Thus, for an IRR of 60 dB in the LO (see Fig. 2), the IRR of the TX and the RX should only be limited by themselves.

**IV. Measurement Results**

A. Transceiver Chip and Test Setup

The transceiver was fabricated in a 65-nm CMOS process, and the chip micrograph is shown in Fig. 5. The active die area is 0.82 × 0.5 mm², of which only 0.00245 mm² is due to the LO switches and source followers added to assist the calibration. The experimental setup is shown in Fig. 6. The baseband I/Q signals are generated by the ALTERA DE4 FPGA. It interfaces with the RX and the TX through the Texas Instrument DACs (5662) and ADCs (ADS62P23). Both...
Fig. 5. Chip micrograph of the fabricated 65-nm CMOS transceiver. The only add-on analog parts for calibration are the LO switches and source followers.

Fig. 6. Experimental setup.

have a 12-bit resolution and an 80-MHz conversion rate. The master clock is generated by the FPGA for synchronization. All RF and LO switches are driven by the FPGA through digital level shifters downscaling the control signal from 3.3 to 1.2 V, befitting the employed 65-nm CMOS devices. The output signal from the DA is measured by the R&S FSU-8 spectrum analyzer for the single-tone test. The digital outputs from the FPGA are captured by the Agilent 16902B logic analyzer for the RX postcompensation test.

B. Algorithm Implemented in the FPGA and Simulated in ASIC

Fig. 7 shows the time diagram of the data picking process. The preread phase learns the dc offsets. A dc signal with amplitude \(c\) (~0.2 V, to uphold the linearity) is then transmitted at \(I_{tx}\), to obtain \(I_{rx}\) and \(Q_{rx}\). Afterward, transmit data are exchanged, i.e., \(I_{rx} = 0\) and \(Q_{tx} = c\) to obtain \(I_{rx}\), where \(Q_{rx}\) is ignored. The process is repeated once after creating the 90° phase shift via LO switching. After data collection, the I/Q-imbalance parameters are computed in the FPGA with (12)–(17) in Section III. The computation employs a CORDIC algorithm, in which only shift bits and adders are required in the entire computation, rendering it very power and area efficient. For example, after picking \(I_{rx, Path1}\) and \(I_{rx, Path4}\), (12) and (13) can be solved by the CORDIC after 25 clock cycles under a 100-MHz clock rate. Since there are three sets of equations, 75 clock cycles are entailed totally. There is one more clock cycle for the computation of the parameters in (4) and (5).

The algorithm is also converted into a 65-nm CMOS application-specific integrated circuit (ASIC) under the Cadence Encounter, the required power, area, and calibration time are estimated, as summarized in Table I. The simulated digital power during compensation is 366.55 \(\mu\)W, and the entire calibration process takes 760 ns and consumes 206 pJ of energy to complete at a 100-MHz clock rate. The entailed digital area is \(\sim 0.02\) mm².

C. IRR Before and After Calibration

Fig. 8(a) and (b) shows the TX output spectra for a single-tone test before and after calibration, respectively. The IRR is improved from 27.8 to 37.5 dB. The calculated I/Q-imbalance parameters are shown in Table II. The results of the RX before
TABLE II
CALCULATED I/Q IMBALANCE PARAMETERS

<table>
<thead>
<tr>
<th>G</th>
<th>ϕ</th>
<th>α</th>
<th>θ</th>
<th>β</th>
<th>ξ</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3055</td>
<td>44.7003°</td>
<td>1.0281</td>
<td>-3.2828°</td>
<td>1.0823</td>
<td>1.9306°</td>
</tr>
</tbody>
</table>

Fig. 9. RX output (a) before and (b) after calibration.

TABLE III
CHIP SUMMARY

<table>
<thead>
<tr>
<th>Technology</th>
<th>65 nm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver Chip Area</td>
<td>0.41 mm²</td>
</tr>
<tr>
<td>Analog Area for Calibration</td>
<td>0.00245 mm²</td>
</tr>
<tr>
<td>Operation Frequency</td>
<td>1.4 GHz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td></td>
</tr>
<tr>
<td>RX Path</td>
<td>18 mW</td>
</tr>
<tr>
<td>LO Generator</td>
<td>22 mW</td>
</tr>
<tr>
<td>DA</td>
<td>20 mW</td>
</tr>
<tr>
<td>TX IRR Before and after Calibration</td>
<td>27.8 dB → 37.2 dB</td>
</tr>
<tr>
<td>RX IRR Before and after Calibration</td>
<td>31.2 dB → 42 dB</td>
</tr>
</tbody>
</table>

TABLE IV
COMPARISON WITH THE STATE OF THE ART

<table>
<thead>
<tr>
<th>2-D Search</th>
<th>Sine Test Tone</th>
<th>Dedicated Detector</th>
<th>High-Speed ADC</th>
<th>TX IRR Improved</th>
<th>RX IRR Improved</th>
</tr>
</thead>
<tbody>
<tr>
<td>This Work ¹</td>
<td></td>
<td></td>
<td></td>
<td>10 dB</td>
<td>10 dB</td>
</tr>
<tr>
<td>[4] ²</td>
<td>v</td>
<td>v</td>
<td>v</td>
<td>12 dB</td>
<td>12 dB</td>
</tr>
<tr>
<td>[6]</td>
<td>v</td>
<td>v</td>
<td>v</td>
<td>15.6 dB</td>
<td>No</td>
</tr>
<tr>
<td>[7]</td>
<td>v</td>
<td>v</td>
<td>v</td>
<td>24 dB</td>
<td>No</td>
</tr>
</tbody>
</table>

¹ Reuse of RX mixers, LPFs and ADCs. The only add-on hardware is a set of source followers and MOS switches.
² Result is extracted from the gain and phase mismatches.

V. Conclusion

A nonrecursive digital calibration technique for joint elimination of TX–RX I/Q imbalances has been described. The only add-on analog hardware is a set of source followers and MOS switches for generating an extra 90° phase shift in the reference LO, which is shared among the TX and the RX. The I/Q accuracy of the LO is optimized at the circuit level via employing a three-stage RC–CR network to achieve adequate I/Q accuracy over process variations. This work avoids the sinusoidal test tone, loop-back detector, high-speed ADC, and 2-D recursive search algorithm that were commonly required in the prior art. A 65-nm CMOS transceiver prototype codesigned with an FPGA-implemented algorithm shows a 10-dB improvement in the IRR of both the TX and the RX in one combined process.

References