A LOW COMPLEXITY UWB CIRCUIT TRANSCEIVER ARCHITECTURE FOR LOW COST SENSOR TAG SYSTEMS

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Abstract - This paper presents the architecture of a low power, low complexity Ultra Wideband (UWB) transceiver circuit. The circuit is designed for low data rate, low cost applications with built in location and tracking capabilities. The system is based on a non-coherent architecture which enables the receiver to be extremely simple and largely insensitive to the transmitted pulse shape. The circuit presented contains the oscillator, the transmitter, the receiver and baseband digital signal processing (DSP) block. The oscillator contains the quartz oscillator, a delay locked-loop (DLL) and edge combiner for clock multiplication to generate a 528 MHz timing signal for pulse generation. The transmitter contains a second DLL to fix the delay of the UWB pulse, the UWB pulse generator and antenna. The transmitted UWB pulse is presented. The receiver contains low noise amplifier, variable gain amplifier, squaring circuits, integrators for energy collection, 4 bit analogue-to-digital converters (ADC), digital control logic, integrator and gain selection logic block and detection/bit decision block. The circuits are designed in a 0.35 μm Si-Ge BiCMOS process from Austria Microsystems.

Keywords - UWB transceiver, UWB pulse generator, DLL based clock synthesis.

I. INTRODUCTION

Ultra wideband (UWB) is a very promising technology for future short-range indoor data communications applications [1]. The Federal Communications Commission (FCC) defines a radio system to be an UWB system if the fractional bandwidth $B_B$ or the -10 dB bandwidth of the signal is greater than 20% or greater than 500 MHz, respectively [2]. The UWB concept can be based on time-hopping (TH), direct-sequence (DS) spread spectrum approaches, fast frequency sweeping, or multi-carrier techniques. The data modulation schemes most often used in UWB systems are pulse position modulation (PPM) and pulse amplitude modulation (PAM).

The system concept is to have an indoor network with data rates of the order of 1 kbps - 100 kbps, an unlimited number of TAGs, a low power, low-cost, low-complexity UWB transceiver. The system concept utilize individual identification of each unit, 1 measurement/second per unit, centralized control and positioning calculation in base stations, operation in unlicensed bands and two way data transfer sufficient to allow position information to be relayed. Also, device mobility is supposed to be slow (less than 40 km/h) and they have the possibility to join/leave the measurement area at arbitrary times. The stated intention is to be able to track devices in a specified measurement area for later processing or online monitoring purposes.

The bandwidth of the UWB signal means that the number of the distinguished multipath components is very large [3]. This characteristic can give a gain both in terms of diversity and accuracy. In order to be able to exploit both advantages a higher implementation complexity is needed. In order to gain diversity it means to implement a RAKE receiver with a larger number of fingers and to implement an algorithm to search the strongest path. On the other hand to exploit the accuracy a high frequency clock able to sample inside a sub-nanosecond time window is needed. Using such a high frequency clock, on the order of gigahertz, is not appropriate for implementing a low-power UWB TAG transceiver.

The low complexity, low cost and low power UWB transceiver design targets combined with channel characteristics gives the idea to simplify the transceiver as much as possible and let all the computation capability to the base station. To achieve a reasonable BER for reasonable SNR we must design a robust receiver inside UWB TAG. The simplest choice to be designed is the energy collection approach which is able to recover the energy coming from the rich multipath channel. This non-coherent approach avoids requiring the implementation of channel estimation with the drawback of noise and interference enhancement. Because the modulation has no correlation in the receiver it needs to be orthogonal in the time domain.

The duty cycle ratio of UWB TAG is 1% because it is transmitting/receiving 5000 bits to/from UWB base station 1000 us every 1 second. The above characteristic combined with low frequency reference oscillator make the low power implementation of UWB TAG feasible.

The low-complexity of UWB TAG is given by the fact that DLL frequency synthesis approach is used [4] and at the receiver an architecture based on simple power integration circuit is employed. An UWB transceiver prototype which makes use of an architecture based on sample/hold and A/D converters was presented in [5]. The analogue-to-digital...
conversion resolution used is 1 bit. An “all-digital” UWB receiver is presented in [6] where it is shown that the sufficient ADC resolution needed for reliable detection of a UWB signal is 4 bits. A UWB transceiver architecture and its typical performance parameters which is not based on impulse radio but on multiple bands are presented in [7]. The ADC resolution used in [7] is 6 bits. An time-modulated UWB receiver block diagram is presented in [8] where the ASIC implementation requirements of an integrated circuit correlator are determined. A much more complex digital processor module implemented in field programmable gate array (FPGA) technology which is used in a UWB transceiver is presented in [9]. A fully digital UWB receiver architecture based on TH-PPM approach is presented in [10]. The paper is organized as follows: in section II the clock synthesis together with transmitter and receiver architectures are described, then section III and IV give the simulation results and the conclusions, respectively.

II. TRANSCIEVER ARCHITECTURE
The UWB transceiver architecture for the UWB TAGs is based on a non-coherent structure utilizing bit position modulation (BPM) [13], [14].

While sacrificing some performance in term of spectral efficiency, it greatly simplifies the implementation and decrease the size and cost of the circuit. The architecture for the UWB TAG transceiver is presented in Fig. 1. The UWB signal used for this study is based on a train of short pulses multiplied by a spreading sequence using the direct sequence (DS) approach. The bit interval is divided into 2 time slots (binary modulation). As the detection procedure is based on energy collection, the separation of different users can only be done in the time domain. The transmitted signal for single user is given by equation (1).

\[ s(t) = \sum_{k=0}^{m} \sum_{\alpha=1}^{N} w_\alpha \left( t - kT_b - \delta \Delta T_j \right) c_p \]  

where \( w_\alpha(t) \) is the transmitted pulse with pulse width \( T_p \), \( T_b \) is the symbol interval, \( \delta = 125 \) ns is the delay used to distinguish different symbols and \( d_t \in [0,1] \) is the transmitted symbol. \( T = NT_p \) with \( N \) integer is the chip interval, and \( c_p \) is the \( j \)th chip of the pseudo-random (PR) code. The pseudo random (PR) code is bipolar with values \((-1,+1)\). Data rate \( R_d \) is defined by \( 1/T_b = 1/(2\delta) \).

A. TRANSMITTER ARCHITECTURE
The UWB transceiver clock generation is based on a 33 MHz crystal reference clock with high Q and DLL based frequency synthesis. Low reference clock frequency is used mainly because of low-power consumption requirements. For UWB system, timing is very important. Sub nanosecond pulses need to be transmitted using an accurate reference clock. Also at receiver, an accurate sampling is needed.

In this paper we utilize one DLL plus edge combiner in order to avoid classic frequency synthesis with PLL and N divider. The DLL-based clock multiplication approach presented in Fig. 2 takes advantages of the inherently low jitter of a low-frequency crystal oscillator reference to produce a low-phase-noise RF signal. This is accomplished by taking each relatively jitter-free but infrequent edge of the crystal oscillator output and from that generating a burst of well-controlled evenly spaced edges that span one period of the crystal oscillator. These evenly-spaced edges are combined by the AND-OR edge combiner to form a higher-frequency clock signal. The phase detector generates UP/DOWN signals according with the phase difference between the reference signal and the voltage controlled delay line’s (VCDL) final stage output. The phase detector architecture was presented in [15]. The DLL-CM is in locked condition, if the input and output of the voltage controlled delay line are in phase. One delay cell contains two cascading CMOS inverters. Delay is adjusted by the charge pump and loop filter through control voltage such that to minimize the phase error. A classification of charge pump architectures is given in [16]. Our charge pump architecture is based on a single ended architecture with output active amplifier [16].

Fig. 1. Circuit architecture of UWB TAG.
The charge pump produces the control voltage needed to fix the delay edges of VCDL within range of phase error tolerated by edge combiner. The control voltage controls the delay stages such that the phase error between input reference clock and final stage output of VCDL is 55 ps for all CMOS and temperature corners. The function of the edge combiner is to take the outputs of the DLL and generate a 528 MHz signal. For a clock multiplication of 16 we make use of 32 delay elements. Each delayed version DELAYi, i=1,..,32, of the reference clock is fed to the AND gate. Then each output of the AND gate, INj, j=1,..16, is fed in the OR gate. The RF 528 MHz clock signal is produced at the output of the OR gate.

In figure 3 the digital edge combiner based on AND-OR gates is presented.

The second DLL (DLL-PG) is used to fix a delay of UWB pulse generator. The difference between DLL-CM and DLL-PG is that the voltage controlled delay line of DLL-PG generate 120 ps delayed edges compared with 2 ns delayed edges in DLL-CM.

B. UWB Pulse Generator

The UWB pulse generator used in transmitter is presented in [16]. The structure and performance are more or less identical due to the use of the same IC process. The pulse generator creates two short pulses from two trigger signals which have a fixed delay between them. Here, the two trigger signals are provided by DLL-PG as presented in Fig. 1. The short pulses generated by NAND-gates are converted into a differential signals by a micro-mixer [18]. Two of these differential pulses with a fixed time delay are subtracted from each other in an analogue linear subtraction circuit. The output is a differential monocycle pulse with a typical pulse width of 500 ps.

C. RECEIVER ARCHITECTURE

The receiver is based on a simple power integration circuit. It contains low noise amplifier (LNA), variable gain amplifier (VGA), multiplication and integration circuits and 4-bit A/D converters, the digital control logic (DCL) and detection/bit decision block.

The incoming UWB signal is amplified by the LNA, squared in by a multiplier and then integrated. This technique has the disadvantage that, as well as signal, noise is amplified at the receiver. The used wideband LNA was presented in [19]. It consists of a single stage in common-emitter configuration and an emitter follower in the feedback path. Flat frequency response and matching to 50 Ω are achieved by emitter degeneration and shunt feedback including Q1, L1, R2 and R3.

The VGA was presented in [19] and is based on Gilbert cell [20]. The gain may be varied with a control voltage connected to the bases of the upper transistors. The control voltage range is from 1.36 V to 1.6 V, and the corresponding gain range is 36 dB from -17 dB to 19 dB, respectively. Two additional amplifier stages of the receiver contribute a fixed 40 dB gain, which gives a gain range from 40 dB to 75 dB for the receiver chain. The automatic gain control is digital so that there are four different control voltages and hence four different gain levels available. One of these is selected through monitoring the outputs of the A/D converters. If more than one of the outputs has the maximum value of '111', the gain is decreased, until only one achieves that value. On the other hand, if all of the outputs are at the minimum level, the gain is increased. The gain selection is made by the gain selection block as shown in Fig. 1. Receiver architecture contains a bank of 8 integrators. The integrator is a two stage integrator, which consists of a high-frequency Gm-C integrator presented in [21] and a differential operational amplifier in an inverting integrator configuration. Each of the integrators starts to collect the energy inside of a quarter of a bit time which is 30 ns. In order to have an accurate timing (start and stop instants) of the integration operation we make use of a digital control logic (DCL) based on eight 4 bit counters: one counter for each integrator. The principle of operation and results of DCL were presented in [19].

The automatic gain control (AGC) loop contains the integrator and gain selection logic (IGSL), squaring circuit, variable gain amplifier, a bank of eight integrators and eight 4 bit A/D converters. We use four integrators for energy
collection together with four 4 bit A/D converters for a bit time interval of 120 ns. The 4 bit A/D converters make use of medium speed, medium accuracy successive approximation architecture (SAR) [22]. The bit time interval equal four times the clock reference period. The integrator and gain selection logic (IGSL) contains digital logic which implements the integrator selection based on the outputs given by 4 bit A/D converters and gain selection on VGA. After the integrator selection is done by AGC, two energy collection values out of the integrators are fed into detection/bit decision logic block consisting of comparators. The detection/detection logic block produces the resulting bit to be processed by the baseband DSP block. The baseband DSP logic contains digital logic which implements the MASTER/SLAVE functionality of UWB TAG. Also, the DSP logic controls the transmission of DLL-PG and UWB pulse generator.

In Fig. 4, the beacon detection block is presented. The signal coming from integrators is converted to a digital value by the 4 bit A/D converters. Based on these digital values the selection of the maximum value is done by the maxselection block. The maximum on position i, i=1,..8, trigger the numerator NUMi, i=1,..8. After 40 bits of preamble the maximum selection between the integrator outputs is done. If there are more than one winner the selection is made randomly based on modulo operation. If the value of numerators NUMi, i=1,..8, is bigger than a predefine threshold the preamble is considered to be detected. The synchronization is achieved if the beacon is detected twice.

In Fig. 5 waveforms after the integrator winner detection are presented. Vector v contains a '1' in position i which means the winner is integrator number i, i=8, 4 respectively.

The basic state machine of the slave UWB TAG is presented in Fig. 6. Its functionality is described below. In DETECTION state, after PREAMBUL_SEARCH state, 63 bits are detected and then in BARKER_CORR state the barker correlation is executed in order to find the starting point of the information bits. Starting from this point the TAG counter counts 128 information bits and puts them in a receiving FIFO. In WAIT_FOR_SLOT_AFTER_RX state first block of data is loaded from transmission FIFO in transmission register. The UWB TAG waits for the moment to transmit. It transmits slots of 128 bits when it receives the slot address from MAC layer. When transmission FIFO is empty the UWB TAG goes to WAIT_FOR_SLOT_AFTER_TX state. When the TAG is in WAIT_FOR_SLOT_AFTER_TX state and the guard period of 20 bits is empty the TAG goes to DETECTION state. In DETECTION state, after WAIT_FOR_SLOT_AFTER_TX state, the TAG detect 128 bits and puts them in receiving FIFO in LOAD_FIFO state.

III. SIMULATION RESULTS

The transmitter architecture was tested independently with a 33 MHz clock input. The transmitted UWB pulse is presented in Fig. 7. The typical pulse width is 500 ps. Digital selection of the detected winner integrator is presented in Fig. 5.
IV. CONCLUSIONS

In this paper a low complexity architecture of an UWB TAG circuit transceiver has been presented. Circuits are designed in 0.35 Si-Ge BiCMOS process technology. Simulation results show that frequency synthesis based on delay-locked loop and digital AND-OR edge combiner is feasible for generating timing for UWB pulse transmission with pulse width of 500 ps. The corresponding centre frequency of the pulse is 2 GHz and the bandwidth at -10 dB is 4.03 GHz.

Timing signals out of the integrator winner detection block were presented. Also, the UWB transmitted pulse is presented. The UWB beacon detection block and slave state machine for UWB TAG were also presented.

REFERENCES


