HIGH-VOLTAGE SERIES MOSFET OUTPUT DRIVER FOR NANOMETER TECHNOLOGIES

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Abstract— This paper presents the stacked MOSFET as an integrated output driver for applications on planetary exploration probes. The stacked MOSFET is a scalable implementation of series connected MOSFETs for high-voltage monolithic switching applications. A single low-voltage input signal activates the first MOSFET, which in turn causes the entire stack of devices to turn on by charge injection through parasitic and inserted capacitances. Voltage division provides static and dynamic protection by balancing the output voltage across the stack so that the voltage seen by each device never exceeds its breakdown voltage. Simulations for a five device stack implemented in Honeywell's 150 nm process verify the static and dynamic voltage balancing of the output signal. The simulated stack is shown to handle five times the nominal operating voltage and verifies that the stack is scalable to accommodate voltages needed for drive actuators.

***Index Terms*—Capacitance, charge injection, integrated circuits, high-voltage techniques**

I. INTRODUCTION

ON-CHIP high voltage output drivers minimize power consumption and mass, which are critical commodities for atmospheric entry and descent probes. Stacked MOSFETs in combination with level shifters are one circuit technique to switch high-voltages on-chip. The stacked MOSFET can be fabricated in inherently radiation hard processes, which is another important consideration for space applications.

The stacked MOSFET enables rail-to-rail high voltage switching. The stacked MOSFET can be implemented in three topologies, the NMOS, the PMOS, and the push-pull. A five device NMOS topology takes a low-voltage (0 V to 3.3 V) input signal and the output switches 0 V to 15 V. The PMOS topology requires a level translated input signal (11.7V to 15V). The push-pull stack topology implements the PMOS and NMOS sections like a CMOS inverter, with the PMOS on top of the NMOS.

The stacked MOSFET could be used in a variety of ways in a planetary exploration probe. The push-pull topology can be used, for example, to create a buck, boost, or forward converter on-chip. As part of a converter, the stacked MOSFET takes a low voltage input and outputs a DC voltage level for electronics and sensors on a planetary probe. If the stacked MOSFET were scaled correctly it could drive 28V, which is required by some micro satellite thrusters.

The goal of this paper is to show that the stacked MOSFET can be used as a scalable high voltage driver for applications on planetary exploration probes. An overview of the Stacked MOSFET topologies (NMOS, PMOS, and push-pull) will be presented along with their design equations. Simulation results will be presented.

II. DERIVATION OF DESIGN EQUATIONS

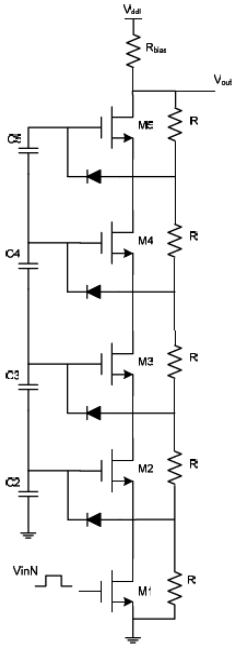

Fig.1 Schematic of a five-device Stacked MOSFET

Fig. 1 shows the topology for a five device NMOS stack. The MOSFETs are placed in series. In the off state, the voltage is divided equally across each device by the resistors so that none of the MOSFETs support a voltage greater than the break down voltage. In the on state, the gate-source voltage required to turn on each NMOS is set by the inserted and parasitic capacitance. As the stack grows, each capacitor in the stack must support a larger voltage, however the voltage rating of the capacitors is limited by the dielectric used between the

capacitor plates. The topology in Fig. 1 allows the capacitors to be scaled as the stack grows. The equations for the five device stack are based on the equations for an *n* device stack presented in [1].

A. Derivation of a Five-Device NMOS Stacked MOSFET

When Vin is low, all of the devices will be off, allowing the output to rise to Vdd assuming that

$$R_{bias} << 5R \tag{1}$$

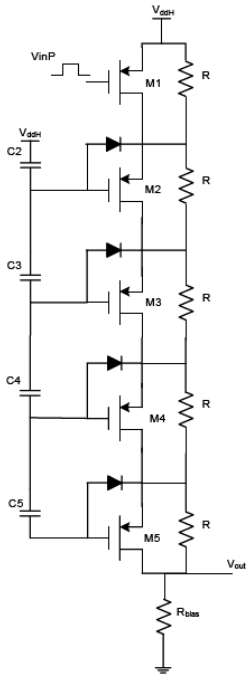

Fig.2 Schematic for a five-device PMOS stack

The drain voltages of the individual devices are set according to the voltage division across the resistors such that

$$V_{drain_k} = \frac{k \cdot R}{5R + R_{bias}} \cdot Vdd \tag{2}$$

Where V_{drain_k} represents voltage on the drain of the k^{th} device and all R's are equal. In the off state, the gate source voltage can be solved for as

$$V_{gs_k} = -V_{diode} \tag{3}$$

The devices are held off because the gate-source voltage is equal to the forward bias voltage of the diode.

When Vin switches from low to high, V_{drain1} is pulled to ground which reverse biases the diode and leaves the gate-source voltage of M2 to be set by the capacitive voltage division of the inserted capacitance C_k and the total lumped parasitic capacitance across the gate source [1]. Since the capacitors are tied together, C_k is a function of C_{k-1} and C_{k+1}. The value for C_k can be set such that the gate-source voltage will turn on M2, which will cause V_{drain2} to be pulled to ground and start to turn on M3. According to [1] $C_5 = C_{unit}$, $C_4 = 2C_{unit}$, $C_3 = 3C_{unit}$, and $C_2 = 4C_{unit}$. Where C_{unit} is defined as

$$C_{unit} = C_p \cdot \left(\frac{V_{drain2}}{Vgs + V_{diode}} - \frac{C_2 + 2C_p}{C_2 + C_p} \right)^{-1} \tag{4}$$

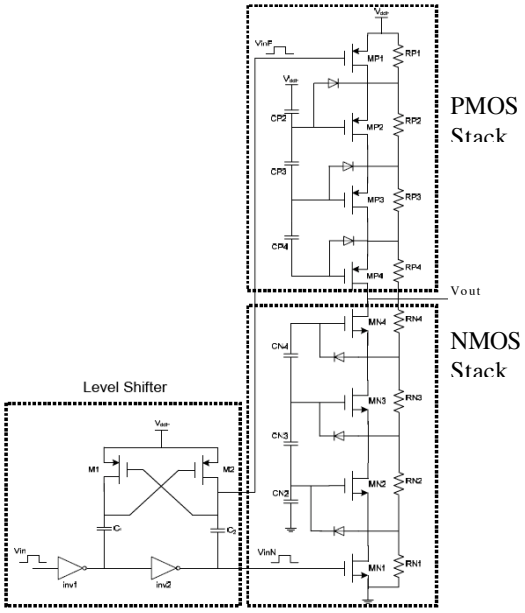

Fig. 3 Schematic for a push-pull stack

B. Derivation of a Five-Device PMOS stacked MOSFET

Fig.2 shows the topology for a five-device PMOS stack. The PMOS operates in a complementary fashion to the NMOS. The input for the PMOS needs to be level shifted to switch between Vdd and Vdd minus the nominal voltage. The drain voltages for the PMOS stack in the off state are still set according to voltage division across the resistors.

$$V_{drain_p} = Vdd \frac{(5-p) \cdot R}{5R + R_{bias}} \tag{5}$$

V_{drain_p} represents the voltage on the drain of the p^{th} device. The analysis for the PMOS stack is the same as the NMOS stack except V_{drain_p} is used in the equations instead of V_{drain_k}.

C. Derivation of a Five-Device Push-Pull Stacked MOSFET

The push-pull stack has the five-device PMOS stack connected in series with the five-device NMOS stack. The push-pull stack has ten devices, but functions as a five device stack. The benefit of the push-pull stack is that it has active

rising and falling edges. Fig. 3 shows the topology of the push-pull stack with a level shifter to provide the shifted input needed for the PMOS side of the stack. The push-pull stack is analyzed using the equations derived previously for the NMOS and PMOS topologies.

III. DESIGN AND SIMULATION

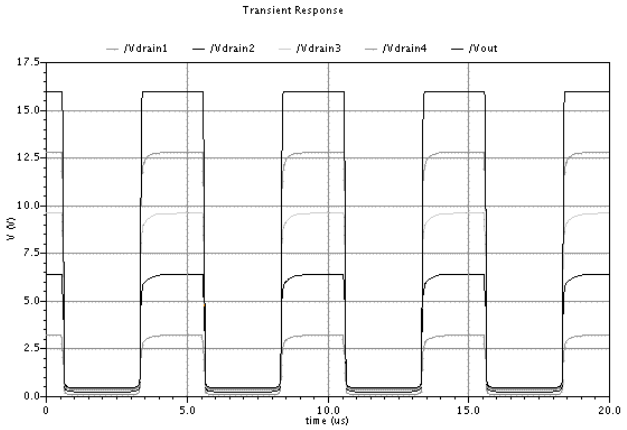

Fig.4 Drain Voltages for Five-Device NMOS stack

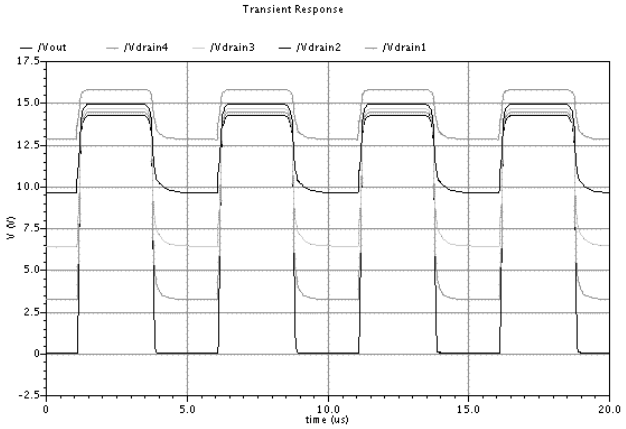

Fig.5 Drain Voltages for Five-Device PMOS Stack

The equations derived in the pervious section were used to design a five-device stack in the NMOS, PMOS, and push-pull topologies to be implemented in Honeywell's 150nm process. The nominal voltage for the NMOS and PMOS devices is 3.3 V. The circuits were designed to switch 15 V rail-to-rail. The models used in simulation were provided by Honeywell.

A. Five-Device NMOS Stacked MOSFET

The first step was to find the parasitic capacitance C_p. This was done by implementing a two device stack with C_2 equal to 1 pF. The circuit was simulated and V_{drain1}, V_{gs}, and V_{diode} were measured.

$$C_p = C_2\left(\frac{V_{drain1}}{V_{gs}+V_{diode}} - 1\right) \quad (6)$$

Equation (6) was used to find C_p = 478 fF. Then equation (4) was used to find C_{unit} = 759 fF. $C_5 = C_{unit}$, $C_4 = 2C_{unit}$, $C_3 = 3C_{unit}$, and $C_2 = 4C_{unit}$.

A two device stack was simulated using this C_{unit} to verify operation. Next a three device stack was simulated and the resistances and inserted capacitances were adjusted until the

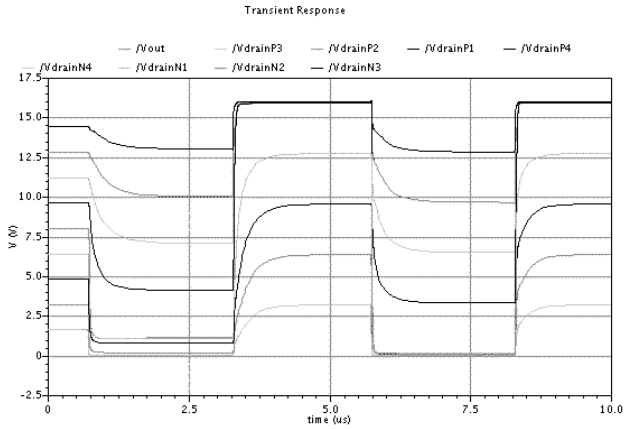

Fig.6 Drain Voltages for push-pull stacked MOSFET

stack simulated correctly. This process was repeated until the five device stack switched 0V to 15V rail-to-rail. The final values were R=80kΩ and C_{unit}= 759pF.

Fig.4 shows the drain voltages in the NMOS stack divide the output voltage equally across the stack so that none of the devices support a voltage greater than the breakdown voltage. The rising and falling edges show that the entire stack is turning on and off together, so output is balanced across the stack during the entire switching period. Fig.4 shows the active falling edge because the NMOS have an active pull down.

B. Five-Device PMOS Stacked MOSFET

The parasitic capacitance of the five-device PMOS stack was found the same way as that of the NMOS stack. A two-device stack was implemented using C_2 = 1pF. Using C_p in equation (4), C_{unit} = 1.6pf. $C_5 = C_{unit}$, $C_4 = 2C_{unit}$, $C_3 = 3C_{unit}$ and $C_2 = 4C_{unit}$.

The same iterative process used to design the NMOS stack was used to design the PMOS stack. The final values for the PMOS stack were R=80kΩ and C_{unit}= 1.16pF.

Fig.5 shows the drain voltages in the PMOS stack. Again the output voltage is divided equally across the entire stack. The rising and falling edges of the figure show the dynamic balancing of the output during turn on and turn off. Fig. 5 shows the active rising edge because the PMOS have an active pull up.

C. Push-Pull Stacked MOSFET

The NMOS and PMOS were put together and C_{unit}=1.16pF was used for each stack. Fig.6 shows the drain voltages for the Push-Pull stack. The figure again shows that the output is statically and dynamically balanced during the entire switching period so that no device supports a drain source voltage larger than the break down voltage. The Push-Pull stack has active rising and falling edges because of the active pull up of the PMOS stack and the active pull down of the NMOS stack.

IV. Conclusion

This paper presented the design equations and simulation results for a five-device stack in NMOS, PMOS, and push-pull topologies in Honeywell's 150nm process. The simulations showed that the stacked MOSFET is a scalable circuit technique to handle high-voltage switching. The five-device stack presented is currently in fabrication. The five-device stacks were able to switch five times the nominal voltage for the individual devices, as predicted. Simulated results for the five-device NMOS stack correlate with the experimental results for a two-device NMOS stack presented by [2]. Experimental results have verified an integrated stacked MOSFET could drive a 28V load for microsatellite actuators. Therefore, the Stacked MOSFET can be scaled to reach any voltage required by an application; the limitation to the maximum voltage being the breakdown voltage of the substrate.

All of the Stacked MOSFET topologies showed monolithic switching capabilities in simulations and experiments with static and dynamic balancing of the output signal. The stacked MOSFET has been realized in discrete and integrated configurations. Therefore the stacked MOSFET could be using in large DC-DC power converters in discrete configuration or in small integrated point-of-use DC-DC power converters. The DC-DC converters could be used to power sensors, electronics, actuators, and a variety of scientific devices on a planetary exploration probe.

The stacked MOSFET presented is an integrated high-voltage driver that has a low voltage input, so it reduces mass and power which are critical considerations for space. The Honeywell 150nm process is a radiation hard process, so in this process the stacked MOSFET is radiation hard by process. These characteristics make the stacked MOSFET well suited for space applications.

References

[1] E.Mentze, The Stacked MOSFET: A Self-Biased Scalable High-Voltage Switching Circuit for Application to Low-Voltage Nanometer Scale CMOS Technologies and Discrete Power Electronics, Idaho, University of Idaho, Dec 2006.

[2] E. Mentze, H. Hess, K.M. Buck, and T. Windley, "A Scalable High-Voltage Output Drive for Low-Voltage CMOS Technologies" IEEE Trans. VLSI Systems, vol.14, no.12, pp. 1347-1353, Dec 2006.

[3] H. Ballan and M. Declercq, *High Voltage Devices and Circuits in Standard CMOS Technologies*. Norwell, MA: Kluwer, 1999.

[4] T. Yamaguchi and S. Morimoto, "Process and device design of a 1000-V MOS IC," *IEEE Trans. Electron Devices*, vol. 29, no. 8, pp. 1171–1178, Aug. 1982.

[5] V. Rumennik and D. L. Heald, "Integrated high and lowvoltage CMOS technology," in *IEEE Int. Electron Devices Meeting Dig., Abst. 4.3*, 1982, pp. 77–80.

[6] Z. Parpia, J. G. Mena, and C. A. T. Salma, "A novel CMOS compatible high voltage transistor structure," *IEEE Trans. Electron Devices*, vol. 33, no. 12, pp. 1948–1952, Dec. 1986.

[7] K. M. Buck, H. W. Li, S. Subramanian, H. L. Hess, and M. Mojarradi, "Development and testing of high-voltage devices fabricated in standard CMOS and soi technologies," in *Proc. 11th Annu. NASA Symp.VLSI Des.*, 2003, pp. 157–163.

[8] N. Iwamori, S. Mizuno, H. Fujino, and K. Kawarnoto, "Mixed process IC on SOI wafer for automotive application," *JSAE Rev.*, vol. 22, no. 2, pp. 217–219, Apr. 2001.

[9] E. J. Mentze, K. M. Buck, H. L. Hess, D. Cox, and M. Mojarradi, "A low voltage to high voltage level shifter in a low voltage 0.25 _m, PD SOI process," in *Proc. IEEE Annu. Symp. VLSI*, 2004, pp. 218–221.

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