Compare and Contrast HiSIM-HV and BSIM based compact model of High Voltage MOSFETs for Analog Applications

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ABSTRACT

A pair of scalable models, one utilizing the Surface Potential-based HiSIM-HV 1.0.2 model, and the other, the conventional Vth-based BSIM3v3.24 model, were extracted based on a test vehicle designed with both Drain-Extended CMOS and LDMOS Transistors. All devices were designed with a single fixed channel length but varying drift length and width. The test vehicle is processed using Fairchild Semiconductor's 0.35µm, BiCMOS/DMOS process. The key difference between the HiSIM-HV and BSIM3-based macro models is that BSIM3 model required additional elements to model the extended drift region where the potential based HiSIM-HV contains an intrinsic drift element. The two models are then compared and contrasted in two major areas: 1) Model Accuracies, including L_{dr} (Length of the drift region) scaling, 2) Model Performance in an actual CAD Environment, Cadence ADE running MMSIM 7.1 in this case, including simulation speeds, convergence stability, relative accuracies under both DC and Transient Simulations. Finally, conclusions are presented to reflect the viability of each model in the current Analog-Mixed-Signal Applications and Designs.

Keywords: hisim, ldmos, high-voltage, power, analog

1 INTRODUCTION

In recent years, high-voltage MOSFET transistors have moved from the world of discrete devices to being part of a fully scalable integrated circuit environment where they co-exist with standard MOSFETs and other standard devices. The high-voltage (HVMOS) and laterally-diffused (LDMOS) transistors typically have an extended drain/drift region and are asymmetric. In order to facilitate a fully integrated design, an accurate and efficient compact model for is needed for accurately simulating these transistors. Until recently, there has been no industry standard for high-voltage MOSFET modeling, so macro models were constructed using standard BSIM model(s) with additional elements for simulating the extended drain region, extended diode performance, and other advanced features[1],[2]. Recently, the Compact Model Council (CMC) has selected the HiSIM-HV model as the industry standard for HVMOS and LDMOS transistors. In this paper, we will compare the traditional approach of the BSIM macro model with the stand-alone HiSIM-HV model comparing simulation and fitting with experimental data.

2 BSIM MACRO MODEL VS. HISIM-HV MODEL

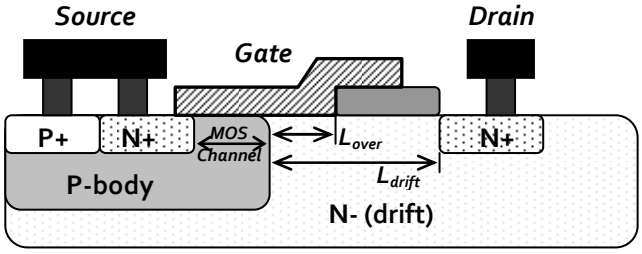

Figure 1: Typical cross-section of N-type HVMOS/LDMOS transistor.

2.1 Extended-drain MOS Architecture

High-voltage MOSFET devices usually have a unique architecture where there is an extended drain or drift region. The reason for this extended region is to allow higher voltages on the drain terminal than can be sustained on the gate oxide. The source side is similar to a typical MOS in the asymmetric case.

The drain side is somewhat complicated and can be broken into three regions. The standard MOS channel region, the drift region under the polysilicon gate, and the drift region not under the gate. The channel region is treated like a standard MOSFET which we will call the core device. The drift region is essentially a resistance between the active MOS channel and the drain terminal. The length of this extension determines the maximum voltage that can be applied to the drain terminal. In addition, part of the drift region is under the poly gate and then the rest of the drift region extends to the drain terminal.

To properly characterize these regions, both the current and capacitance needs to be defined. The current portion can be defined as a resistance that extends from the drain terminal of the aggregate device to the drain terminal of the core device. Looking at the architecture, the portion of the

resistance under the gate will be affected by the V_{gs} and the rest of the resistance is a lightly doped diffused region which will be dependent upon the voltage on the drain terminal[3]. Finally, in cases where there is a separate body connection from the source, the V_{bs} will also impact the resistance. This gives a drift resistance, R_{drift}, of:

$$R_{drift} = f(V_{gs}, V_{ds}, V_{bs})$$

The difficult part is defining the functions to describe R_{drift}. The drain current saturates, first, through the velocity saturation of the drift region before the channel reaches saturation through pinch-off which is what is called quasisaturation. This makes characterizing the drift resistor especially at high V_{ds} and high V_{gs} very critical.

The capacitance in the drift regions (under and not under the gate) is complex and is highly dependent upon drift region doping. It has been observed in both 2-D device simulations and in measurements that at high V_{gs} the drain resistance bears the bulk of the voltage drop. The profiles of C_{gd} and C_{gs} are quite different for the LDMOS architecture. When the V_{gs} is swept from negative to positive, the C_{gd} behaves normally in the "off" state. As V_{gs} approaches, an electron accumulation charge forms in the drift region that is under the gate. The C_{gd} then peaks around V_{th}. At $V_{gs} > V_{th}$, the core MOS channel starts to invert and the drift region becomes more resistive, the charge shifts from the drift region to the channel of the core MOSFET. This leads to C_{gd} decreasing and an increase in C_{gs}. Depending on the drift region and doping, the portion of the capacitance shared by C_{gs} and C_{gd} will be different, though for physical consistency these will never be greater than the gate oxide capacitance when the channel is fully inverted. It has been shown through 2-D simulations, that lighter doped drift regions lead to higher peaks in the Cgd. It has also been observed that the Cgd can peak greater than the total oxide capacitance (C_{ox}•WL). So it is key to be able to model this distributed behavior of the capacitance especially in the C_{gd} region where there is significant peaking as the device is turning on[4].

2.2 High-voltage MOSFET Modeling

The traditional approach to HVMOS modeling is to use a standard BSIM3/4 MOSFET model coupled with external elements to emulate the extended drift/drain region. This approach is uses a standard BSIM MOSFET model that is available in most simulators and allows the modeling engineer to use behavioral or other circuit elements to customize the drift region, self-heating, breakdowns, etc. In some cases, the MOSFET is modeled as 2 MOSFET devices in series which gives more accurate results in the subthreshold but tends to have convergency issues with the internal "floating" node. Since for years there has been no industry standard for this type of model, there are several variations on this formulation found in the literature which have advantages and disadvantages.

In 2008, the CMC selected the HiSIM-HV as the standard for high-voltage MOSFET modeling. This comprehensive model includes all of the standard MOSFET model elements as well as the features that are unique and important to extended drain devices (Ldrift scaling, unique capacitance phenomena, self-heating, etc.)

2.3 BSIM-based Macro Model

The BSIM-based macro model approach has been used for many years and has followed many different paths. Inherent to all of these models is the use of the BSIM Vth-based model as the "base". The BSIM model uses a gradual channel approximation and charge sheet approximation for the drift-diffusion approximation established by Pao, Sah. Another feature of the BSIM model is it is a "regionally" based model where the Ids is determined by different equations in different regions. This lead to discontinuities in the Ids so special "smoothing" equations for $V_{gs}(V_{gseff})$, $V_{ds}(V_{dseff})$ and $V_{bs}(V_{bseff})$ were created to smooth out the discontinuities.

Originally, this yielded a simpler model which is based on applied voltages. As technology progressed and device features shrunk, more and more parameters and equations were added to account for the discrepancy in the equations at small geometries. This has led to the 100+ parameter BSIM3/4 model that we see today. Finally, the BSIM3 model also assumes a symmetric geometry that does not lend itself well to most HVMOS architectures.

In addition to the MOSFET element, most HVMOS models use external elements to simulate the drift region. Some models use non-physical parameters in the BSIM model for *A0*, *AGS*, *DELTA*, *PCLM*, etc. to mimic the behavior seen in drain-extended devices but these are often not scalable and have fitting problems in other regions of the device. The typical approach is to use behavioral or other elements to emulate the drift region resistance. Some approaches use a JFET for modeling this region but it has some drawbacks and limitations in fitting over both V_{ds} and V_{gs}. Other approaches use various versions of empirical equations to approximate the resistance in the drift region. These approximations also have certain limitations in fitting and are independent of the MOSFET. The BSIM model lacks the self-heating feature that is very important in power MOSFET modeling. Our approach has been to implement the self-heating into the drift resistor element but this ignores the thermal changes in the MOSFET as the device is thermally elevated.

Additional approaches also include capacitive elements for better modeling of the channel capacitance. The unique nature of the gate capacitance in the LDMOS structure is not easily implemented using the BSIM macromodel approach. The "bump" in the C_{gd} can be implemented using a behavioral capacitance model but this model must be both V_{ds} and V_{gs} dependent[5]. However, since this element is independent of the core MOS device, the shifting of the charge from C_{gd} to C_{gs} cannot be implemented properly. Behavioral capacitances are also notoriously known for causing convergence and simulation slowdown.

This is most likely due to causing issues with charge conservation.

Finally, in most cases, a separate drain-body diode is implemented since the BSIM diode has some limitations as well as its assumed symmetry between source and drain is not valid.

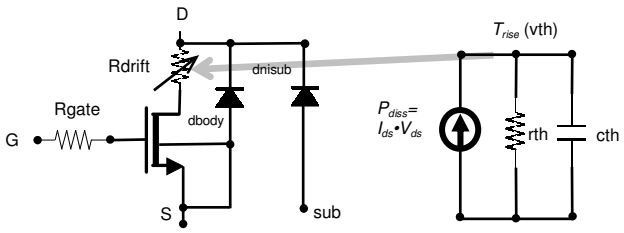

Fig. 2: BSIM HVMOS macromodel subcircuit

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All of these approaches lack some vital elements necessary to produce a physically consistent model for the high-voltage MOSFET. The V_{th} approximation model used by BSIM does not lend itself easily to adding the extended drain region due to its use of gradual channel approximation. Also, due to the subcircuit architecture, the BSIM model sees a reduced V_{ds} value since there is a voltage drop across the drain region, so the subcircuit elements operate independently making it more difficult for good physical parameter extraction.

2.4 HiSIM-HV Model

The HiSIM standard model was developed as more physical alternative to the BSIM model using the standard drift-diffusion approximation but using surface potential mechanics for model development. This application allows the MOS transistor to use a unified Ids equation rather than the "zone" fitting with smoothing functions used in BSIM models. Also, the HiSIM approach incorporates the actual physics of the short-channel and narrow-channel effects rather than using fitting functions. Polysilicon depletion effects are also implemented into the HiSIM approach[6].

The surface potential approach all insures that all charges are explicitly represented which in turn insures that all the capacitances are self-consistent. This means there are much fewer "fitting" parameters resulting in a reduced parameter set for the model, but since all aspects of the model are interrelated, it also means that the extraction must be much more rigorous for all regions to fit properly.

The HiSIM-HV (high-voltage) is an extension of the standard HiSIM model. The HiSIM-HV model adds the addition of the drain/drift region in the HVMOS or LDMOS architecture into the model formulation which includes all charges (current and capacitance). By this inclusion, all the surface potential to be completely calculated across the device within a single model[3].

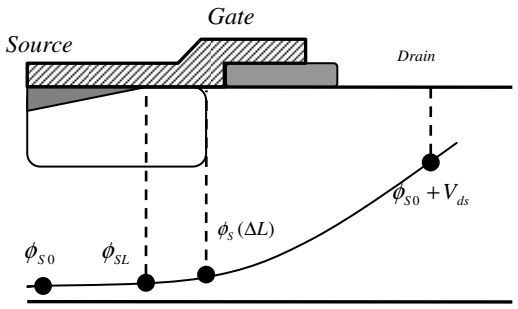

Fig. 3: Surface potential distribution of HVMOS architecture.

The HiSIM-HV model uses physically consistent drift region properties coupled with the standard HiSIM channel properties to produce a physically consistent complete model from source contact to drain contact. The φ_{SO} is the suface potential at the source side, φ_{SL} is the surface potential at pinch-off, $\varphi_S(\Delta L)$ is the channel-drain junction potential in the core MOS, and $\varphi_{S0}+V_{ds}$ is the final potential value at the drain terminal. This methodology also allows for the correct capacitances to be correctly computed across the channel and at various gate and drain voltages. The inclusion of the drift resistance along with improved capacitance modeling parameters allow the HiSIM-HV model to use a single model deck to properly characterize the drift resistance region for both current and capacitance.

The HiSIM-HV model also adds some physical phenomena to the intrinsic model that are not found in the BSIM model or even in the BSIM macromodel. The HiSIM-HV includes a self-heating (SH) model that applies to the entire device. This is different from the BSIM macromodel where the self-heating cannot impact the BSIM model directly. Also, the self-heating is internal to the model, so you don't have the convergence and "phantom" current issues that you have with a self-heating subcircuit.

3 RESULTS AND COMPARISONS

The best way to compare the fitting and performance of the BSIM macromodel and the HiSIM-HV model is to use actual device measurements. With several different types of devices and architectures available, we looked at 3 different devices: N-type LDMOS, P-type LDMOS and N-type HVMOS. All of these architectures use an extended drain or drift region to allow higher voltages on the drains.

Similar comparison results were seen for all 3 different types of transistors. The focus in this paper will be on the N-type LNDMOS device. We look at the model fittings w.ith I_d vs V_g and V_d, C vs V_g as well as over temperature measurements.

3.1 DC Measurements

One key aspect of model comparison is the forward operating DC characteristics especially in the operational region of the MOSFET. For most applications, HV MOS transistors operate in the linear or low-V_{gs} saturation region. In most linear region applications, the device is used in a switching configuration where the V_{ds} is low (~0.1V) and V_{gs} is full "on" ($V_{gs} >> V_{th}$). In this mode, the drain/drift resistor is somewhat dependent on V_{gs} but since V_{ds} is so low, there is little effect of drain voltage on the channel resistance. Because of this phenomena, the fitting is very similar to traditional MOSFET fitting. There is usually little issue fitting the BSIM macromodel in this region. The HiSIM model also is primarily using the standard HiSIM 2.4 model to fit this region. Comparing the fits for both BSIM macromodel and HiSIM-HV, both fits are very good. The BSIM has a little advantage in fitting the subthreshold region on the Id-Vg curve since the NFACTOR fitting parameter is available. HiSIM does not have such a parameter since it is surface-potential based and uses a uniform equation to fit all regions.

For higher-V_{gs}, the I_{ds}-V_{gs} curve is much better fitting for the HiSIM-HV model vs the BSIM3 macromodel. This is due to the better fitting of the HiSIM-HV model in the quasisaturation and saturation regions.

They are not usually operated in the high-V_{gs} saturation region. Imposing this application regime on the device, the traditional model extraction using the BSIM macromodel sacrificed fitting in the high-V_{gs}/V_{ds} region of the transistor for better fitting in the linear and quasisaturation regions. Even in these regions the HiSIM-HV model fits very well. This is important for some analog applications and highly capacitive loads where the device is saturated at high V_{gs}.

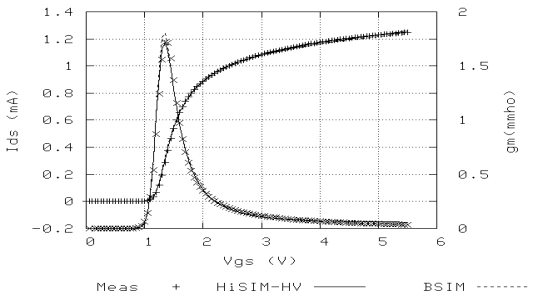

Figure 4: I_{ds} vs V_{gs} @ V_{ds} =0.1 for HiSIM-HV vs BSIM

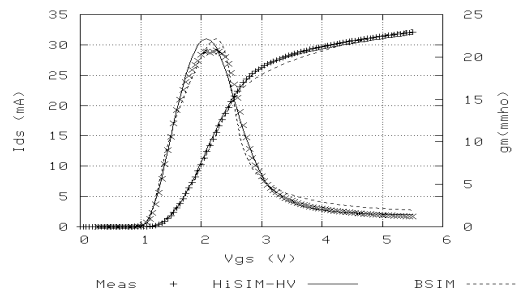

Figure 5 I_{ds} vs V_{gs} @ V_{ds} =5.0, HiSIM-HV vs BSIM

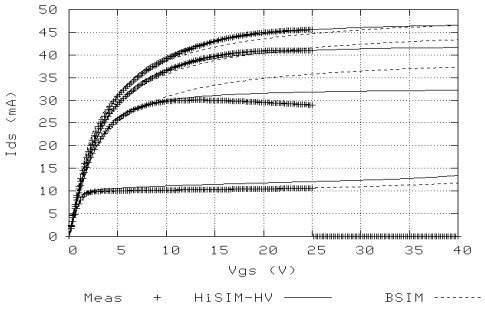

Figure 6: I_{ds} vs V_{ds} @ V_{gs} =2,3,4,5; HiSIM-HV vs BSIM

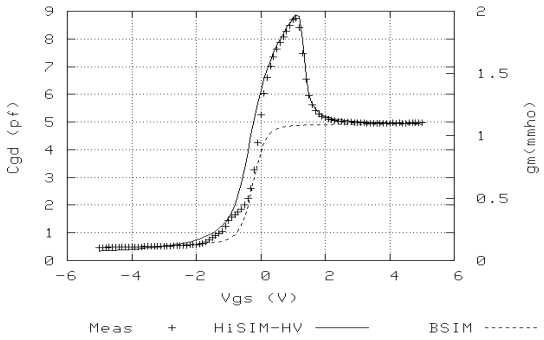

Figure 7: C_{gd} vs V_{gs} @ V_{ds} =0; HiSIM-HV vs BSIM

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