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FIELD PROGRAMMABLE ANALOGUE ARRAY BASED ON MOSFET TRANSCONDUCTORS

E. K. F. Lee and P. G. Gulak

Indexing terms: Programmable logic arrays, Semiconductor devices and materials, Field-effect transistors, Logic devices

An area efficient and parasitic insensitive technique for the implementation of a field programmable analogue array is proposed. The connections between configurable analogue blocks are realised using MOSFET transconductors. The conductance is controlled by varying the gate voltages defined by a multivalued memory system or external/internal signals.

Introduction: Field programmable gate arrays for prototyping digital circuits are now commercially available from several vendors. Conspicuously absent in the literature is a field-programmable analogue array (FPAA) and perhaps for good reason because many more factors must be addressed such as bandwidth, linearity, signal-to-noise ratio, frequency response, etc.; to address these, we developed one approach to realise a field programmable analogue array [1] that used subthreshold current-mode techniques. The reconfiguration for different analogue functions and the connections between them were made by pass transistors activated by a set of configuration bits. However, this approach is not appropriate for linear analogue circuit applications due to the parasitic effects of the pass transistors. In this Letter, a new technique is proposed to eliminate the parasitic effects. At the same time, high linearity, noise immunity and area efficiency are achieved.

When a pass transistor is used as a switch, nonideal effects such as nonlinear resistance and parasitic capacitance will affect the signal passing through it. To circumvent these effects, four-transistor transconductors [2] shown in Fig. 1

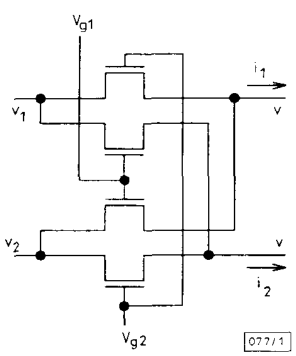

Fig. 1 *Four-transistor transconductor*

can be used as switches. The parasitic capacitance in each transistor is cancelled due to transistor matching and differential signalling. The transconductor is the 'off' state when the gate voltages are low. The transconductance G_{on} in the 'on' state is

$$G_{on} = \mu C_{OX} \frac{W}{L} (V_{g1} - V_{g2})$$

$$\text{for } v_1, v_2 \leq \min\left[V_{g1} - V_T, V_{g2} - V_T\right]$$

The transconductance is linear within the above ranges. Therefore, we can use this technique for three purposes: on/off switch, polarity change switch and variable resistor.

Based on the transconductance technique, a new architecture for the implementation of a field programmable analogue array is proposed as shown in Fig. 2. It consists of two crossbar interconnection networks, multivalued memory refresh circuits, an array of programmable differential voltage or current sources, and an array of configurable analogue blocks (CABs). Each line represents a differential wire and the circles represent the MOSFET transconductors. The two interconnection networks are the VRIN (variable resistor interconnection network) and the SCRN (signal controlled resistor network). The gate voltages of the transconductance in the VRIN are controlled by multivalued memories [3, 4]. The gate voltages in the SCRN are controlled by the output voltages of the CABs or external input signals. Therefore, the SCRN allows the realisation of four-quadrant multipliers and dividers [5], and time-varying circuits.

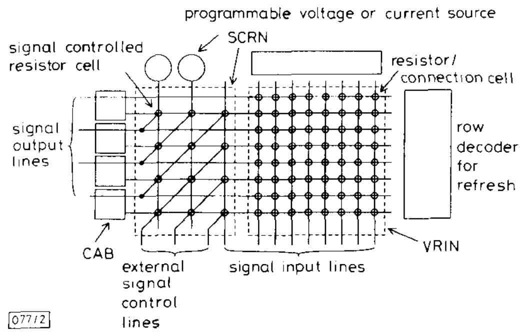

Fig. 2 *Architecture for field programmable analogue array*

The CABs consist of either configurable active or passive (diodes and capacitors) elements. Because MOSFET transconductors combined with different types of active element have been applied to different analogue signal processing problems (for example, continuous time filter [6]), different types of active elements such as opamps and current amplifiers can be used for the CABs. However, different choices of active element will lead to different tradeoffs in the entire array design and circuit performance. Opamps with capacitors controlled by switches are chosen for the CAG as shown in Fig. 3. The programmable sources can be constructed using multivalued memories with voltage or current amplifiers as buffers.

To demonstrate the flexibility of this architecture, two circuits are embedded in the FPAA. Fig. 4 shows a fully differential continuous time biquad circuit embedded into the FPAA.

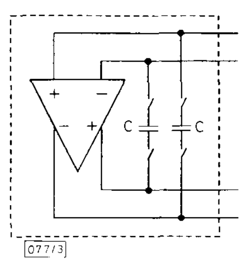

Fig. 3 *Schematic diagram of CAB*

The CABs are configured as integrators (differential opamps with feedback capacitors). Different transfer functions can be programmed by controlling the gate voltages of the transconductors through the multivalued memories. The frequency

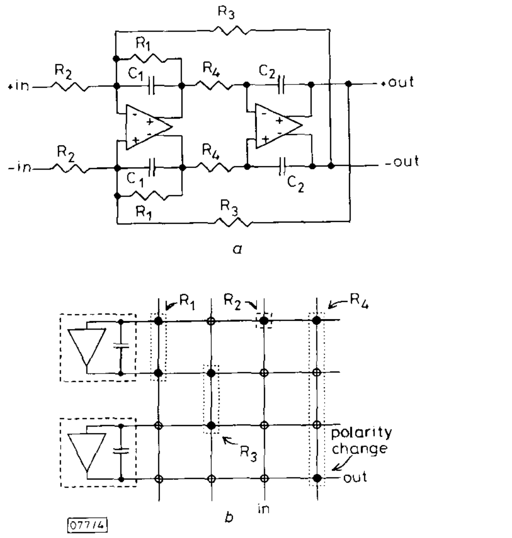

Fig. 4 *Schematic diagram of fully differential biquad and its embedding into FPAA*

a Schematic diagram
b Embedding of biquad into FPAA

response of the filter will not be affected by the parasitic capacitance of the transconductors and the connection wires because the parasitic capacitance will be cancelled in a first order approximation due to differential signalling. The second circuit which realises a simple VCO is shown in Fig. 5*a*. It consists of an integrator, a multiplexer and a comparator with hysteresis. If the differential control voltage v_c is set to a constant voltage, v_1 will increase (decrease) as time increases. When v_1 is higher (lower) than the upper (lower) threshold voltage of the comparator, the multiplexer will select different polarities of v_c. As a result, v_1 and v_2 will oscillate and the frequency of oscillation will be dependent on the RC time

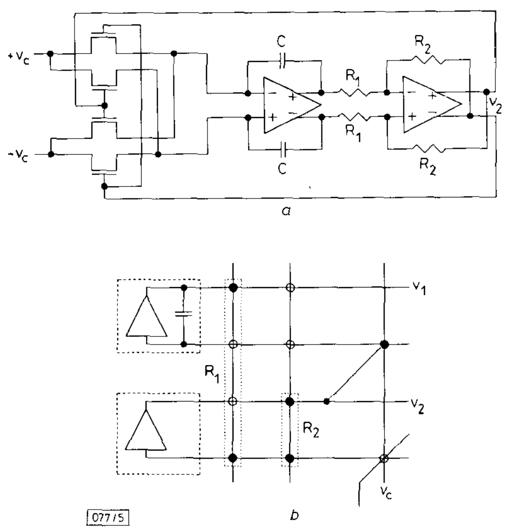

Fig. 5 *Schematic diagram of VCO and its embedding into FPAA*

a Schematic diagram
b Embedding of VCO into FPAA

constant, the threshold voltages and the control voltages. The comparator with hysteresis is realised by an opamp with positive feedback resistors. The circuit can be embedded into the array as shown in Fig. 5*b*.

Conclusion: A new FPAA architecture is proposed which consists of two crossbar interconnection networks formed by MOSFET transconductors, a multivalued memory system, arrays of CABs and programmable sources. The proposed design uses the connection switches in the interconnection networks as resistors (variable or signal controlled) and switches (on/off or polarity change). Die area use using the proposed design is higher than that of previous designs [1] because the interconnection networks also operate as programmable functional elements. Furthermore, the parasitic effects and noise due to the interconnection networks will be eliminated by differential signalling. In addition, the high linearity of the MOSFET transconductance allows the proposed design to fulfill a wide range of applications.

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ULTRAHIGH-SENSITIVITY LOW COHERENCE OTDR USING Er^{3+}-DOPED HIGH-POWER SUPERFLUORESCENT FIBRE SOURCE

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Indexing terms: Light sources, Optical fibres

The first-known demonstration of an Er^{3+}-doped superfluorescent fibre source coupled to a high-resolution OTDR based on low coherence interference (low coherence OTDR) is reported. Linearly-polarised light with 14 mW output from the source achieves a −146 dB minimum detectable reflectivity at 3 Hz bandwidth. The spatial resolution determined by spectral FWHM is 28 μm for silica-based waveguides.

Introduction: Optical time domain reflectometry based on low coherence interference (low coherence OTDR) is a promising candidate for diagnosing miniaturised optical waveguides [1, 2]. Increasing the dynamic range of the Rayleigh backscattering measurement using the OTDR requires a high-power broadband light source because the sensitivity at the shot-noise limited operation increases with the available power of the light source used. When superluminescent diodes (SLDs) are employed, the minimum detectable reflectivity is limited to ~ −140 dB due to the available optical power of ~1 mW [3]. Recently, superfluorescent fibre sources using rare-earth-doped fibres have been developed to provide more than