A Design Strategy for a 1-V Rail-to-Rail Input / Output CMOS Opamp

Christian Jesus B. FAYOMI 1, Mohamad SAWAN 1 and Gordon W. ROBERTS 2

1 Ecole Polytechnique de Montreal, Department of Electrical and Computer Engineering
P.O Box 6079, Station "Centre Ville", Montreal, CANADA H3C 3A7
2 Microelectronics and Computer Systems Laboratory, McGill University
Montreal, CANADA H3A 2A7
Email: {fayomi, roberts}@macs.ece.mcgill.ca | sawan@vlsi.polymtl.ca

ABSTRACT

A design strategy for a rail-to-rail input / output operational amplifier in standard CMOS 0.18 µm digital process with a 0.5-V threshold is presented. It uses a novel level shifting technique of the input signal and a dynamically biased class AB output stage based on a switched-capacitor configuration. The amplifier is capable of working with a power supply as low as 1-V while providing a 26.6 MHz unity gain frequency and a 67 degree phase margin with a load condition of 5 pF and 20 kΩ. The overall circuit dissipates 400 µW.

1. INTRODUCTION

A fundamental building block in low-voltage design is the operational amplifier (opamp). Unlike the transconductance amplifier, it includes an output stage capable of driving off-chip resistive loads. Obviously, the output stage must respect the specification requirement for drive capability, linearity and output swing. Another critical aspect in low-voltage design is the common-mode input swing, which depends on the input stage.

In recent years, much effort has been put into the reduction of the supply voltage and the supply power of mixed-signal CMOS systems. This is primarily due to the increasing importance of battery-powered electronics, and a continued down-scaling of device sizes. Three main reasons can be given for the advent of low-voltage circuits. As the channel length is scaled down into submicrons and the gate-oxide thickness becomes only several nanometers thick, the supply voltage has to be reduced (down to 1.5 V and below in the near future) in order to ensure device reliability. The second reason emanates from the increasing components on a single chip. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic function per unit area, the power per electronic function has to be lowered in order to prevent overheating of the chip. The third reason is dictated by portable, battery-powered equipment. In order to have an acceptable operation period from a battery, both the supply power and the supply voltage have to be reduced.

A particular consequence of the lowered power supply is the need for rail-to-rail input stages in order to compensate for the reduced input common-mode and dynamic range. The power dissipated by analog circuitry, however, does not necessarily decrease when the supply lowers, as the traditional stacking of transistors has to be replaced by folding techniques, which inevitably increases the current drawn from the supply. Hence, to decrease the power dissipated in low-voltage analog circuits, the design has to be kept as simple as possible.

In order to maximize the dynamic range, a low-voltage amplifier must be able to deal with signal voltages that extend from rail-to-rail. Such efforts have been underway for several years now. In CMOS op amp circuits, improved input range operation has been achieved by connecting complementary (nMOS and pMOS) differential amplifiers in parallel. However at extremely low-voltage supply (1-V and below) classical solutions are being replaced by new configurations. A novel design strategy based on a switched-capacitor arrangement is described here for an extremely low-voltage opamp circuit. The block diagram of the opamp is shown in Figure 1. The main analog building blocks are discussed in section 2 and preliminary results are introduced in section 3.

2. RAIL-TO-RAIL INPUT / OUTPUT OPAMP

2.1. Input Level Shifter Circuit

The most commonly used input stage for an opamp is a single differential pair. It can be composed of either a p-channel or a n-channel input pair. In a well-designed low-voltage (LV) opamp the minimum supply voltage value is imposed by the differential pair of the input stage, and is given by [4]:

\[ (V_{DDA})_{min} = V_{th} + 2 \cdot |V_{DSsat}| \]  

where \( V_{th} \) is the threshold of the input stage device and \( V_{DSsat} \) is the saturation voltage of the devices. For typical CMOS processes, this value turns out to be around 1 V. On the other hand, the main limitation of differential pairs results from the reduced input common-mode (CM) range. For a n-channel input pair, this is given by:

\[ V_a < V_{CM} < V_{DDA} \]  

where

\[ V_a = V_{SSA} + V_{DSsat} + 2 \cdot |V_{DSsat}| \]  

\[ V_{SSA} \text{ and } V_{BDJO} \text{ being the negative and positive supply, respectively.} \]

The CM of a p-channel input pair is given by:

\[ V_{SSA} < V_{CM} < V_b \]  

where

\[ V_b = V_{DDA} - |V_{th,p}| - 2 \cdot |V_{DSsat}| \]  

To avoid this drawback, the traditional solution has been based on using parallel-connected complementary pairs in the input stage [2] as shown in Figure 2a. Basically at least one of the input pairs is adequately biased for any value of the input CM voltage. However, the situation is drastically different when the total supply voltage is further reduced, as shown in Figure 2b. Now a forbidden amplifier operation zone arises for input CM voltages in the middle range: the input voltage is not able to turn on any transistor in this range, and therefore the amplifier operation is limited to CM input voltages.
close to either supply rail. To overcome this limitation, the concept of dynamic level-shifting has been proposed for bipolar operational amplifiers [5]. A similar method has been reported in [3] for CMOS based operational amplifier circuits. These methods have been implemented in the continuous time domain and the level shifter circuit dissipates a static power. A switched-capacitor based approach is proposed here to realize the level shifting function and is depicted in Figure 3a with its clocking circuitry (Figure 3b). This limits the circuit to sample data applications. The level shifter circuit makes use of the control circuit of a pMOS bootstrapped constant impedance switch described in [6]. When the clock signal is low, the gate voltage of the pMOS type input differential transistor is set to V_DD and therefore is off. At the same time node b is set to V_DD + V_shift. The charge Q_ch1 stored in capacitance C_b is given by:

\[ Q_{ch1} = C_b \cdot V_{shift} \]  \hspace{1cm} (6)

where V_shift is an arbitrary voltage greater than the threshold of the pMOS input pair devices.

When the input clock signal goes high, the transmission gate formed by N2 and P2 starts conducting the input signal V_in. Charge stored in capacitance C_b thus becomes:

\[ Q_{ch2} = C_b \cdot (V_n - V_{dd}) \]  \hspace{1cm} (7)

Using the charge conservation principle, the input drive voltage of the differential pair can be derived from (6) and (7) and is given by:

\[ V_{ddo} = V_{in} - V_{shift} \]  \hspace{1cm} (8)

Equation (8) shows that a linear relation exists between the input signal and the control voltage of the differential pair. The input voltage is therefore level-shifted down. The value of this voltage is low enough to turn on the differential pair at any input CM level and therefore suppress the forbidden operation zone of the opamp. The input CM is typically between -1 and 0 V for an input signal varying from 0 to 1 V and for a V_shift equal to 1 V. Reliability is not a concern since a 1.8 V technology is used at a 1 V supply voltage.

2.2. Differential input pair

The input stage is shown in Figure 4. It is made up of the source-coupled pair M1-M2 and the folded cascode mirror (MN1-MN2). Transistors MS1 and MS2 have been added to enhance the slew-rate performance of the folded cascode circuit [7]. When the operational amplifier is slew-rate limited, these transistors prevent the drain of M1 and M2 from having large transients that change their small-signal voltages to level very close to the positive power-supply voltage. The purpose of transistor MRa is to sink the biasing current of the input stage when the clock signal is low, thus avoiding this node being charged to V_DD. However, this transistor can be removed without any damage to the circuit. The body of the input source coupled transistors M1-M2 is tied to a high voltage 2 V_DD. Assuming that the biasing current of the differential pair is 2 I_BIAS, the source-gate voltage of transistor M1 (or M2) is given by:

\[ V_{sg} = V_{na} = \frac{2 I_{bias}}{\mu C_{ox} (W/L)_{M1}} \]  \hspace{1cm} (9)

Remembering the fact that the gate-voltage of M1 is given by (8), the source-voltage of M1 (node a) is given by:

\[ V_a = V_{in} - V_{shift} + \sqrt{\frac{2 I_{bias}}{\mu C_{ox} (W/L)_{M1}}} \]  \hspace{1cm} (10)

For a CM signal close to the negative supply voltage (V_SSA), and for a small value of bias current, the value of this voltage is close to that of node c. Therefore the behaviour of the circuit is no longer similar to that of a differential pair. Several solutions can be used. The first method is to increase the bias current level. This approach leads to an increase of the power dissipation of the circuit. The second solution is to use large length devices, which in turn increases the parasitic capacitance at this node and the overall circuit area. Another possibility is to slightly increase the threshold voltage of the source-coupled input pair device. This method has been adopted here due to the fact that we have a voltage close to 2 V_DD on-chip.

2.3. Class AB output stage

A dynamically biased class AB output stage similar to the design reported in [8] has been used and is shown in Figure 5. All the switches are implemented with nMOS transistors and are driven by the clock booster of Figure 3a. Switch S_in has been added to reduce the output capacitance seen by node VOD and thus increases the circuit unity gain bandwidth (UGBW).

2.4. Alternative implementation

Another possibility is a nMOS implementation of the level shifter circuit as depicted in Figure 6. It uses a generalisation of the nMOS bootstrapped switch method. A linear relation exists between the input signal and level shifter output and is given by:

\[ V_{ddo} = V_{in} + V_{shift} \]  \hspace{1cm} (11)

The related nMOS differential pair is shown in Figure 7. The functionality of the circuit is similar to the pMOS implementation and the same output stage configuration can also be used.

3. PRELIMINARY RESULTS

The proposed implementation has been simulated with HSPICE using BSIMv3. A 0.18 µm digital CMOS technology has been used. Threshold voltages are approximately 0.52 V and -0.48 V for nMOS and pMOS transistors respectively. The frequency response of the circuit is depicted in figure 8. The amplifier operates with a supply voltage as low as 1-V, provides a 26.6 MHz unity gain frequency and a 67 degree phase margin with a load condition of 5 pF and 20 kΩ. The overall circuit power dissipation is 400 µW. The step input response shown in Figure 9 uses a dc model of the input level shifter circuit. The level shifter circuit has been used in a previous design [6] that is already submitted for fabrication. Layout of key component (level shifter) has been submitted for fabrication and some experimental will follow soon. The overall circuit layout is in progress. Fringing capacitance have been extensively used in the implementation of the capacitors because of the non-availability of poly-poly capacitors [9].

4. CONCLUSION
A novel design strategy for a 1-V rail-to-rail input/output operational amplifier has been proposed. It uses a novel level shifting technique of the input signal and a dynamically biased class AB output stage based on a switched-capacitor arrangement. The amplifier is capable of operating with a power supply as low as 1-V while providing a 26.6 MHz unity gain frequency and a 67 degree phase margin with a load condition of 5 pF and 20 kΩ. The circuit dissipates 400 µW. Layout of key component (level shifter) has been submitted for fabrication and some experimental will follow soon. The overall circuit layout is in progress. Applications of the circuit extend from sample-data systems to switched-capacitor filter and rail-to-rail data converters, to name just a few examples.

REFERENCES

Figure 1: Low-voltage CMOS rail-to-rail input/output opamp block diagram

Figure 2: (a) Typical input stage for rail-to-rail opamp; (b) Operation zones for low supply voltage operation; (c) Operation zones for extremely low supply voltage operation.

Figure 3: (a) pMOS input level shifter; (b) Clock booster circuit.
Figure 4: Low-voltage pMOS input stage

Figure 7: Low-voltage nMOS input stage

Figure 5: Low-voltage output stage

Figure 6: nMOS level shifter

Figure 8: Frequency response of the opamp

Figure 9: Step input response of the opamp