Abstract—A methodological study of an electronic ballast for electrodeless fluorescent lamps (EFLs) including design and development issues is presented in this paper. The ballast is intended to feed a 100-W EFL at 250 kHz with dimming feature. The proposed topology is composed of a single-ended primary-inductance converter, used as power-factor (PF)-correction stage, integrated with a resonant half-bridge inverter, used as lamp-power control stage. The integration of both stages is proposed in this paper, in order to reduce the number of active switches, as well as to simplify the required driving and control circuity for this application. Experimental results demonstrate the feasibility of the proposed solution that achieves 54% lamp-power dimming (46 W). The implemented topology attained very high PF (0.989) and low line-current total harmonic distortion (14.929%), without using electromagnetic interference filter, while the measured efficiency was 87% at nominal lamp power.

Index Terms—Electrodeless fluorescent lamps (FLs) (EFLs), high power factor (PF), high switching frequency, integration technique.

I. INTRODUCTION

NOWADAYS, a great amount of the electrical energy used worldwide is consumed as artificial lighting. One way to reduce the electrical energy consumption is the use of high-frequency electronic ballasts feeding discharge lamps. Lighting systems based on fluorescent lamps (FLs) became popular due to their well-known features as, for example, high luminous efficiency and good color rendering index (CRI), as shown in [1]–[3]. However, the traditional FLs have low lifetime, approximately 10 000 h [4], compared with the electrodeless FL (EFL), which can reach 100 000 h [5]. The presence of electrodes in traditional FLs is the main issue to cause lamp malfunction; in addition, they are responsible for energy loss and complicating the ignition process [6].

The absence of electrodes is the main advantage of EFLs that makes possible a higher lifetime, with low lumen depreciation [7]. Moreover, at the present time, this technology makes possible to build EFLs up to around 1000 W of rating power [8]. This type of lamp presents a CRI higher than 90, with color temperatures between 2700 and 6500 K. In addition, the lamp can achieve up to 110 lm/W of luminous efficiency [9].

The electromagnetic interference (EMI) filter is designed to eliminate the harmonic components generated by the high-frequency switching of the PF correction (PFC) stage, because otherwise, high-frequency harmonics can decrease the system PF and cause interference problems with other equipment. The requirements for this first stage will depend on the selected converter and design methodology. Standards establish that FL electronic ballasts must have a PFC stage for powers above a determined power level. For example, IEC 61000-3-2 Class C regulation limits the harmonic content of the current drained from the line, and it is particularly stringent for powers above 25 W [11]. For EFL having therefore a power higher than 100 W, the inclusion of a PFC stage results mandatory.

The voltage-fed inverter with resonant load is widely used in FL systems as power control (PC) stage. This circuit typically employs a half-bridge inverter to generate the square waveform

Fig. 1 shows some different EFL models, as shown in Fig. 2, which should provide satisfactory lamp operation, fulfilling the standards of power factor (PF) and efficiency of the energy drained from the grid [10].

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applied to the resonant load and set the lamp operating frequency [12], [13].

The dimming process for lamps has been discussed in several papers [14]–[17]. However, this issue is still open to discussion. The performance of a lighting system with controlled light intensity must meet the requirements of the standard C82.11 [18], which regulates high-frequency FL ballast operation, as well as the quality of the utility power supply. The dimming systems are generally more expensive than traditional ones without dimming, but as an advantage, their outcome will provide energy savings. Properly designed systems can achieve a reduction in consumption of up to 50% with operating frequency control [19] or more than 60% when combined with other methods of dimming [20], whereas the luminous flux of FLs is proportional to the power supplied to them. Besides saving energy, a dimmable system provides adequate lighting to perform activities, and also, when compared to electromagnetic ballast, it can avoid problems in viewing monitors, audible noise, flicker, and stroboscopic effect [21].

In this paper, an integrated converter that incorporates both the PFC and the PC stages is proposed. A methodology for achieving luminous flux control in this type of integrated converters is also investigated. For the PFC stage, a single-ended primary-inductance converter (SEPIC) topology is employed, while for the PC stage, a half-bridge resonant inverter is used. Both of them will operate at the same switching frequency \( f_s \) given by the lamp requirements. The proposed converter is then intended to drive an EFL-type 100-W Icetron/Endura from Osram operating at 250 kHz. Electrical, built, and lighting features of this lamp are presented in [8] and [9].

This paper is organized as follows. In Section II, the EFL model and equivalent circuits are presented. Section III deals with the SEPIC as PFC stage and with the analysis of the integration between PFC and PC stages. In Section IV, the dimming methodology is presented, and the limits imposed by the PFC stage are analyzed. Section V presents a design of the SEPIC half-bridge integrated converter. Section VI shows the prototype and experimental results, and Section VII describes the conclusions of this paper.

II. ELECTRICAL MODEL OF THE EFL

The electrical model for discharge lamps is a concept widespread in the literature [22], [23]. In this section, an electrical model for the EFL is presented. The model is intended to represent the EFL electrical behavior as a function of the lamp power, and it can be employed to analyze the converter operation under both nominal and reduced power operations.

The EFL under study presents two external coils \( (L_{CORE}) \) connected in parallel. These coils act as a primary winding of a transformer, and the load of the secondary winding corresponds to the plasma inside the discharge tube. In this way, the energy transfer from the external coils to the electric discharge occurs via the electromagnetic field generated by the inductors, thus producing the luminous radiation.

Fig. 3 shows the simplified EFL electrical model under study. Owing to their closed magnetic path, the external coils have a coupling factor close to unity [24]. The lamp can then be represented by a parallel network given by an equivalent resistance \( (R_{LP}) \) and an equivalent inductance \( (L_{LP}) \).

In this paper, the control of the lamp luminous flux is pursued. To obtain it, the EFL equivalent inductance and resistance as a function of the lamp power are mandatory. The lamp model can be acquired by using a voltage-fed resonant inverter to supply the lamp. By varying the dc input voltage applied to the inverter, the lamp power can be modified. Thus, from the measured lamp current and voltage waveforms at each operating point, the equivalent resistance and inductance can be obtained. It has been found in [25] that suitable expressions to model the lamp equivalent resistance and inductance as a function of the lamp average power \( (P_{LP}) \) are given by

\[
R_{LP}(P_{LP}) = R_1 e^{P_{LP}/P_1} + R_2 e^{-P_{LP}/P_2} \quad (1)
\]

\[
L_{LP}(P_{LP}) = A_3 P_{LP}^3 + A_2 P_{LP}^2 + A_1 P_{LP} + A_0. \quad (2)
\]

Following this process, the 100-W Icetron/Endura from Osram was modeled in a previous paper [25]. Table I shows the parameters obtained for this particular lamp. Fig. 4 shows the variation of the EFL equivalent inductance and resistance as a function of the lamp power.
TABLE I
EFL LAMP MODEL PARAMETERS OBTAINED FOR THE 100-W ICETRON/ENDURA FROM OSRAM

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>2.497 Ω</td>
</tr>
<tr>
<td>$R_2$</td>
<td>43.22 Ω</td>
</tr>
<tr>
<td>$P_1$</td>
<td>52.63 W</td>
</tr>
<tr>
<td>$P_2$</td>
<td>7.41 W</td>
</tr>
<tr>
<td>$A_3$</td>
<td>0.0020 μH/W^3</td>
</tr>
<tr>
<td>$A_2$</td>
<td>0.328 μH/W^2</td>
</tr>
<tr>
<td>$A_1$</td>
<td>-18.97 μH/W</td>
</tr>
<tr>
<td>$A_0$</td>
<td>1330.2 μH</td>
</tr>
</tbody>
</table>

Fig. 4. Equivalent inductance and resistance as a function of the lamp power for the 100-W Icetron/Endura EFL.

III. SEPIC INTEGRATED WITH HALF-BRIDGE RESONANT INVERTER

This paper proposes the integration of the PFC and the PC stages, in order to reduce the number of active switches, as well as their respective control circuits. The integration technique is the combination of two controlled switches in a single one. As a condition, both switches must have at least one common node [26]. One limiting factor of the integration technique is that both stages, PFC and PC, being integrated will have the same switching period ($T_s$) and duty cycle ($D$) imposed on the shared switch. After the integration, each stage will keep its own characteristics independently, as if there were no circuit component sharing [27].

Fig. 5 shows the proposed topology in its nonintegrated form. Fig. 6 shows the integrated topology. As commented previously, it is made up by a SEPIC as PFC stage and a half-bridge resonant inverter as a PC stage.

A. SEPIC as PFC Stage

The SEPIC is suitable to be employed as a PFC stage and output voltage regulator in the proposed topology. This converter is attractive because it operates as a voltage step-down or step-up stage, depending on the imposed duty cycle. Another advantage is that the output voltage has the same polarity as the input voltage, thus simplifying control and protection circuitries. The flyback PFC topology may also be considered as an alternative to feed the half-bridge inverter. One of the features of this topology is the insulation between input and output. However, when applied to the integration technique, the flyback topology intrinsic insulation no longer takes place. In this way, the flyback topology resembles the buck–boost topology where leakage inductances and core size are reduced.

The noninversion of the output voltage and the possibility of input filter elimination are some features that lead to the use of SEPIC PFC instead of buck–boost PFC topology. In addition, if the input inductance used in the SEPIC ($L_1$) is high, the line current will present inherently low ripple, thus requiring small EMI filter components that, in some cases, may be eliminated. This reduces the number of stages, increases efficiency, and decreases cost.

The SEPIC can be operated in continuous conduction mode (CCM) and/or discontinuous conduction mode (DCM). Given the low power level intended for the proposed application (< 300 W) and in order to simplify the control circuit, the DCM is chosen [28]. In this way, the SEPIC operating in the DCM with constant duty cycle and switching frequency behaves as a resistance to the ac line, thus assuring high-input PF.

B. Half-Bridge Resonant Inverter as PC Stage

The use of a high-frequency half-bridge inverter, followed by a resonant filter, to perform the lamp starting and stabilization in steady state is consolidated in the literature [12].

The resonant load consists of an LCC filter, associated with the EFL electrical model. The operating frequency is given by the half-bridge inverter, which usually operates, near the filter resonant frequency during starting process. The resonant filter is used to adapt the square waveform supplied by the inverter, attenuating the high-order harmonic components and supplying the lamp with sinusoidal waveforms [29]. A number of criteria must be considered when designing this circuit, so that the lamp can be satisfactorily driven. For example, the circuit must provide the required lamp ignition voltage and limit the current in steady state to its nominal value.
D. Operation Stages

In this section, the operation stages of the SEPIC half-bridge converter are presented. The equivalent circuits for each operation stage are shown in Fig. 7. In the analysis, the resonant filter current is considered sinusoidal, and the semiconductors are considered ideal switches. Fig. 8 shows the main operating waveforms. In the following, the operating stages of the proposed integrated topology are presented.

**Stage 1** \((t_0 \rightarrow t_1)\): In this stage, switches \(S_2\) and \(S_{1,3}\) are off. The SEPIC is in its freewheeling interval, where current \(i_{L1}\) is equal to \(-i_{L2}\). The resonant current \(i_F\) flows through diode \(D_2\).

**Stage 2** \((t_1 \rightarrow t_2)\): In this stage, switch \(S_{1,3}\) is turned on, and switch \(S_2\) is off. In the SEPIC, \(V_g\) is applied to the input inductor \(L_1\), while the voltage across capacitor \(C_1\) is applied to inductor \(L_2\). In this stage, the resonant current circulates through diode \(D_2\), and switch \(S_{1,3}\) is subjected only to the SEPIC current. This stage ends when the current through diode \(D_2\) reaches zero due to the inversion of the resonant current.

**Stage 3** \((t_2 \rightarrow t_3)\): In this stage, \(S_{1,3}\) is conducting, diode \(D_2\) is off, and the resonant current circulates through diode \(D_{HB}\) and switch \(S_{1,3}\). In the SEPIC topology, \(L_1\) and \(L_2\) are still being energized by the input voltage and \(C_1\) capacitor voltage, respectively.

**Stage 4** \((t_3 \rightarrow t_4 \rightarrow t_5)\): In this stage, \(S_{1,3}\) is turned off. In the half-bridge inverter, the resonant current circulates through the body diode of switch \(S_2(D_Y)\). In the SEPIC, the inductors \(L_1\) and \(L_2\) are de-energized by the voltage across capacitor \(C_{bus}\). Both inductances and resonant circuit supply current to the \(C_{bus}\) capacitor. In this stage, \(S_2\) is turned on; however, the resonant current circulates through the body diode of \(S_2\), so the switch \(S_2\) is turned on with zero voltage, thus achieving zero voltage switching (ZVS).

**Stage 5** \((t_5 \rightarrow t_6)\): In this stage, \(S_2\) is conducting. The resonant current reverses and begins to circulate through switch \(S_2\).

**Stage 6** \((t_6 \rightarrow t_7)\): In this stage, diode \(D_1\) current reaches zero, characterizing the DCM operation. The resonant current...
circulates through switch $S_2$. The SEPIC enters in freewheeling mode, where the currents through inductors $L_1$ and $L_2$ are equal in magnitude ($i_R$) and have the direction shown in Fig. 7(f). At the end of this stage, switch $S_2$ is turned off, reaching stage 1 and repeating the process.

IV. Dimming Methodology—Analysis of the Limits Imposed by the PFC Stage

A. Proposed Dimming Methodology

The dimming feature can be achieved through different methods: frequency modulation [17], [30], pulsewidth modulation [31], changing the output filter parameters [32], [33], burst-mode technique [34], and by controlling the bus voltage [17], [35].

In [17], a comparison between the EFL dimming methods, considering frequency and bus-voltage variation, is carried out. Results presented in [17] show that the bus-voltage-variation technique provides approximately a linear feature in relation to the lamp power.

In this paper, the variation of the bus voltage is investigated to incorporate dimming capability to the proposed electronic ballast. The duty cycle of the integrated switch is varied in order to control the bus voltage ($V_{bus}$) and, consequently, the power delivered to the lamp. One advantage of this method is that, owing to the PFC stage behavior, a nearly linear characteristic between the bus voltage and lamp power is achieved.

The converter input power depends directly on the duty cycle applied to the PFC stage. Thus, the greater duty cycle, the greater input power, and, also, the higher lamp power, the greater $V_{bus}$.

The minimum power delivered to the lamp is determined by the minimum value of the duty cycle that can be achieved to assure DCM operation. This limit is given by the relation between peak input voltage ($V_{pk}$) and bus voltage, as shown in

$$D < \frac{V_{bus}(P_{LP})}{V_{bus}(P_{LP}) + V_{pk}}$$

(3)

As long as the duty cycle is decreased, the bus voltage is also reduced, while the line peak voltage remains constant. As can be seen therefore from (3), there will be a minimum duty cycle for which (3) is not fulfilled, thus entering in CCM mode, increasing line-current distortion, and decreasing PF. From the values of the lamp model, $R_{LP}(P_{LP})$ and $L_{LP}(P_{LP})$, and the rest of the components of the resonant filter, the total impedance of the resonant filter $Z_T(P_{LP})$ can be obtained as functions of the lamp power, as shown in

$$Z_T(P_{LP}) = Z_P(P_{LP}) + Z_S$$

(4)

where $Z_P$ is the equivalent impedance of $L_{LP}$, $R_{LP}$, and $C_P$ and $Z_S$ is the equivalent impedance of $L_S$ and $C_S$ and can be obtained by (5) and (6), respectively, with $\omega_S = 2\pi f_S$

$$Z_P(P_{LP}) = \left\{ \frac{1}{R_{LP}(P_{LP})} + j \right\} \times \left[ \omega_S C_P(P_{LP}) - \frac{1}{\omega_S L_{LP}(P_{LP})} \right]^{-1}$$

(5)

$$Z_S = j \left( \frac{\omega_S^2 L_S C_S - 1}{\omega_S C_S} \right).$$

(6)
Using the total impedance $Z_T(P_{LP})$, the necessary rms voltage to be applied to the input of the resonant tank ($V_{ab}(P_{LP})$) for a given lamp power can be calculated as follows:

$$V_{ab}(P_{LP}) = \sqrt{P_{LP} R_{LP}(P_{LP})} \left| Z_T(P_{LP}) \right| Z_T(P_{LP}) .$$

Taking into account that the voltage applied to the resonant filter is a square voltage with a 50% duty cycle, the required bus voltage ($V_{bus}(P_{LP})$) for a given lamp power is finally obtained as shown in

$$V_{bus}(P_{LP}) = \frac{V_{ab}(P_{LP}) \pi}{\sqrt{2}} = \frac{\pi \sqrt{P_{LP} R_{LP}(P_{LP})}}{\sqrt{2}} \left| Z_T(P_{LP}) \right| Z_T(P_{LP}) .$$

The limits imposed by the PFC stage can then be analyzed employing (3) and (8) for any particular converter, as it will be shown in Section VI.

B. Variation of Resonant Load Phase Angle Under Dimming Operation

The lamp luminous output is changed by varying the lamp power. This lamp-power variation causes changes in the lamp electrical parameters that, in turn, modify the phase angle of the total impedance that loads the resonant inverter.

The phase angle of the total resonant load ($\phi$) can be calculated as a function of the lamp power as shown in

$$\phi(P_{LP}) = \tan^{-1} \left\{ \frac{\text{Im} \left[ Z_T(P_{LP}) \right]}{\text{Re} \left[ Z_T(P_{LP}) \right]} \right\} .$$

The analysis of the phase angle of the resonant load results very important in order to verify whether the switch $S_2$ will be operating under ZVS mode.

V. DESIGN METHODOLOGY

The design of the SEPIC half-bridge electronic ballast is summarized according to the following steps.

A. Input Data

The first step consists in defining the main electronic ballast data: lamp frequency operation, peak input voltage, lamp power, and bus voltage. These parameters must be defined for the nominal lamp power.

B. Resonant Filter

The LCC resonant filter is chosen according to the electrodeless lamp requirements and characteristics. The filter design must consider a number of criteria for the satisfactory system operation such as provide the lamp ignition voltage, limit lamp current, and provide a symmetrical voltage waveform to the lamp. The LCC resonant filter design methodology has been previously presented in [36] and [37].

The values of the resonant filter components are determined by using (10) and (11). The series capacitor $C_S$ value is defined in the project taking into account that it must have a sufficient value to remove the dc voltage applied to the resonant filter. Its value is usually selected to be around 10–20 times the value of the parallel capacitance $C_P$

$$C_P = \left\{ \frac{1}{\omega_S R_{LP}} \sqrt{\frac{P_{LP} R_{LP}}{V_{ab}^2}} \left[ 1 + (\tan(\phi))^2 \right] - 1 \right\} + \frac{1}{\omega_S^2 L_{LP}}$$

$$L_S = \frac{\tan(\phi) R_{LP} + \omega_S R_{LP}^2 C_P}{\omega_S (1 + C_P^2 R_{LP}^2 \omega_S^2)} + \frac{1}{C_S \omega_S^2} .$$

The phase angle of the resonant load is selected so that the nominal lamp power can be obtained at steady-state operation. It must also be taken into account that, during the lamp starting, the switching frequency must be close to the filter resonant frequency in order to provide enough voltage gain to assure lamp ignition. In addition, the switching losses of the half-bridge inverter can be minimized by designing the converter so that the resonant current is lagged with respect to the voltage applied to the resonant tank. This is achieved by designing the total resonant load so that it presents an inductive behavior. In this way, at the instant in which the shared switch is turned off, the resonant current is forced to circulate through the body diode of switch $S_2$ [Fig. 7(d)], which must be turned on before the resonant current reaches zero. This process assures that the switch $S_2$ will enter in conduction mode with nearly ZVS mode. Owing to the behavior of the SEPIC as PFC, the shared switch $S_{1,3}$ does not present ZVS feature, but as it operates in DCM and the resonant load behaves inductively, it also presents soft-switching operation with zero losses during the turn-on process.

C. SEPIC Half-Bridge

Through the operation stages presented previously, it is observed that the integrated topology comprises the steps of both SEPIC PFC and resonant inverter, which are analyzed individually. Thus, it is possible to perform a design for both stages independently. The SEPIC topology, operating under DCM, can be represented using the equivalent circuit shown in Fig. 9 [38].

In Fig. 9, the current source $i(t)$ represents the output current of the PFC stage averaged within each line period and can be calculated as shown in (12). The resistances $R_{SEPIC}$ and $R_{HB}$ represent the PFC and PC stage equivalent input resistances, respectively, and are given by (13) and (14), respectively.
Owing to the resistive load emulation performed by the SEPIC stage, a high PF is assured

\[
i(t) = \frac{D^2T_sV_{pk}^2\sin^2(\omega t)}{2L_{eq}V_{bus}} \tag{12}\]

\[
R_{SEPIC} = \frac{2L_{eq}}{D^2T_s} \tag{13}\]

\[
R_{HEB} = \frac{4L_{eq}V_{bus}^2}{D^2T_sV_{pk}^2} \tag{14}\]

In the SEPIC topology, due to the location of the inductive elements \(L_1\) and \(L_2\), the power transfer is determined by an equivalent inductance \(L_{eq}\), corresponding to the parallel association of both inductances, as given by

\[
L_{eq} = \frac{V_{pk}^2D^2T_s}{2P_{L}} \tag{15}\]

Inductors \(L_1\) and \(L_2\) can be obtained using (16) and (17), respectively, where \(i_{\text{ripple}}\) corresponds to the maximum input-current ripple, which takes place at the peak line voltage \(V_{pk}\). This ripple is usually an input data for the design of the converter [38]

\[
L_1 = \frac{V_{pk}DT_s}{\rho_{\text{ripple}}} \tag{16}\]

\[
L_2 = \frac{L_1L_{eq}}{L_1 + L_{eq}} \tag{17}\]

In the design of the SEPIC, the voltage across capacitor \(C_1\) can be assumed constant within a switching period, but at the same time, it must follow the line-voltage low-frequency variation. When operating as PFC stage, the resonant frequency \(f_R\) given by \(C_1\), \(L_1\), and \(L_2\) must be higher than the line frequency, in order to avoid input-current oscillations within each line half cycle. Additionally, the resonant frequency given by \(L_2\) and \(C_1\) must be lower than the switching frequency, so that a constant voltage within a switching period can be assured [39]. In this way, capacitance \(C_1\) can be obtained for a given resonant frequency \(f_R\) using

\[
C_1 = \frac{1}{(2\pi f_R)^2(L_1 + L_2)} \tag{18}\]

D. Switch Voltage and Current

The main efforts of voltage and current in the switches are given to the condition of nominal lamp power.

The peak voltage on \(S_{1,3}\) and \(S_2\) are \((V_{pk} + V_{bus})\) and \(V_{bus}\), respectively. Due to the proposed integration, the shared switch \(S_{1,3}\) must handle, during stage 3, the sum of the input current and the load resonant current. Equation (19) defines the shared switch instantaneous current, where the variable \(k\) corresponds to an integer counter, which starts at zero and is incremented in each switching period

\[
i_{S_{1,3}}(t) = \begin{cases} 
G(t), & \text{if } kT_s \leq (t-t_d) < [kT_s + \frac{\theta}{2\pi}] \\
H(t), & \text{if } [kT_s + \frac{\theta}{2\pi}] \leq (t-t_d) < [kT_s + DT_s] \\
0, & \text{otherwise} 
\end{cases} \tag{19}\]

\[
i_{S_{1,3}}(t) = \frac{2P_{L}}{Z_p}, \quad K_{S_{1,3}} = \frac{kT_s}{Z_p}, \quad T_{S_{1,3}} = \frac{T_s}{Z_p} \tag{20}\]

The \(S_2\) rms current is obtained from

\[
i_{S_{2}}(t) = \sqrt{\int_{t}^{t+T_s} [i_F(t)]^2 dt} \tag{21}\]

VI. Prototype and Experimental Results

This section presents the parameters of the proposed SEPIC half-bridge converter and its experimental results. The converter was designed according to the methodology presented in Section V. Table II shows the converter parameters, components, and lamp parameter nominal power.

Using the input data shown in Table II, the EFL characteristic values and impedance angle \(\theta = 38^\circ\), the resonant filter components can be calculated based on (10) and (11).
Equation (3) is used in order to determine the maximum duty cycle that can be imposed to the PFC stage at nominal power. The duty cycle is selected to be slightly below this maximum value so that DCM operation is assured. In this case, the maximum duty cycle utilized in $S_{1.3}$ is 0.44. In order to determine the switch $S_2$ duty cycle, it is necessary to define the dead time ($t_d$) between half-bridge switches. In this design, a $t_d$ of 240 ns was considered at rated power. Because of this, the switch $S_2$ duty cycle is defined to be 0.44. Switches $S_{1.3}$ and $S_2$ control signals are generated by a microcontroller. Switch $S_2$ is maintained with a fixed duty cycle and switch $S_{1.3}$ duty cycle changes according to the dimming level. Under dimming operation, as long as the switch $S_{1.3}$ duty cycle is decreased to reduce lamp power, $t_d$ will automatically increase in the same amount, thus assuring safe operation of the converter switches.

Once the duty cycle has been determined, the values of the inductances $L_{eq}$, $L_1$, and $L_2$ are calculated for the nominal lamp power using (15)–(17). Capacitance $C_1$ is determined using (18) so that the resonant frequency $f_{R}$ is ten times lower than the switching frequency which, in this case, is 25 kHz. Consequently, the resonant frequency given by $L_2$ and $C_1$ is approximately 100 kHz.

Reducing the converter power, by decreasing the duty cycle $D$, diminishes $V_{bus}$ as shown by (8). Using (22) and taking into account that $V_{pk} = 311$ V, it is possible to determine the minimum $V_{bus}$ imposed to the PFC stage in order to assure DCM operation. Relating (8) and (22), as shown in Fig. 10, the lower limit of $D$ can be determined

$$V_{bus_{min}}(D) = \frac{V_{pk}D}{1-D}. \quad (22)$$

Thus, in order to assure DCM operation for the PFC stage, the duty cycle is limited in the range 0.30–0.44. The maximum value, 0.44, corresponds to the nominal lamp power (100 W), and the minimum value ($D_{min}$), 0.30, corresponds to 44% of the nominal power (44 W). With the presented methodology, a 56% lamp-power dimming has therefore been achieved.

The ZVS operation of the resonant inverter was shown in the detail shown in Fig. 8. The variation of the resonant-current phase angle is given by (7), and it is represented in Fig. 11 for the values of $C_S$, $L_S$, and $C_P$ in Table II and the lamp parameters shown in (1) and (2) and Table I.

Initially, with lamp power close to the nominal value, the resonant-current phase angle is nearly constant. However, for lower lamp power, the resonant tank behavior becomes more inductive. This behavior helps to maintain ZVS operation in switch $S_2$ even when reducing the duty cycle to dim the lamp.

With the results obtained from the previous design, a laboratory prototype was built. Fig. 12 shows lamp voltage and current waveforms during ignition. Voltage and current peaks of 1.66 kV and 3.36 A, respectively, were measured.

Fig. 13 shows the integrated switch ($S_{1.3}$) current waveform, which is characterized by overcurrent stress, and the integrated switch voltage waveform. The measured peak voltage and current and rms current in switch $S_{1.3}$ were 640 V, 4.32 A, and 1.682 A, respectively.

Fig. 14 shows the diode $D_1$ current waveform. As can be seen, this current goes to zero before the next switching period, proving DCM operation.

Fig. 15(a)–(f) shows the line and lamp voltages and current waveforms under dimming operation. As can be seen, the lamp power was varied from approximately 100 down to 46 W, which represents a total dimming range of 54%. It is important to point out that the output capacitance of the MOSFETs and the parasitic capacitances of the diodes used in the converter have an influence on the input-current waveforms in DCM operation.
These parasitic capacitances cause input-current distortion due to the effect of the high-frequency oscillations appearing during the idle interval after the conduction of diode $D_1$ [40]. The effect is more important due to the high switching frequency used in the converter (250 kHz). Nevertheless, in the present prototype, the distortion has been maintained to a minimum by careful selection of the MOSFET and diodes, so that they exhibit very low parasitic capacitances.

Fig. 16 shows the experimental measurements of the lamp power, input power, and efficiency under dimming operation. Fig. 17 shows the converter PF and input-current total harmonic distortion (THD) also under dimming operation. The implemented prototype presented, at nominal lamp power (100 W), a PF of 0.989, an input-current THD of 14.929%, and an efficiency of 87%. At minimum lamp power (46 W), it presented a PF of 0.993, an input-current THD of 11.972%, and an efficiency of 79%. The experimental results showed a complying with IEC 61000-3-2 Class C, as shown in Fig. 18.

Fig. 19 shows the EFL Icetron/Endura lamp under operation for nominal and minimum power levels as a result of duty cycle control.
VII. CONCLUSION

This paper has presented the SEPIC half-bridge integrated topology to feed an EFL. Initially, important characteristics of ELFs were presented, as well as its electric model, necessary for the design of the integrated converter. The proposed circuit was designed for DCM operation, so that the converter could be represented as an equivalent resistance. Thus, a high system PF was obtained, associated with a low THD, in order to optimize the energy drained from the ac line. The stages of operation were also presented. The SEPIC is designed in such a way that it does not necessitate the use of EMI filter. The integration of the PFC and PC stages reduced the system component count. However, the integrated switch should be designed so as to handle both efforts of circuit current and voltage. In spite of the stage integration, as well as high switching frequency required to supply the lamp and the absence of EMI filter, the experimental results validated the proposed topology. The topology achieved an efficiency ranging between 87% and 79% and input-current THD between 14.9% and 12%. This is considered adequate, taking into account that the converter operated at 250 kHz and was designed to provide dimming functionality.

REFERENCES


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