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Modeling and extraction of gate bias-dependent parasitic source and drain resistances in MOSFETs

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Abstract

Gate voltage-dependent parasitic source and drain resistances in MOSFETs have been modeled and extracted with a symmetric additional resistance method (sARM) for better description of asymmetric parasitic resistances which are induced by intentional and/or accidental variations in the layout and fabrication process. A good agreement of nonlinear models with the sARM has been verified with experimental data obtained from n-channel LDD MOSFETs.
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Keywords: MOSFET; Source resistance; Drain resistance; Nonlinear model; Parameter extraction

1. Introduction

Accurate modeling and extraction of characteristic model parameters in MOSFETs, especially bias-dependent parasitic source and drain resistances, is crucial to the simulation and implementation of high performance CMOS devices and integrated circuits [1]. In the modeling and extraction of parasitic source and drain resistances (R_S and R_D, respectively) in MOSFETs, there are difficulties in obtaining separated values of R_S and R_D due to the isolated gate. It is also well known that the electrical performance and reliability, including transconductance, saturated drain current, cut-off frequency, noise figure, and degradation due to hot carriers, depend more on R_S than R_D [2,3]. However, R_S and R_D have been usually assumed to be the same ($R_S = R_D$) [4–7] even though asymmetric lightly doped drain (LDD) structures are essential, in order to guarantee the robustness of MOSFETs against the hot-carriers, and result in nonequal R_S and R_D ($R_S \neq R_D$) [8–11]. Otherwise, complicated characterization process and/or high frequency scattering parameters are required with extra test structures for the extraction of separated R_S and R_D [8–13] Recently, we have reported an additional resistance method for extraction of separated nonlinear resistances under the assumption that R_S and R_D follow the same dependence on the gate bias (V_{GS}) [14].

In this paper, considering asymmetries caused by intentional and/or accidental layout and process variations, improved nonlinear models are reported for better description of V_{GS}-dependent R_S and R_D in MOSFETs. An improved symmetric additional resistance method (sARM) is also described for extraction of parasitic source and drain resistances in MOSFETs with a fixed external resistance (R_{ext}).

2. Nonlinear resistance models and sARM

There has been enormous effort on the nonlinear modeling and extraction of separated source and drain resistances in MOSFETs [5–14]. As one of useful works, Lou et al. [8] recently reported the drain-current-conductance method (DCCM) with nonlinear R_S and R_D modeled by

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$$R_{S,D}(V_{eff}) = R_{SO,DO} + \frac{1}{1 + \kappa_{S,D} V_{eff}^{m_{s,d}}}, \quad (1)$$

where $V_{eff} = V_{GS} - V_{TN}$, $R_{SO}(R_{DO})$ is the V_{GS}-independent source (drain) resistance; $\kappa_S(\kappa_D)$ and $m_s(m_d)$, the nonlinearity constants for source (drain) resistance; and V_{TN}, the threshold voltage of n-channel MOSFETs. However, the variation of V_{GS}-dependent component is extremely limited to *only* 1 Ω (i.e., $R_{SO,DO} < R_{S,D} < R_{SO,DO} + 1$) and, therefore, it is in lack of implementing experimental observations in parasitic resistances with the gate voltage over a wide range of variations in the fabrication process and layout of scaled MOSFETs. Recently we had also reported a nonlinear resistance model, with a unique ARM method, described by [14]

$$R_{S,D}(V_{eff}) = R_{SO,DO} + R_{Si,Di}(V_{eff}) = R_{SO,DO} + \frac{1}{\kappa_{S,D} V_{eff}}. \quad (2)$$

In the previous work, however, it was focused on the extraction method rather than the resistance models and is still in need of improved models for the V_{GS}-dependent R_S and R_D in MOSFETs with asymmetric layout and/or fabrication process.

In this work, improved V_{GS}-dependent nonlinear models for R_S and R_D are proposed and described as

$$R_S(V_{eff}) = R_{SO} + R_{Si}(V_{eff}) = R_{SO} + \frac{1}{\kappa_S V_{eff}^{m_s}}, \quad (3)$$

$$R_D(V_{eff}) = R_{DO} + R_{Di}(V_{eff}) = R_{DO} + \frac{1}{\kappa_D V_{eff}^{m_d}}, \quad (4)$$

respectively. We note that $R_{SO}(R_{DO})$ and $R_{Si}(R_{Di})$ are bias-independent part and V_{GS}-dependent of part in the source (drain) resistance, respectively. They are believed to be more effective and appropriate to MOSFETs with nonuniform and retrograde doping profiles over a wide range of variations in the modeling of V_{GS}-dependent resistances. These nonlinear models are flexible enough to accommodate variations of resistance values during the fabrication process and/or layout design of each device. V_{GS}-independent parasitic elements R_{SO} and R_{DO} model the contact resistances, the metallic interconnection resistances, and the external source/drain resistances in the heavily doped external source/drain regions. $\kappa_s(\kappa_d)$ and $m_s(m_d)$, on the other hand, describe nonlinear variations of $R_S(R_D)$ which are caused by the modulation of conductivity under the gate with V_{GS}. These elements are also very sensitive to the asymmetries in layout and process and detrimental to the performance and reliability of their integrated circuits whatever they are caused by intentional and/or accidental implementation [2,3]. Even though parasitic resistances are modulated by the drain voltage, V_{DS}-dependent variation of R_S ands R_D is not considered in this work because V_{DS}-dependent modulation of the current–voltage (I–V) characteristics are typically modeled by the channel length modulation parameter $\lambda(I_D = I_{DO}(1 + \lambda V_{DS})$ under a high drain voltage.

In the extraction of characteristic model parameters in MOSFETs, including separated V_{GS}-dependent R_S and R_D in the proposed nonlinear resistance models, we used a sARM. The sARM method, applied to MOSFETs under linear mode of operation with a small drain voltage (V_{DS}) as schematically described in Fig. 1, uses a fixed and identical value of the external resistance R_{ext} while arbitrary values have been used in the previous ARM method with nonlinear resistance models [14]. By using the sARM method with a large identical value of R_{ext}, device equations and parameter extraction process can be significantly simplified with more accurate values during a nonlinear fitting process.

In the linear mode of operation under a small drain voltage to the MOSFETs, the I–V characteristics of MOSFETs, including voltage drops across the parasitic source and drain resistances, can be described by

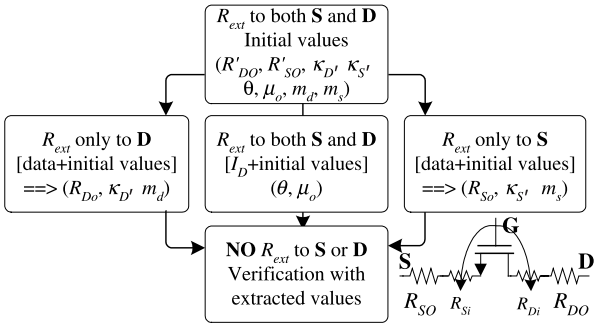

Fig. 1. Schematic diagram of the sARM method for nonlinear modeling and extraction of parasitic source and drain resistances in MOSFETs.

$$I_D = \frac{K}{1+\theta(V_{eff}-I_D R_S)}\left\{V_{eff}-\frac{1}{2}(V_{DS}-I_D(R_D+R_S))\right\} \times \{V_{DS}-I_D(R_D+R_S)\}. \quad (5)$$

Combining the proposed R_S and R_D models with the sARM method as an extraction method schematically described in Fig. 1, we obtain an analytical result for the total resistance R_T for each case of measurement with external resistance R_{ext},

$$R_T = R_D + R_S + \frac{1+\theta(V_{eff}-I_D R_S)}{K[V_{eff}-0.5V_{DS}+I_D(R_D+R_S)]}, \quad (6)$$

where $K = \mu_0 C_{ox} W/L_{eff}$, $L_{eff} = L - \Delta L$ with I_D, the drain current; C_{ox}, the oxide capacitance per unit area; μ_0, the low-field mobility; W, the gate width; L, the gate length; and ΔL, the channel length reduction. This result is used for the extraction of model parameters in R_S, R_D, and effective mobility (μ_{eff}) of channel carriers. For accurate extraction of the effective mobility in the channel, we also included a voltage drop across the parasitic source resistance R_S in the model as

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-I_D R_S - V_{TN})}, \quad (7)$$

with θ as a mobility degradation factor due to the transversal electrical field.

We finally obtain analytical results, which will be used in the sARM extraction method, for I_D, R_D, R_S, and μ_{eff} as described by

$$I_D = \{-B - \sqrt{B^2-4AC}\}/2A, \quad (8)$$

$$R_D = \{-E + \sqrt{E^2-4DF}\}/2D, \quad (9)$$

$$R_S = \{-H - \sqrt{H^2-4GI}\}/2G, \quad (10)$$

$$\mu_{eff} = \frac{I_D}{\frac{C_{ox}W}{L_{eff}}[V_{eff}-\{V_{DS}-I_D(R_D+R_S)\}/2][V_{DS}-I_D(R_D+R_S)]}, \quad (11)$$

where

$$A = \theta R_S - K(R_D+R_S)(R_D-R_S)/2,$$

$$B = -[1+\theta V_{eff}+K(R_D+R_S)(V_{eff}-V_{DS}/2) - K(R_D+R_S)/2], \quad (12)$$

$$C = K(V_{eff}-V_{DS}/2)V_{DS}, \quad (13)$$

$$D = G = KI_D^2/2, \quad (14)$$

$$E = KI_D[(V_{eff}-(V_{DS}+I_D R_S)/2)-(V_{DS}-I_D R_S)/2], \quad (15)$$

$$F = I_D[1+\theta(V_{eff}-I_D R_S)] - K[V_{eff}-(V_{DS}+I_D R_S)/2] \times (V_{DS}-I_D R_S), \quad (16)$$

$$H = \theta I_D^2 - KI_D[\{V_{eff}-(V_{DS}-I_D R_S)/2\} + (V_{DS}-I_D R_S)/2], \quad (17)$$

and

$$I = K[V_{eff}-(V_{DS}-I_D R_S)/2](V_{DS}-I_D R_S) - I_D(1+\theta V_{eff}). \quad (18)$$

3. Experimental results

With a procedure schematically described in Fig. 1(a) with above analytical relations, the I–V characteristics of MOSFETs are obtained with four different probing configurations of R_{ext} (fixed to $R_{ext} = 993\ \Omega$ in this work); (A) R_{ext} to both the source and drain, (B) R_{ext} only to the source, (C) R_{ext} only to the drain, and (D) no R_{ext} to the source or drain. Coarse values of model parameters are primarily obtained from the experimental data with R_{ext} to both source and drain terminals. These are used as initial values for the extraction of final values with a nonlinear fitting process combining measured I–V data from four different probing conditions.

We applied the nonlinear R_S and R_D models with the sARM method to n-channel LDD MOSFETs ($W/L = 30$ μm/0.6 μm; $V_{TN} = 0.41$ V, 30 μm/1.0 μm; $V_{TN} = 0.69$ V) which have lightly doped source and drain regions. The linear extraction method by Lee et al. [15] and the channel resistance method [4] have been used for the extraction of V_{TN} and L_{eff}, respectively. With the measured data from MOSFETs on wafer with identical large external resistances ($R_{ext} \gg R_S$, R_D) to both source and drain as described in Fig. 1(a), a total resistance R_T for the sARM can be simplified into

$$R_T = (R_{ext}+R_D)+(R_{ext}+R_S) + \frac{1+\theta[V_{eff}-I_D(R_{ext}+R_{SO}+\kappa_S V_{eff}^{-m_s})]}{K(V_{eff}-V_{DS}/2)}, \quad (19)$$

and we obtain *initial* values (R'_{SO}/R'_{DO}, κ'_S/κ'_D, m'_s/m'_d, θ', μ'_0) for nonlinear least square fit process.

Combining initial values obtained from the measurement configuration A with data from the configuration B, we obtain R_S while R_D is obtained from the combination of A and D. We also obtain μ_{eff}, as a function of V_{GS}, from the combination of B, C, and D with a nonlinear fitting process. Through a nonlinear least square fit combining *initial* values and experimental data for three-other configurations with fixed R_{ext} ($= 993\ \Omega$), we obtained V_{GS}-dependent R_S and R_D for MOSFETs with $L = 0.6$ and 1.0 μm as shown in Fig. 2. A good

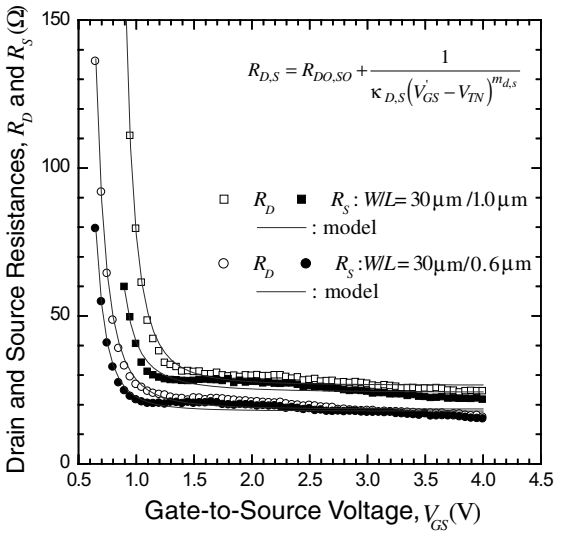

Fig. 2. V_{GS}-dependent R_D and R_S in n-channel LDD MOSFETs ($L = 0.6$ and 1.0 μm) extracted by the sARM method with new nonlinear models for R_D and R_S.

agreement of extracted data with new nonlinear models has been obtained for all of the DUTs. Extracted model parameters in V_{GS}-dependent R_S and R_D models are also summarized in Table 1. We note that, even for MOSFET structures with LDD regions in both source and drain, R_{DO} is larger than R_{SO} mainly due to asymmetry caused by layout, process, and possibly expanded depletion of the LDD region in the drain. Significant asymmetries have been observed in the nonlinear model parameters ($\kappa_D - \kappa_S$ and $m_d - m_s$) for each device due to similar reasons.

Large differences in the model parameters of MOSFETs with $L = 0.6$ and 1.0 μm are also observed due to asymmetries in layout and process variations as well as short channel effects. Compared with model parameters in the drain resistance (R_{DO}, m_d, κ_d), as shown in Table 1 with $V'_{GS} \equiv V_{GS} - I_D R_S$, there is a strong dependence of model parameters of the source resistance (R_{SO}, m_s, κ_s) on the gate length. We also note that R_{SO} in the source resistance model is very close to R_{DO} in the drain resistance model for each case of gate length ($R_{SO}/R_{DO} = 17.85\ \Omega/18.48\ \Omega|_{0.6\ \mu m}$ and $24.09\ \Omega/26.57\ \Omega|_{1.0\ \mu m}$) contrary to significant differences in the nonlinear part

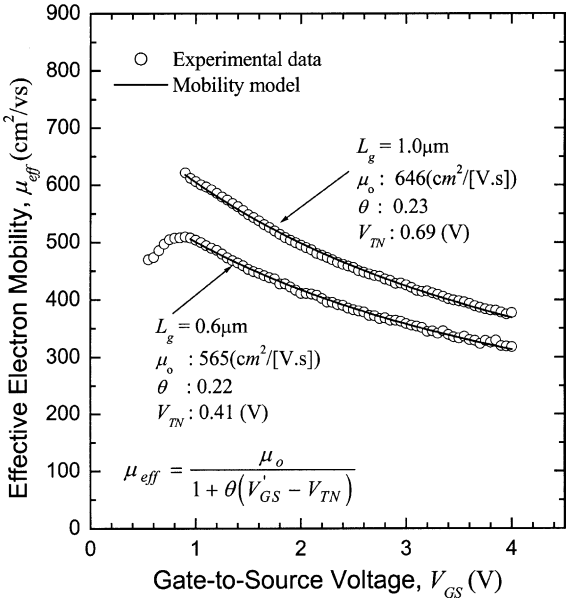

Fig. 3. Effective mobility (μ_{eff}) in n-channel LDD MOSFETs ($L = 0.6$ and 1.0 μm) extracted by the sARM method considering the voltage drop across R_S.

Table 1
Extracted model parameters for nonlinear parasitic R_S and R_D in MOSFETs

Model parameters		Gate: W/L	
		30 μm/0.6 μm	30 μm/1.0 μm
Intrinsic parameters	V_{TN} (V)	0.41	0.69
	C_{ox} (F/cm^2)	0.15×10^{-6}	0.15×10^{-6}
	t_{ox} (nm)	23	23
	ΔL (μm)	0.28	0.28
$\mu_{eff} = \frac{\mu_0}{1 + \theta(V'_{GS} - V_{TN})}$	μ_0 (cm^2/[V · s])	565	646
	θ (1 V^{-1})	0.22	0.23
$R_D(V_{GS}) = R_{DO} + \frac{1}{\kappa_D(V_{GS} - V_{TN})^{m_d}}$	$R_{DO}(\Omega)$	18.48	26.57
	κ_D	0.43	0.42
	m_d	2.75	2.61
$R_S(V_{GS}) = R_{SO} + \frac{1}{\kappa_S(V_{GS} - V_{TN})^{m_s}}$	$R_{SO}(\Omega)$	17.85	24.09
	κ_S	0.94	0.49
	m_s	2.84	1.82

($m_s/m_d = 2.84/2.75|_{0.6\ \mu m}$ and $1.82/2.61|_{1.0\ \mu m}$, $\kappa_s/\kappa_d = 0.94/0.43|_{0.6\ \mu m}$ and $0.49/0.42|_{1.0\ \mu m}$) of the resistances. This means that the extrinsic part of the R_S and R_D in a specific gate length is symmetric because they come mainly from the contact, interconnection, and external resistances in the heavily doped n^+ regions which are predominantly governed by the fabrication process. Nonlinear part of the model parameters, on the other hand, depends on the gate length because the effective gate voltage ($V_{eff} = V_{GS} - V_{TN}$) and resultant modulation of the conductive layers in the source and drain regions are significantly different for MOSFETs with different gate length. This results in considerable discrepancies in the nonlinear model parameters. This is also more significant in the nonlinear part of the source resistances because a modulation of the space charge region into the channel region is modeled as a channel length reduction (λ).

We also verified a good agreement (Fig. 3) of measured data with extracted model parameters considering the voltage drop across the R_S. As shown in Fig. 3 and Table 1, there are differences in the low-field mobility (μ_0) and V_{GS}-dependence in each MOSFET with a different gate length. A discrepancy (~12%) in the low-field mobility ($\mu_0 = 565|_{0.6\ \mu m}$ vs. $646|_{1.0\ \mu m}$) is probably induced by the nonuniform distribution of device characteristics by either fabrication process or physical layout. A difference in the field-dependent mobility vs. V_{GS} plots in Fig. 3 comes mainly due to a different effective electric field established by the different gate length for the same gate voltage. Comparing experimental I_D–V_{GS} characteristics with data generated by extracted model parameters, we confirmed the validity of the new nonlinear resistance models with the sARM method. As shown in Fig. 4(a) and (b), a good agreement has been also obtained over a full range of the measured drain current in MOSFETs with $W/L = 30$ μm/0.6 μm (Fig. 4(a)) and 30 μm/1.0 μm (Fig. 4(b)).

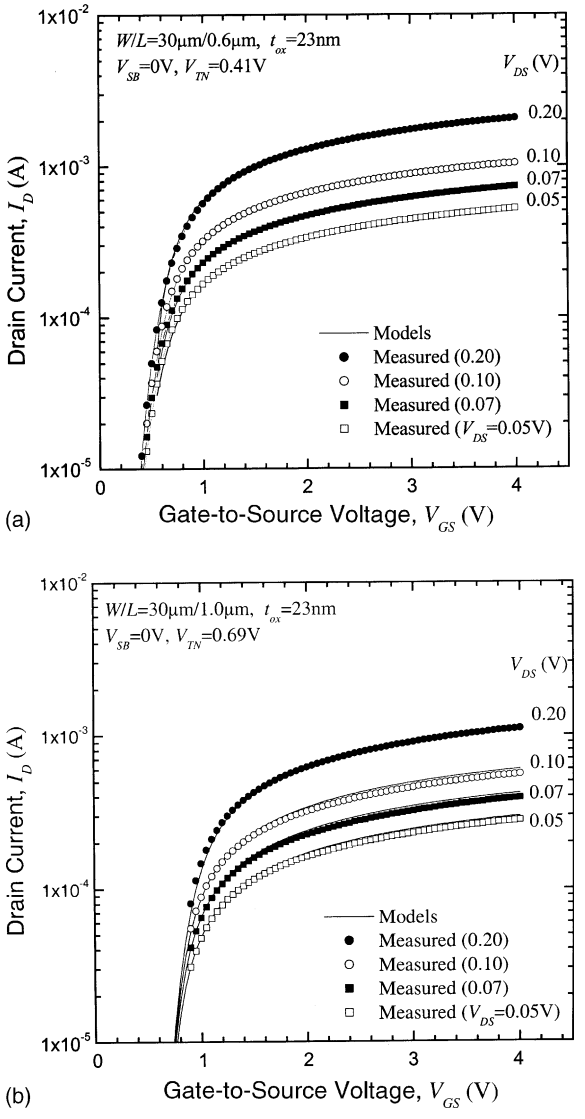

Fig. 4. Verification of the sARM method with V_{GS}-dependent R_D and R_S models for I_D–V_{GS} characteristics in n-channel LDD MOSFETs. (a) $W/L = 30$ μm/0.6 μm and (b) $W/L = 30$ μm/1.0 μm.

4. Conclusion

New nonlinear models with an improved extraction method have been reported for accurate modeling and extraction of V_{GS}-dependent parasitic source and drain resistances R_S and R_D. Nonlinear characteristics of R_S and R_D were independently modeled for better description of asymmetries caused by the layout and fabrication process. A good agreement has been verified with experimental data from n-channel LDD MOSFETs.

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