Design and Reliability of a New WL-CSP

*Li Wetz, Beth Keser, and Jerry White
Motorola SPS
2100 E. Elliot Road, MD EL 606
Tempe, AZ, USA 85284
Li.Wetz@motorola.com
Phone: (480) 413-8022
Fax: (480) 413-3608

Abstract

A new wafer level package has been designed and fabricated in which the entire package can be constructed at the wafer level using batch processing. Peripheral bondpads are redistributed from the die periphery to an area array using a redistribution metal of sputtered aluminum or electroplated copper and a redistribution dielectric. Redistribution of metal at the wafer level aids in eliminating the use of an interposer, or substrate. The redistributed bondpads are plated with the underbump metallurgy and then bumped using solder ball placement. The solder balls are reflowed onto the wafer creating a large standoff that improves reliability. This wafer level chip-scale package (WL-CSP) technology has been evaluated using a test vehicle, which has a 0.5 mm pitch of an 8 x 8 array of bumps on a 5 x 5 mm^2 die. The bump structure and package geometry have been optimized using simulation and validated by experimentation. The board used for reliability testing is a 1.2 mm thick, 2-layer FR-4 board with non-soldermask defined landpads with OSP (organic solderability preservative). The landpads are the same diameter as the redistributed bondpads. Package and board level reliability data will be presented.

Keywords: WL-CSP, wafer level chip scale package, solder ball attach, solder joint reliability, Motorola

Introduction

Wafer-level packaging is becoming a very popular method of packaging low to mid-I/O devices for several reasons: cost, size, and ease of testing. Cost is the largest force driving wafer-level packaging. Using batch processing, an entire wafer can be packaged instead of packaging each singulated die. Wafer level packaging reduces packaging steps, eliminates the use of underfill, and allows for centralized processing in the fab. Also, packaging the wafer allows for a high degree of process integration due to the use of fab-type processing such as thin films and lithography which decreases cost. Centralized packaging in the fab also reduces packaging time and inventory, since devices no longer have to be packaged separately between the fab and the assembly houses. Size is also a driving force for wafer-level packaging. The footprint of a WL-CSP is the same as the die. Wafer-level burn-in and test (WLBT) is also driving the industry toward WL-CSP solutions. Test will no longer be necessary before packaging. A completely packaged wafer can be burned-in and tested after the final packaging step resulting in known good packages (KGP). Testing at the wafer level can reduce test costs by as much as 50%, requires less test capital, and reduces the number of test steps.

One approach to WL-CSP technology is a redistributed ball technology where solder balls are placed at wafer level to form first and second level interconnect. Fraunhofer IZM has done initial studies on this WL-CSP structure using stencil printed bumps [1]. In this study, stencil printed bumps are replaced with direct ball placement to increase bump height. This technology has been described elsewhere, but for the first time; board level reliability data will be presented [2-4].

Target Applications

WL-CSP solutions are blossoming due to the increase in market demand for packages with small footprints. BPA Consulting Ltd. reported 20 million WL-CSPs were sold in 1999 [5]. The devices packaged were primarily flash EEPROM as well as RF, discretes, and SRAM.

In 2004, the market is expected to increase 20 times dominated primarily by flash EEPROM and high speed DRAM. In 1999, WL-CSPs were primarily used in cell phones, but in 2004 other end-use applications will include memory modules, PDA's, laptops, digital camcorders, and digital cameras. By 2004, 217.3 million units of WL-CSPs will be used in cell phones, compared to 16.6 million in 1999. The number of WL-CSPs used in memory

modules will increase from 2 million in 1999 to 82 million in 2004. The growth of WL-CSP use in digital cameras, digital camcorders, PDAs and notebook computers will account for an additional 110 million units.

Prismark Partners LLC forecasts that the WL-CSP market, including integrated passives, will increase to 3.5 billion die in 2005 [6]. This includes approximately 2.5 billion integrated passives. The remaining 1 billion die will be comprised of discretes/analog, logic/ASIC/MCU, low-end memory and performance memory.

Test Vehicle

The test vehicle used for this study was a 5 x 5 mm^2 die with an 8 x 8 array of bumps at a 0.5 mm pitch. There were 496 die packaged on a six-inch wafer. Photographs of the diced WL-CSP are shown in Figures 1 and 2. The preformed balls are eutectic Sn-36Pb-2Ag, Sn-0.7Cu, or Sn-4Ag-0.5Cu with a 300 µm diameter. The redistribution metal was sputtered aluminum with 300 µm redistributed bondpads. The BCB redistribution dielectric was 5 µm thick and had 250 µm diameter openings to the bondpads. The redistribution process has been described previously [7]. 300 µm balls were used to give the maximum bump height for the given 0.5 mm pitch. Figure 3 shows a cross-section of a WL-CSP. The bump height of the WL-CSP is 230 µm and the bump diameter is 320 µm.

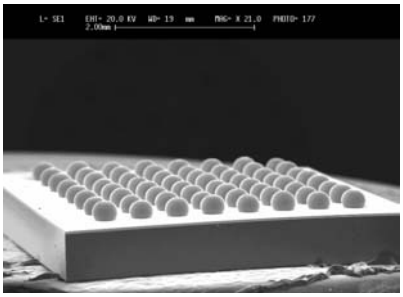

Figure 1: Tilt view of Motorola's WL-CSP.

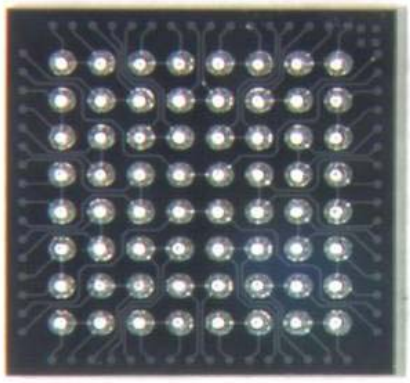

Figure 2: Top view of Motorola's WL-CSP.

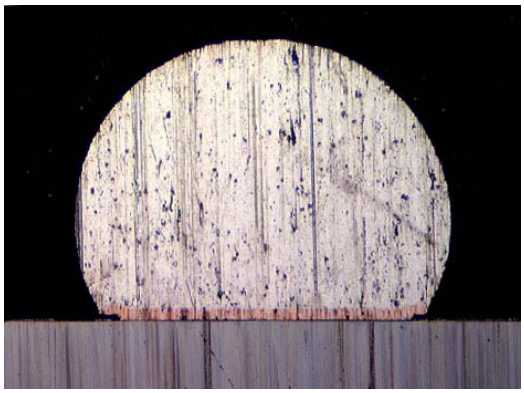

Figure 3: Cross-section of the SnPbAg WL-CSP.

Package Level Reliability

WL-CSPs with SnPbAg and SnCu interconnects were preconditioned at JEDEC MSL1 and MSL3 with reflows of 240°C and subjected to several types of accelerated life testing to predict their reliability. When the resistance of a package increased to 50% above its initial value, the part was considered a failure. All packages were tested using a probe card that placed two probes on each bump and thus was able to provide excellent accuracy and precision in resistance measurements. A cross-section of the WL-CSP package is shown in Figure 3. The ball height and width is 200 µm and 320 µm, respectively. The packages were subjected to liquid-to-liquid thermal shock (LLTS), which cycled parts from –55 to 125°C with a dwell time of 10 minutes and a ramp time of less than 10 seconds; air-to-air thermal shock (AATS), which cycled parts from –55 to 125°C with a dwell time of 5 minutes and a ramp time of 10 seconds; air-to-air thermal cycles (AATC) from –40 to 125°C and 0 to 100°C at a rate of 1 cycle/40 minutes (10 minute ramp and 10 minute dwell); high temperature storage (HTS, 125°C); and autoclave (121°C, 100%RH, 2 atm). The package level reliability was excellent. The results are shown in Table 1. Most testing was stopped before failure. The SnPbAg WL-CSP that was preconditioned at MSL3 had one failure after 2900 cycles LLTS. The WL-CSP packages fulfill the package level reliability requirements for commercial, industrial, and automotive uses.

Table 1. Package level reliability results.

WL-CSP	SnPbAg		SnCu	
Package Level Reliaibility	MSL1/240°C	MSL3/240°C	MSL1/240°C	MSL3/240°C
LLTS -55/125°C 10 min dwell/1 min ramp	>3000 cycles	2900	>3000 cycles	>3000 cycles
AATC 0/100°C 10 min dwell/10 min ramp	>2200 cycles	>2200 cycles	>2200 cycles	>2200 cycles
AATC -40/125°C 15 min dwell/10 min ramp	>2000 cycles	>2000 cycles	>2000 cycles	>2000 cycles
HTS 150°C	>2200 cycles	>2200 cycles	>2200 cycles	>2200 cycles
Autoclave 121°C, 100% RH, 2 atm	>336 hrs	>336 hrs	>336 hrs	>336 hrs

Board Level Reliability

WL-CSPs were attached to boards and subjected to accelerated life tests to determine their reliability. Board attach was performed on SnPbAg WL-CSPs assembled with both flux and SnPbAg solder paste. The data represents the flux-assembled samples, however, there was little difference in reliability for between the two. SnCu WL-CSPs were assembled with flux, and SnAgCu were assembled with SnAgCu solder paste. The boards were 2-layer FR-4, single-sided, conventional copper laminated core construction with OSP, and non-soldermask defined pad openings that were 100 µm greater than the 250 µm test pads. The board thickness was 1.2 mm. A cross-section of the WL-CSP attached to the board is shown in Figure 4. The standoff height between board and die is approximately 192 µm and the bump diameter is 317 µm.

Board level reliability for LLTS (-55/125°C), AATC (0/100°C), AATC (-45/125°C), and THB (85°C with 85% relative humidity and 5V bias) were performed. The boards were tested for failure every 100 cycles for LLTS and AATC cycling. Packages in THB were tested every 168 hours. Resistance levels determined failure criteria. When the resistance of a package increased to 50% above its initial value, the part was considered a failure. Where applicable, Weibull plots were generated to determine the characteristic reliability of each solder. Board level reliability results can be found in Table 2.

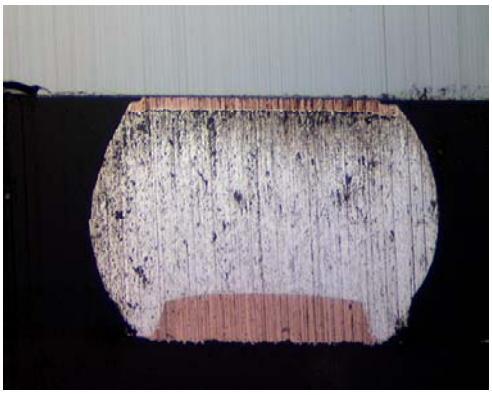

Figure 4: Cross-section of the WL-CSP attached to the board.

Table 2: Board level reliability results.

	Cycles to First Failure		
	SnPbAg	SnCu	SnAgCu
LLTS	1300	500	700
0/100°C AATC	2100	2500	3100
-40/125°C AATC	1400	1400	1900
THB	0 fails @ 1008 hrs		

Figure 5 is a Weibull plot showing the characteristic life of each package type. The characteristic life is defined as the age at which 63.2% of the units have failed. The Weibull plot assumes a single failure mode for all samples. SnPbAg packages had time to first failure at 1300 cycles and a characteristic life of 2083 cycles. SnCu packages had first fail at 500 cycles with a characteristic life of 1236. SnAgCu had first failure at 700 cycles with a characteristic life of 2091 cycles. The dominant failure mode for all alloys was solder cracking. Cross-sections can be seen in Figure 6.

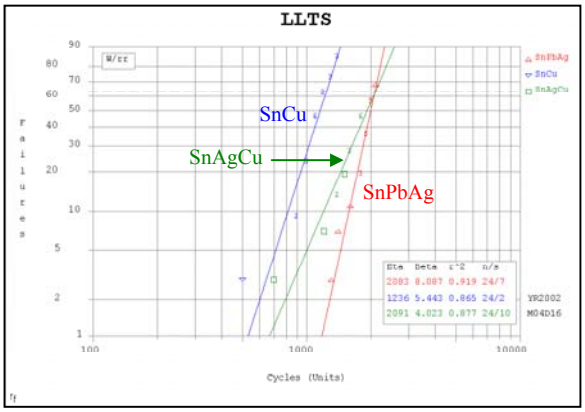

Figure 5: Weibull of LLTS reliability results.

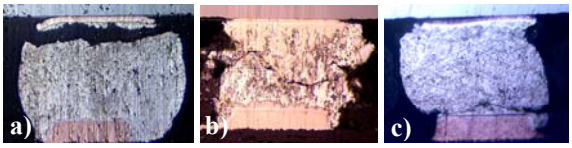

Figure 6: Cross-sections of WL-CSPs after LLTS reliability testing: (a) SnPbAg after 1500 cycles, (b) SnCu after 1300 cycles, (c) SnAgCu after 700 cycles. Failure mode was solder cracking in all cases.

Figure 7 shows a Weibull plot of the SnPbAg reliability data for 0/100°C AATC. The characteristic life for SnPbAg is 2754 with the first failure occurring at 2100 cycles. The other two alloys are not plotted due to the lack of failures. SnCu had first failure at 2500 cycles; SnAgCu had first failure at 3100 cycles. Both Pb-free alloys had only two failures before the reliability test was concluded. The dominant failure mode for SnPbAg parts, as well as for the limited number of failed SnCu and SnAgCu parts, was solder cracking, as seen in Figure 8.

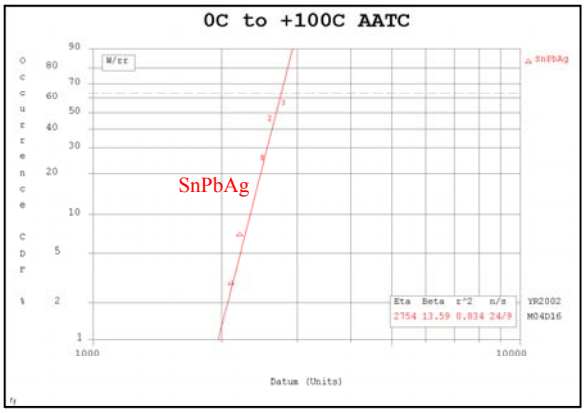

Figure 7: Weibull of 0/100°C AATC reliability results.

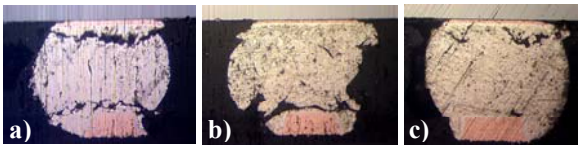

Figure 8: Cross-sections of WL-CSPs after 0/100°C AATC reliability testing: (a) SnPbAg after 2000 cycles, (b) SnCu after 3300 cycles, (c) SnAgCu after 2800 cycles. Failure mode was solder cracking in all cases.

Figure 9 is a Weibull plot of –40/125°C AATC. SnPbAg packages had time to first failure at 1400 cycles with a characteristic life of 2696 cycles. SnCu packages had first failure at 1400 cycles with a characteristic life of 1923 cycles. The characteristic life for SnAgCu is 2638 with the first failure occurring at 1900 cycles. The dominant failure mode for all alloys was solder cracking. Cross-sections can be seen in Figure 10.

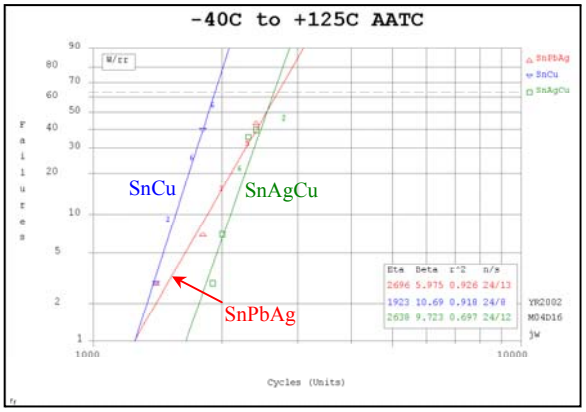

Figure 9: Weibull of -40/125°C AATC reliability results.

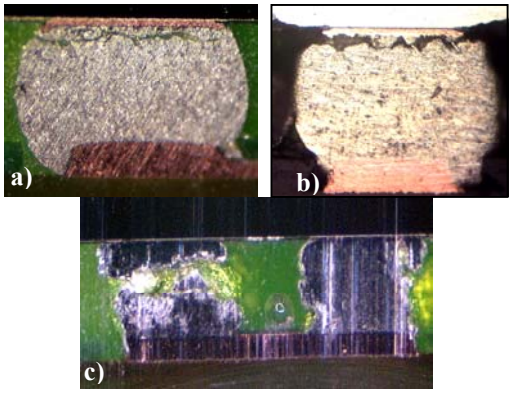

Figure 10: Cross-sections of WL-CSPs after –40/125°C AATC reliability testing: (a) SnPbAg after 1000 cycles, (b) SnCu after 1900 cycles, (c) SnAgCu after 700 cycles. Failure mode was solder cracking for all cases.

WL-CSP –40/125°C AATC reliability was compared to a commercially available WL-CSP with protection around the solder ball. Both test vehicles utilized test die with 0.3 mm solder balls at a 0.5 mm pitch; the other's DNP (distance to neutral point) is 3.18 mm [8], Motorola's DNP is 3.54 mm. Both used 2-layer FR-4 boards with non-soldermask defined (NSMD) bondpads coated with OSP. Motorola's board thickness is 1.2 mm while the other's is 1.57 mm. They reported a characteristic life of 993 cycles while Motorola achieved a characteristic life of 2696 cycles. Motorola's WL-CSP resulted in far better reliability even though the die size is slightly larger and the board is thinner.

Summary

Wafer level packaging technology simplifies processing and reduces cost by eliminating substrate and underfill. Using preformed balls results in a large overall collapse height, which meets solder joint reliability requirements for commercial applications.

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