Multimedia Data Processing Elements for Digital TV and Multimedia Services in Home Server Platform

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Abstract — This paper describes the design and implementation of multimedia data processing elements for a home server platform. Generally, a home server can be considered as an integrated form of a multimedia data server, home control server, and home information server. As a multimedia data server, the proposed scheme has a digital TV receiver module and a multimedia codec module. Thus, watching digital TV and remote multimedia services are available in this platform. In addition, an error resilient scheme using digital watermarking is implemented to correct transmission errors in a noisy channel.

Index Terms — Digital TV, home networks, home server, multimedia, watermark.

I. INTRODUCTION

According to the newly developed digital information appliances and various kinds of wired and wireless home network standards such as HomePNA, IEEE1394, PLC, WirelessLAN, and etc., the concept and importance of a home server platform become more and more prominent. Although there are lots of opinions about the definition of the home server, we consider it as an integrated form of a multimedia data server, home control server, and home information server in a box [1]-[3]. The infrastructure for high-speed transmission of large size data has been constructed because of rapid spread of high-speed access networks such as xDSL as well as high-speed home networks. Moreover, as DVD players and titles are spreading widely and digital TV (D-TV) broadcast has begun, the importance of a home server platform, as a multimedia data server begins to attract considerable attention. This paper proposes the architecture of the multimedia data processing elements in the home server for watching D-TV and remote multimedia services.

The home server platform, as a multimedia data server, is responsible for storage, management, and distribution of the multimedia data with huge size of storage devices. Users can enjoy lots of multimedia services using a home server platform, for example, appreciating DVD titles, watching D-TV, and remote multimedia services. In addition, a home server can record a D-TV program, and transfer multimedia data to a remote client. The architecture of the home server platform is illustrated in Fig. 1, which can be divided into three groups of hardware devices, software modules, and contents and services. First, hardware devices in the home server consist of several home network devices, a D-TV receiver, and a multimedia codec module. Second, the software modules are categorized into system software and middleware. The system software includes a real time operating system (RTOS) for the home server, Java Virtual Machine (JVM), and open service gateway initiative (OSGi) framework. The middleware consists of the agent software, OSGi service bundles, and the control /multimedia middleware [4]. Finally, contents and services such as D-TV, remote medical services, remote education, and cyber home are available on this basis.

Fig. 1. Architecture of the home server platform

This paper describes the definition, design, and implementation of multimedia data processing functions for a home server as a multimedia data server. Section 2 defines multimedia data processing functions for a home server, and Section 3 describes the architecture of a D-TV receiver. A multimedia codec module for a home server is discussed in Section 4, and implementation results are presented in Section 5. Finally, conclusions and future works are discussed in Section 6.

II. MULTIMEDIA FUNCTIONS IN HOME SERVER

Various kinds of multimedia services are available in a home server. However, this paper considers the three most essential multimedia services: a DVD player, a D-TV receiver, and a remote multimedia service. First, a DVD player employs a software player using computing power of the home server processor itself. Second, a D-TV receiver uses a hardware module attached to the home server platform. Finally, a remote
multimedia service transforms D-TV contents to a low bit rate multimedia stream using a multimedia codec module, and transfers the stream to a remote client. Thus, the home server platform has two hardware modules including a D-TV receiver module and a multimedia codec module for processing the multimedia data. The home server platform can support multimedia applications based on these two hardware modules.

Fig. 2. Multimedia data processing modules in home server

The architecture of multimedia data processing modules for D-TV and remote multimedia services in the home server is shown in Fig. 2. The D-TV receiver module can receive Advanced Television Systems Committee (ATSC) broadcast signal and display it on a HDTV by decoding MPEG-2 data. In addition, the D-TV receiver can send VGA size (640x480 pixels/frame) video image to the multimedia codec module (H.263 encoder) via VIP port. The multimedia codec module reduces the resolution of the video data to common intermediate format (CIF) size (352x288 pixels/frame) using bilinear interpolation, encodes the video data to a H.263 stream [5]-[7], and sends it to a network device in the home server. Either video in port or VIP port can be used to the video source for the multimedia codec module.

III. D-TV RECEIVER MODULE

The block diagram of a D-TV receiver module for the home server platform is shown in Fig. 3. The D-TV receiver module decodes the received D-TV broadcast signal using a tuner, an IF demodulator, an ADC, a VSB demodulator, and an MPEG decoder. HD size video data can be displayed on a HDTV through the video mux, which is employed to multiplex decoded video data and VGA (RGB) signal from the graphics module in the home server main board. Simultaneously, the D-TV receiver module can transmit VGA size video data to the multimedia codec module using VIP port. Besides, the D-TV receiver can process additionally transmitted data broadcast as well as high definition video. Especially, the D-TV receiver supports ATSC A/65 program and system information protocol (PSIP) standard for handling the electronic program guide (EPG). Therefore, users can utilize user-friendly information such as registered recording.

IV. MULTIMEDIA CODEC MODULE

The multimedia codec module receives video data from either video in port or VIP port. While the video data is downsized and encoded to an H.263 stream, an error resilient scheme is implemented to reduce the noise effects in the transmission channel. This section discusses the hardware description of the multimedia codec module and the error resilient scheme for H.263 encoder and decoder.

The multimedia codec module performs down sampling of input video using bilinear interpolation. A VGA size input image is converted into a CIF size image. In order to support remote multimedia service, the multimedia codec for a home sever should process at least 15 frames per second for CIF size video. The home server has to support various application services for multiple users as well as multimedia data processing. Thus, it is difficult to expect adequate quality of service (QoS), if the main processor of the home server is responsible for all of the multimedia codec functions. The proposed multimedia codec module makes use of a hardware module using a DSP and a field programmable gate array (FPGA) so as to reduce the load on the main processor and to support the required codec performance continually. Whereas the most parts of the codec algorithm are implemented in a DSP, motion estimation (ME) and motion compensation (MC) parts that require lots of computing time operate in a FPGA.

A. Hardware Description

The block diagram of the multimedia codec module using a DSP and a FPGA is shown in Fig. 4. The codec module consists of an analog control module and a digital control module. The analog control module manages input and output of video data, and the digital control module is responsible for encoding input video data using the DSP and the FPGA. In the codec module, the DSP controls the operation of the total codec module and outputs encoded video stream to PCI bus.

The architecture and data flow of the video input and output system using a DSP is illustrated in Fig. 5. The video input flow in Fig. 5 (a) shows the process for writing video signal to system memory of the DSP. First, the input video signal from either video in port or VIP port is stored in the frame buffer. If
the video source is video in port, the composite video signal from the video in port is transformed into \( Y \), \( C_b \), and \( C_r \) data using the video decoder. Second, the event-interrupt generator sends the read access ready interrupt signal to the DSP. Finally, the DSP requests DMA, and the DMA controller loads video data from the frame buffer to the system memory of the DSP. Fig. 5 (b) shows the process for video output. The DMA controller directly transfers video data stored in the DSP system memory to the display buffer. The video encoder transforms the video data of \( Y \), \( C_b \), and \( C_r \) to the analog video signal and outputs to a display device.

Fig. 4. Block diagram of multimedia codec module

Fig. 5. Architecture and flow of the video input and output in multimedia codec

The constitution of motion estimation and compensation module implemented in the FPGA is represented in Fig. 6. Inside the FPGA, there are two kinds of buses such as a system bus and an internal bus, and these buses are connected to the external system bus by a multiplexer. Data for current frame, previous frame, reconstruction frame, and motion vectors can interface with the DSP via the system memory. Simple nearest-neighbor search method based on TMN8 [7] is implemented on the FPGA.

Fig. 6. Block diagram of the FPGA module

B. Error resilient codec scheme

The multimedia codec resizes an input image with VGA size to a CIF size image, and encodes this CIF size image
using an H.263 encoder. The user can receive and play an H.263 stream in the remote client. Multimedia data can be easily corrupted by channel noise during the transmission process, and as a result the degradation of the image quality in the receiver becomes serious. In this paper, the information for detecting transmission error is embedded into block based DCT coefficients and motion vectors using an information hiding technique. As the transmission errors are found using the embedded data, the video quality can be improved by correcting errors in the receiver. The previous transmission error detection methods using the information hiding technique can only detect the location of error blocks and assist to correct transmission errors [8], [9]. However, the proposed method can claim intellectual property rights (IPR) for multimedia data besides an error resilient scheme, because it does not embed simple parity bits to detect transmission errors. In the proposed scheme, the embedded signal is generated from IPR information. The IPR information is transformed into watermark signal by encoding it using a convolutional encoder, and the watermark signal is embedded into every macro block in a frame during the video encoding process [10], [11]. The bit rate of the watermark signal is greater than that of IPR information because of the convolutional encoding process. However, the watermark signal does not increase the bit rate of the encoded video stream, and does not violate video encoding standards.

1) Video encoder

In the video encoding and information embedding step, while input video data is encoded using a block based encoding method, information for detecting transmission errors and claiming IPR for the multimedia data is embedded into the encoded stream. As shown in Fig. 7, video data is basically encoded using an H.263 encoding scheme, except for convolutional coding, interleaving, and data embedding steps.

![Fig. 7. H.263 encoding process using information hiding](image)

The watermark signal (W), which can be used to detect transmission errors, is obtained from IPR information (I) by using the convolutional encoder like the one shown in Fig. 8. The convolutional encoder outputs the encoded codewords by the operation of generator polynomials, when the original data is sequentially input to the shift registers [12]. In convolutional coding, the number of generator polynomials determines the amount of additional information. The generator polynomials used for making the codewords are

\[ g_1(x) = 1 + x + x^2 + x^4 \]

\[ g_2(x) = 1 + x^3 + x^4. \]

Because the convolutional encoder has two generator polynomials and its constraint length is 5, an m-bit data stream is transformed into 2(m+4)-bit convolutionally encoded data. This paper uses ASCII codes of 5 arbitrary characters as IPR information. Thus, the length of the input data stream m is 5 × 8–40 bits, and the number of bits in the encoded data is 2(m+4)=88 bits.

![Fig. 8. Convolutional encoder (rate = 1/2)](image)

The convolutional code can effectively correct random errors, but it is incapable of correcting errors concentrated in a specific region. If the errors are concentrated in a restricted region during the video transmission process, they can hardly be corrected in the receiver stage. As a result, bit error rates (BER) of IPR information increase because of spread error effects. In order to reduce the error effects, after rearranging the watermark signal to a two-dimensional array, its corresponding rows and columns are interchanged like

\[ w(u, v) = w(v, u), \]

where \( w \) and \( w \) are the original watermark signal and its interleaved one, respectively, and \( u \) and \( v \) mean the row and column of a macro block in a frame.

During the H.263 encoding process, one bit in \( W \) signal is embedded into a macro block. For an intra-frame, if the embedded bit is '1', DC components of DCT coefficients in a macro block are converted into odd values. Otherwise, they are converted into even values. Similarly, for an inter-frame, if the embedded bit is '1', a motion vector for a macro block is converted into an odd value. Otherwise, it is converted into an even value.

Since the block based DCT coefficients and motion vectors in which the watermark signal is embedded are encoded into a stream, the bit rate of the encoded video stream does not increase. Moreover, the encoded stream does not violate video encoding standards. The sender transmits the encoded and information-embedded stream to the receiver.

2) Video decoder

The receiver decodes and displays the received video stream. Because the stream obeys the standard H.263 stream
format, an ordinary H.263 decoder, which does not support the information detection function, can play it. On the other hand, an H.263 decoder supporting information detection function can detect the embedded information and the location of transmission errors. This can help to alleviate the degradation of the reconstructed video quality, and claim the IPR for the multimedia data.

The architecture of an H.263 decoder, which can decode the received stream, display the decoded video, and correct transmission errors using the embedded information, is illustrated in Fig. 9. For every macro block, embedded information can be detected from DCT coefficients and the motion vectors obtained by variable length decoding (VLD). When the decoded DCT coefficients exist for a macro block, their DC components determine the embedded information. If the DC components are even, the embedded information is determined to be '0'. Otherwise, it is determined to be '1'. Similarly, if the variable length decoded motion vector for a macro block is even, the embedded information is determined to be '0'. Otherwise, it is determined to be '1'.

The location of the corrupted macro block can be found by the bit-wise comparison between the detected signal \( W^* \) and the originally embedded signal \( W \) used in the encoder. If they have the same bit value, the corresponding macro block can be considered to be correct. Otherwise, the macro block can be considered to be corrupt, and it is reconstructed from the video data of the macro block in the same location of the previous frame. The receiver can display more improved quality of the video frame \( V^c \) from the received stream using the embedded information.

The watermark signal is reconstructed by de-interleaving the detected signal. De-interleaving is the reverse process of the previously discussed interleaving. The corresponding rows and columns of the detected signal are interchanged like

\[ w^*(u,v) = w^*_v (v,u), \]

where \( w \) and \( w^* \) are the detected watermark signal and its de-interleaved one, respectively, and \( u \) and \( v \) mean the row and column of a macro block in a frame.

The reconstructed IPR information \( I' \) can be obtained by applying the watermark signal, \( W^* \) detected in the decoding process of the received H.263 stream to soft-output Viterbi algorithm (SOVA), and it can be used to claim the rights for the multimedia data.

V. IMPLEMENTATION

The main board of the home server platform is shown in Fig. 10, and it integrates several home networks and multimedia functions on a board. Home network devices include an Ethernet port for uplink, 3 IEEE1394 ports, and 4 USB ports. In addition, the main board has an AC97 audio codec, a VGA graphics module, and 3 PCI slots for attaching a D-TV receiver, a multimedia codec module, and a network add-on board. The network add-on board has two PCMCIA slots for wireless home networks, an Ethernet port for down link, and a phone line connector for VoIP service.

Fig. 10. Home server platform main board

Fig. 11 shows the D-TV receiver module for receiving and displaying terrestrial D-TV broadcast. This module has dual tuner for ATSC and NTSC reception, and supports ATSC display formats such as 720p and 1080i. It also supports a VESA VIP 2.0 for transmitting the decoded video to the multimedia codec module. In addition, a received MPEG-2 stream can be transferred to the host bus using PCI Bridge.

Fig. 11. D-TV receiver module

Fig. 12 (a) shows a received D-TV picture using the receiver module in the home server platform, and (b) shows an example of EPG data browsing using PSIP table information presented by
the broadcast station. At most, 16 days of channels and program information can be browsed in the home server.

(a) Carphone images (19th frame: original, uncorrected, corrected)
(b) Fm images (50th frame: original, uncorrected, corrected)
(c) Trevor images (65th frame: original, uncorrected, corrected)

Fig. 14. Results of transmission error correction using information embedding

Fig. 13. Multimedia codec module

We tested Carphone, Fm, and Trevor video sequences consisting of 150 frames respectively to evaluate error resilient scheme. For these sequences, examples of images in the sender, uncorrected images in the receiver, and corrected images are shown in Fig. 14. In order to simulate a noisy channel, we used an error pattern that has a Rayleigh distribution with 5.0 dB of $E_b/N_0$ value. It can be ascertained that a reconstructed image can improve degradation of the received image by correcting transmission errors in a noisy communication channel.

Fig. 15. Bit error rates of reconstructed intellectual property rights information

Embedded information for detecting transmission errors can also be used to claim IPR for multimedia data. The IPR information for multimedia data can be reconstructed by applying the detected watermark signal to a Viterbi decoder. The IPR detection results for three video streams are shown in Fig. 15. In noisy environments such as below 5.5 dB of $E_b/N_0$ value, BER of reconstructed IPR information are relatively large compared to high $E_b/N_0$ channels. On the other hand, if $E_b/N_0$ value is greater than 6.0 dB, an error bit is rarely found and the IPR information can be reconstructed effectively.

VI. CONCLUSIONS AND FUTURE WORKS

In this paper, multimedia data processing part in a home server platform has been designed and implemented. In order
to present functions as a multimedia data server in the household, a D-TV receiver and a multimedia codec modules have been implemented in the home server. These modules can interface with the host via PCI bus. Without a D-TV set-top box, users can watch terrestrial ATSC broadcast and browse PSIP table information using the D-TV receiver in the home server. Users can also watch the D-TV contents with a remote client using the multimedia codec module in the home server. In addition, the multimedia codec can be used in various applications such as remote conferences, videophone, and remote surveillance. In order to correct transmission errors generated in a noisy channel, an error resilient scheme using information hiding technique has been considered in the multimedia codec module.

Though the concept of a home server platform is not clearly established yet, the home server is expected to be a core device within home in the near future digital information appliance environments. The home server can present various multimedia services and control various information appliances, at anytime and anywhere. Furthermore, it can manage all information within a home, and present information communication methods among family members. Research for reinforcing the functions and presenting more comfortable user interface environments in the home server should continue to advance new generation information appliance environments. Besides, a noble transcoding algorithm including the conversion between multimedia data formats and down sampling in the frequency domain should be implemented to provide various multimedia services.

REFERENCES


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