Low power 2.4 GHz quadrature generation for Body Area Network applications

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Abstract—This paper presents two implementations of low-power quadrature generation for the new Bluetooth low energy standard in the 2.4 GHz ISM band. Both implementations have been designed in a 90 nm CMOS technology for a 1 V supply voltage and post-layout simulation results are presented. The first implementation is a quadrature voltage controlled oscillator (QVCO) with 180 \( \mu \)W power consumption and a phase noise of -112.7 dBc/Hz @1MHz. It employs a new technique to reduce the influence of magnetic coupling between the two spiral inductors. The second implementation employs a VCO running at twice the frequency with a subsequent divide-by-2 stage. Its total power consumption is 320 \( \mu \)W and the phase noise at the quadrature outputs is -115.7 dBc/Hz @1MHz.

I. INTRODUCTION

Body area networks (BAN) based on miniature wireless sensors are expected to allow for a lot of new applications of wireless communication. They range from entertainment and automation to health care or human interface devices. In many of these applications, the need for ultra-low power consumption is prioritary since network nodes are supplied by small batteries or even rely on autonomous energy scavenging techniques.

In order to cope with this operation conditions, the Bluetooth consortium has announced a low energy (LE) enhancement with relaxed radio specifications for the sensor nodes [1]. The increased channel spacing together with the reduced blocking requirements as compared to the core version of the standard, now allow for frequency synthesizers with much lower power consumptions. This is particularly important as the syntheziser has to be frequently turned on to detect and receive commands.

The power consumption of the frequency synthesizer is usually dominated by the voltage controlled oscillator (VCO) and the quadrature generation. Therefore, it is necessary to find the most power efficient solution both on circuit and on architecture levels. In this paper we first analyze the available oscillator topologies in section II and quadrature generation architectures in section III with respect to their power consumption. This is particularly important as the synthesizer has to be frequently turned on to detect and receive commands.

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dominated by the integrated inductor and can be approximated with
\[
\frac{1}{R_p} \approx \frac{Q_L}{\omega_0 L (Q_L^2 + 1)} \quad (1)
\]
where \(Q_L\) is the inductor's quality factor at the oscillating frequency \(\omega_0\) [4]. This implies that apart from a high quality factor also a large inductance is needed. However, the inductance can only be increased until the parasitic capacitance precludes resonance at our design frequency. Bearing in mind this limitation we will select our inductor by searching for a minimum in (1).

### III. Architectures for Quadrature Generation

In order to demodulate the GFSK signals specified by Bluetooth LE, quadrature Local Oscillations (LO) have to be generated. Quadrature may be obtained by combining a VCO running at twice the desired frequency with a divide-by-2 circuit (VCO+DIV2), using a quadrature VCO with two coupled cores (QVCO) or by employing a passive RC-CR network. The latter option will not be considered in the following as it suffers from excessive power consumption required for buffering and cancellation of amplitude mismatches.

The most common approach is the VCO+DIV2 due to its area efficiency and simplicity. It requires only one VCO core and thus only one inductor. However, its operation at twice the frequency requires a smaller inductance which leads to an increased power consumption. Moreover, the divide-by-2 circuit usually consumes a significant amount of power due to its very high input frequency.

Therefore, the QVCO approach is generally regarded as the option that consumes less power [5], [6]. A divide-by-2 block is not needed and the lower oscillating frequency allows larger inductances, thus favoring tank losses reduction according to (1). The main drawback is a larger area occupation because of the two required inductors. Another problem of the QVCO solution is the phase error due to magnetic coupling between the two inductors [7]. However, since this phase error is deterministic it may be reduced through a decoupling network as implemented in our solution presented in section IV.

### IV. Implementation

The two quadrature generation techniques discussed in section III have been implemented using a 90nm CMOS process\(^1\). Both implementation have been taped out for fabrication and their delivery is expected in December 2009.

#### A. QVCO

The quadrature VCO, shown in Fig. 2, is implemented as two current-reuse VCOs coupled to each other by means of coupling transistors. The two 7-turn symmetrical inductors (\(L=13.3\) nH, \(Q_L=12\) @2.45 GHz) have been selected by minimizing tank losses according to (1). Consequently, a very low bias current of 90 \(\mu\)A per core is sufficient to obtain a single-ended amplitude of \(\approx 150\) mV. Coarse tuning to compensate process variations is achieved with a switched MOM-capacitor bank while PMOS varactors allow for fine frequency control within a phase-locked loop.

The coupling between the two cores at a phase difference of \(90^\circ\) is achieved by the parallel coupling transistors MCx. As shown in [8], phase shifting of ideally \(90^\circ\) in the coupling path reduces the phase noise and increases the oscillating amplitude. But since active phase shifting introduces additional power consumption we have implemented passive phase shifters of approximately \(45^\circ\) formed by a serial resistance and the gate capacitance of MCx. In order to allow measurements with and without phase shifting the resistances may be bypassed using switches.

While the dedicated coupling mechanism forces the QVCO to operate in quadrature, the parasitic magnetic coupling tends to pull the QVCO towards in-phase or anti-phase operation. This problem may be avoided by using four inductors instead of two allowing for full symmetry with respect to the four quadrature phases [7]. Therefore, this solution is independent of the operating frequency and the magnitude of magnetic coupling. Alternatively, the magnetic coupling of the two-inductor QVCO may also be canceled. In the two-port representation of the coupled inductors [Fig. 3(a)] the magnetic coupling is represented by the transfer admittances \(y_{12}\) and \(y_{21}\). Therefore, adding a shunt network with transfer admittances of equal magnitude and opposite signs cancels the coupling. Fig. 3(b) shows the simplest configuration of such a network with
\[
C_1 = \frac{2 \Re \{y_{12}\}}{\omega_0 L} \approx \frac{2k}{\omega_0 L} \quad (2)
\]
\[
R_{X1} = -\frac{1}{2 \Re \{y_{21}\}} \approx \frac{Q_L \omega_0 L}{4k}. \quad (3)
\]

Using this structure the required value of \(R_{X1}\) is approximately 50 k\(\Omega\). In order to reduce the required resistance to values in the order of 1 k\(\Omega\), the network of Fig. 3(c) is

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\(^1\)Triple-well process with 7 metal layers (2 thick top layers)
implemented instead.
\[
C_{X2} = \frac{-4}{\omega_0 \Im \{1/y_{21}\}} \approx \frac{4k}{\omega_0^2 L} \\
R_{X2} = -\frac{1}{2} \Re \{1/y_{21}\} \approx \frac{\omega_0 L}{kQ_L} \\
C_2 = \frac{2 \Im \{y_{21} - 1/(y_{21})^*\}}{\omega_0} \approx \frac{4k}{\omega_0^2 L}
\]  

This network consists of MOM-capacitors with \( C_2 = C_{X2} = 16 \ fF \) and high-resistive Poly resistors with \( R_{X2} = 920 \ \Omega \).

Clearly, this cancellation technique is both frequency dependent and susceptible to process variations. Therefore, it may be used in narrow-band systems and only to reduce the phase error due to magnetic coupling to a tolerable level. Fig. 4 shows that the decoupling network achieves at least a 11.5 dB reduction of the coupled voltage from one inductor to the other (both resonating at 2.45 GHz) for the worst-case process corners which are mainly defined by the MOM capacitance variation. The layout implementation of the quadrature VCO with decoupling network is shown in Fig. 5.

### B. VCO+DIV2

Also the VCO running at twice the frequency is implemented as a current-reuse cross-coupled LC VCO. The same inductor selection procedure as for the QVCO has lead to a symmetrical 4-turn inductor (\( L=4.6\ n\text{H}, \ Q_L=12\ @4.9\ GHz \)). Due to the lower inductance compared to the QVCO solution an increased bias current of 150 \( \mu\text{A} \) is required to obtain a single-ended amplitude of \( \approx 250\ \text{mV} \). Again, coarse and fine tuning has been implemented by a switchable capacitor bank and PMOS varactors.

For the divider-by-2 a master-slave configuration of two source-coupled-logic (SCL) latches is commonly used [9]. However, in order to lower the power consumption we have used dynamic single-transistor-clocked (DSTC) latches [10]. Two DSTC latches in a master-slave flip-flop configuration can be seen as a two-stage injection-locked differential ring oscillator. Such injection-locked dividers (ILD) have recently been demonstrated with extremely low power consumption [11], [12]. However, on contrast to these ILDs our DSTC based divider operates differentially and thus offers truly symmetrical output phases.

The circuit implementation of the VCO with the DSTC based divider-by-2 is shown in Fig. 6. Note that no buffering between the VCO and the divider is needed because the cross-coupled NMOS pair of the VCO already provides the required common mode voltage for the NMOS input of the divider with respect to process and temperature variations. Therefore, in the layout of the VCO+DIV2, shown in Fig. 7, these NMOS transistors are implemented as matched devices. The remaining transistors of the DSTC latches are almost minimum sized in order to reduce the power consumption of the divider.

The divider-by-2 block must be symmetrically laid out to achieve small phase errors. Still, a postlayout phase error smaller than 2\( ^\circ \) is hardly achievable. Moreover, mismatch between the minimum sized transistors of the divider introduces a significant statistical phase error with a standard deviation in the order of 4\( ^\circ \).

### V. POSTLAYOUT SIMULATION RESULTS

Both implementations including parasitics extracted from the layouts have been simulated using Cadence® SpectreRF. The simulations are performed with identical load conditions, i.e., in both cases the I and Q outputs have been loaded by output drivers and by the divide-by-4 input stage of a phase-switching prescaler. This divider is also based on the DSTC latches with differently sized input transistors and was also
simulated with extracted parasitics. Moreover, the magnetic coupling between the two QVCO inductors has been estimated using an electromagnetic solver (Momentum) at $k = 1.4\%$.

The phase noise simulation in Fig. 8 shows, that activating the phase shifting in the coupling path of the QVCO reduces the phase noise contribution of the coupling transistors at lower offset frequencies where the $1/f$-noise is dominating. The VCO+DIV2 phase noise is strongly dominated by the LC oscillator. Only at offset frequencies larger than $\approx 10$ MHz thedivider-by-2 contributes significantly to the overall phase noise. Comparing the two architectures, the VCO+DIV2 performs better at larger offset frequencies (>1MHz) which is also the critical frequency range as it is outside the PLL bandwidth.

Table I summarizes the important parameters of both implementations while Table II compares the two designs to recently published work. The figure-of-merit (FoM), defined as in [5]  

\[ FoM(\Delta \omega) = 10 \log \left( \frac{\omega_0}{\Delta \omega} \right) \left( \frac{1}{C(\Delta \omega)} \right)^{\frac{1}{2}} \left( \frac{1 \text{mW}}{P} \right). \]  

relates the phase noise $\mathcal{L}$ at the offset frequency $\Delta \omega$ to power dissipation $P$ and oscillating frequency $\omega_0$.

### VI. CONCLUSIONS

After revising low-power strategies of oscillators and quadrature generation two prototypes have been presented.

### VII. ACKNOWLEDGEMENTS

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### REFERENCES


#### TABLE I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>QVCO</th>
<th>VCO+DIV2</th>
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<tbody>
<tr>
<td>Supply voltage (V)</td>
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<td>1.0</td>
</tr>
<tr>
<td>Oscillator current (µA)</td>
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<td>155</td>
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<tr>
<td>Divider current (µA)</td>
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<tr>
<td>Output amplitude (V)</td>
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<tr>
<td>Output Phase Noise (dBc/Hz)</td>
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<td>-91.4</td>
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<tr>
<td></td>
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<tr>
<td></td>
<td>-112.7/-111.1</td>
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<td></td>
<td>@1MHz</td>
<td>@1MHz</td>
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<td>Area (mm²)</td>
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<td>deterministic</td>
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a Single-ended peak-to-peak

b Performance with/without phase shifting

### TABLE II

<table>
<thead>
<tr>
<th>Architectures</th>
<th>CMOS Process (nm)</th>
<th>Frequency (GHz)</th>
<th>Power (mW)</th>
<th>Phase Noise (dBc/Hz)</th>
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<td></td>
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</tr>
<tr>
<td>QVCO</td>
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<td>2.4</td>
<td>0.18</td>
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<tr>
<td>QVCO+DIV2</td>
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<td>2.4</td>
<td>0.32</td>
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</table>

Although the QVCO approach requires much more area it consumes far less power than the VCO+DIV2 architecture and achieves a comparable phase noise performance. A new technique to reduce the deterministic phase error induced by magnetic coupling in the QVCO has also been presented.

#### REFERENCES

TABLE II

<table>
<thead>
<tr>
<th>Performance comparison to recent quadrature generators</th>
<th>[9]</th>
<th>[13]</th>
<th>[14]</th>
<th>This Work</th>
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<td>CMOS Process (nm)</td>
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<td>180</td>
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<td>Architecture</td>
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<td>Frequency (GHz)</td>
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<tr>
<td>Power (mW)</td>
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<td>1.3/1.5</td>
<td>0.6</td>
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* based on post-layout simulation