

Quantum Cellular Automata based Novel Unit 2:1 Multiplexer

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ABSTRACT

Quantum Cellular Automata (QCA) is an emerging nanotechnology and one of the top six technologies of the future. CMOS technology has a lot of limitations while scaling into a nano-level. QCA technology is a perfect replacement of CMOS technology with no such limitations. In this paper we have proposed one 2:1 multiplexer circuit having lowest complexity and area compared to the existing QCA based approaches. The proposed design is verified using QCADesigner.

General Terms

QCA, QCA Designer, Multiplexer.

Keywords

Majority Voter circuit, Minority Voter Circuit, Nanotechnology .

1. INTRODUCTION

CMOS Technology is approaching its scaling limit very fast. In practical point of view this technology in nano-scales is facing lot of problems. So in order to enhance the performance of a system new nano-technology approach should be taken into account. Quantum Cellular Automata[13,14] is now one of the promising and emerging technology which not only providing a solution at nano- scale, but also offers solutions that currently CMOS technology is facing[1,2]. The basic building block of every QCA circuit is majority gate and every QCA circuit can be built using Majority and inverter gate [3].The majority logic can be implemented in a different manner from that of Boolean logic. The Boolean logic operators (like AND, OR and their complements) and other digital functions can be implemented using Majority logic [4]. The majority logic can be termed as more powerful for implementing digital functions because of very small number of logic gates [5, 6].

In this paper we propose a new design methodology for a 2:1 MUX Using this design as a unit complex MUX design is possible. In comparison to existing implementation, this method has demonstrated significant improvements. The proposed 2:1 MUX resulted in decrease in cell counts and decrease in input to output delay. The presented design is justified using QCA Designer [7] simulation results.

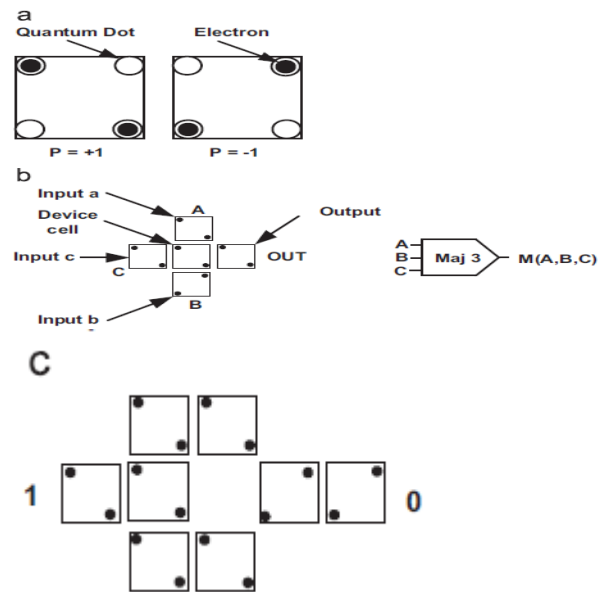


Fig 1: (a) Basic QCA cell and binary encoding, (b) A QCA majority gate and (c) A QCA inverter.

2. DESCRIPTION AND ANALYSIS

2.1 Relevant QCA Concept

This technology is built up in cells. Each cell has 2 electrons trapped on it [8,9] and 4 as illustrated in Fig1(a). The electrons can be on any island and can tunnel between the islands. However, due to Coulomb repulsion, they will always settle to one of two stable states. One configuration of charge represents a binary “1,” the other a “0,” but no current flows into or out of the cell[11,12].

The field from the charge configuration of one cell alters the charge configuration of the next cell. Remarkably, this basic device-device interaction, coupled with a clocking scheme for modulating the effective barrier between states, is sufficient to support general- purpose computing with very low power dissipation. Binary wire can be assembled where all cells in the chain have the same value. The fundamental logic gate is the Majority Gate. A majority gate takes three inputs; its output is equal to whichever two inputs agree as illustrated in Fig 1(b). Assuming three inputs labeled A, B and C, the logic function of majority gate is

$$M(A,B,C)=AB+BC+AC \dots\dots\dots (1)$$

Logical AND and OR functions can be implemented from majority voter by presetting one input immutably to binary values 0 and 1, respectively. A signal is complimented by the not gate as in fig 1(c).

2.2. Advantages of QCA

This technology has many advantages.

- It is “edge driven,” meaning an input is brought to an edge of a QCA block; it is evaluated and output at another edge. This also means that no power lines need be routed internally.
- The second advantage is that QCA systems should be very low power, because there is no current flowing. Only enough energy needs to be added to lift the electrons from their ground states.
- Finally, QCA cells are very small.

2.3. QCA Clocking

The clocking of QCA [10] can be accomplished by controlling the potential barriers between adjacent quantum-dots. When the potential is low the electron wave functions become delocalized resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate, and thus, the electrons begin to localize. As the electrons localize, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs and as a result, the actual inputs can start to feed in new values. This enables easy pipelining of QCA circuits. It has been shown that four clocking zones each $\pi / 2$ degrees out of phase is all that is required by any QCA circuit as shown in Figure 2.

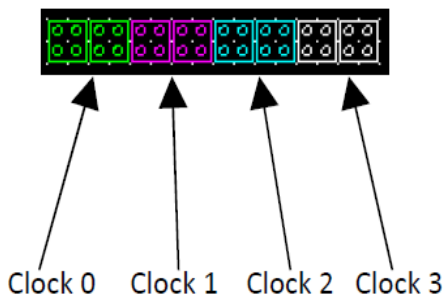


Fig 2: QCA Clocking

3. EARLIER WORK

In article [18], a new design has been proposed. In this design 31 number of cell have been used and four clocks are applied there, so total delay is 360° .

In article [17] another design has been proposed where author(s) have used reduced number of cells and also there is reduction in delay. In this design 27 number of cells have been used and with a delay of 270° .

4. ANALYSIS OF PROPOSED DESIGN

Recent methodologies [15, 16, 17, 18] have shown a lot of improvements in designing QCA multiplexers in terms of complexities (number of cells), areas and speed(delay) over their past methodologies. But the proposed one is having less

complexity, consume less area and higher speed as compared to recent methodologies.

Generally a 2 to 1 multiplexer is having two inputs A and B, one selection input S and one output F as in Fig .3

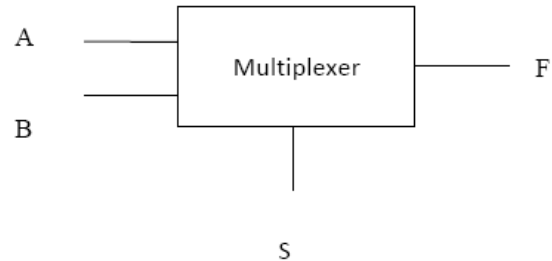


Fig 3: Conventional Multiplexer

Basically our proposed design is composed of two majority voter gate and one minority voter gate as in Fig 4

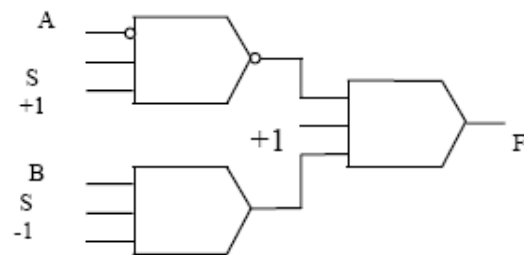


Fig 4: Outline of proposed QCA multiplexer

The input A is complimented before it is applied to the minority voter gate. The A input and selection input S is Ored as the third input of the same is applied with a fixed ‘1’ signal voltage. The Minority voter gate will be given an output which can be represented by a relation as in equation 2,

$$Out_{minv1} = (A' + S)' = AS' \dots\dots\dots (2)$$

Or it can be represented by a Majority-voter logical expression as in equation 3,

$$Out_{minv1} = (Majv(A', S, +1))' = Minv(A', S, +1) \dots\dots\dots (3)$$

The B input is directly applied to another majority-voter gate. The selection input S, input B and another fixed input voltage ‘-1’ are simultaneously applied to this majority-voter gate and will generate a relation as in equation 4,

$$Out_{majv2} = BS \dots\dots\dots (4)$$

Or it can be represented by a Majority-voter logical expression as in equation 5,

$$Out_{majv2} = Majv(B, S, -1) \dots\dots\dots (5)$$

Finally both the majority voter and minority voter logic gates are directly connected to another majority voter gate whose third input is applied with a fixed voltage ‘1’ and generating the output voltage F. This output F can be represented by means of a logical expression as in equation 6 and by means of a majority-voter logical expression as in equation 7.

$$F_{\text{output}} = A S' + B S \dots\dots\dots (6)$$

$$F_{\text{output}} = \text{Majv} ((\text{Majv} (A', S, +1))', \text{Majv} (B, S, -1), +1) \dots\dots (7)$$

Now when S = ‘0’, based on equation 7,

$$(\text{Majv}(A', S, +1))' = (\text{Majv}(A', 0, +1))' = A.$$

and

$$\text{Majv}(B, S, -1) = \text{Majv}(B, 0, -1) = 0.$$

$$\text{So, } F_{\text{output}} = \text{Majv}(A, 0, +1) = A.$$

Now when S = ‘1’, based on equation 7,

$$(\text{Majv}(A', S, +1))' = (\text{Majv}(A', 1, +1))' = 0.$$

and

$$\text{Majv}(B, S, -1) = \text{Majv}(B, 1, -1) = B.$$

$$\text{So, } F_{\text{output}} = \text{Majv}(0, B, +1) = B.$$

In the proposed design we have used 23 numbers of cells and accordingly circuit area is reduced and it is comparatively dense enough and also delay here is 270⁰. We have shown all the data with table 1.

Table 1: Comparative study of our proposed design with some most recent designs

Parameters	2:1 Mux as in paper [18]	2:1 Mux as in paper [17]	Our proposed 2:1 Mux	Percentage Reduction/Increase from the most Recent Design
No of Cells	31	27	23	14.81
Total Area	37908 Sq nm	23328 Sq nm	18144 Sq nm	22.2
Cell Area	10044 Sq nm	8748 Sq nm	7452 Sq nm	14.81
Area Usage	26.50%	37.50%	41.07%	3.57
Input to Output Delay	Four Clock pulses	Three Clock Pulses	Three Clock Pulses	Equal

5. SIMULATION AND PRACTICAL RESULT

For the proposed circuit layout and functionality checking, a simulation tool for QCA circuits QCADesigner version 2.0.3, is used. The following parameters are used for a bitable approximation: cell size=18 nm, clock high = 9.800000e-022 J, clock low=3.800000e-023 J, Dot diameter= 5 nm. Most of the mentioned parameters are default values in QCADesigner. Fig 5 and 6 show circuit layout and simulation results of proposed Multiplexer.

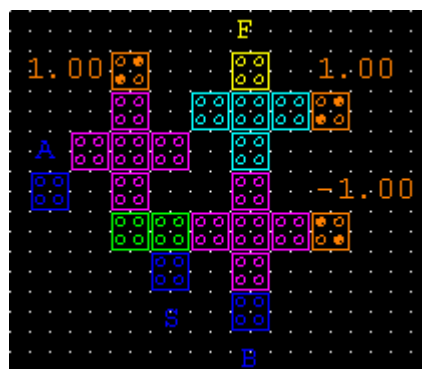


Fig 5: Proposed design of QCA Multiplexer on QCADesigner

As we have found that it is still possible to reduce the complexity (cell number), area, delay and can increase density up to some extent, in immediate manner we started looking for a new design methodology for 2:1 MUX which is very simple but very efficient. For the same we have tried a conventional approach, we used one AND gate for ANDing one input with selection line and one OR gate for ORing another input with selection line and One OR gate to add them.

6. CONCLUSION

Our proposed methodology is an efficient way that greatly reduces no of cells, area and delay in signal propagation from input to output. By this methodology we can go for designing complex multiplexers. This methodology is very simple to implement also. This QCA technology is the future nanotechnology and different classical models can be replaced by this QCA logic and this will become much more efficient and less complex than its classical counterpart.

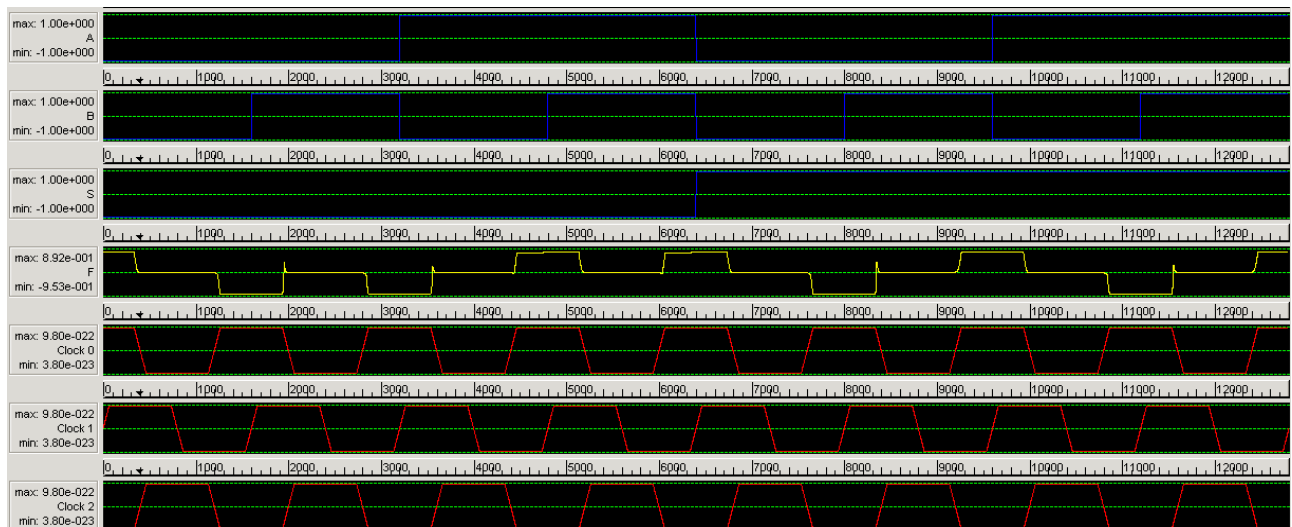


Fig 6: Simulation result of Proposed Multiplexer

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