Floorplan-Aware Decoupling Capacitance Budgeting on Equivalent Circuit Model

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Abstract — In this paper, based on an equivalent circuit model for any noise-aware power network, an accurate estimation uses an exponential discharge style in the equivalent RC circuit to predict the decoupling capacitance (decap) size of any circuit module in a given floorplan. Furthermore, a floorplan-aware budgeting approach is proposed to assign feasible decaps onto all the circuit modules to release all the IR-drop noises in the floorplan. The experimental results show that our proposed budgeting approach based on an accurate estimation obtains very promising results for MCNC benchmark circuits.

I. INTRODUCTION

Generally speaking, the advanced techniques for the design and optimization of the power networks have become essential to tackle the signal integrity in modern VLSI chips. To meet the current electro-migration and voltage IR-drop constraints, the design of the power networks typically consists of the following steps: topology design[1-2], wiring area optimization in power networks[3-6] and the allocation and placement of decoupling capacitances (decaps)[7-8]. Basically, the topology design of a power network is commonly carried out by using a power router. In the topology design of a power network, the optimal work focuses on the optimal assignment of the pins to the pads and the placement of power pads on the power network. It is clear that the topology of a power network has a significant influence on the final layout area. In general, the topology of a power network is often designed as a power mesh, and the power network is divided into uniform power grids. However, the topology design of a power mesh may be a static power design. Based on the topology of a fixed power network, the widths of the wire segments in a power network and the positions of decaps inside a floorplan are determined to meet the current electro-migration and voltage IR-drop constraints by using some wire sizing and decap placement approaches. Most of these approaches formulate the wire sizing problem as a constrained nonlinear programming problem. However, the decap placement in a power network may have a significant over-utilization cost of the chip area. Hence, it is important for the chip cost to develop an efficient and accurate decap budgeting approach on a given floorplan.

For the decap budgeting on a given floorplan, a greedy estimation[7] and an iterative estimation[8] have been proposed. However, these two estimations are based on a linear discharge assumption. In [7], it is assumed that the current of any IR-drop module can be fully provided by the required decap. According to an exponential discharge style in the resultant RC circuit, the required decap is over-estimated and the decap budget is obtained by the proposed greedy model. In [8], it is assumed that the current of any IR-drop module can be provided by the original power supply and the required decap in a linear-ratio model. According to an accurate exponential discharge style in the resultant RC circuit, the required decap is under-estimated and the decap budget is obtained by the proposed iterative model. Beside that, the two estimations only predict feasible decap to release the IR-drop noise inside the IR-drop module.

In this paper, based on an equivalent circuit model for any noise-aware power network, an accurate estimation uses an exponential discharge style in the equivalent RC circuit to predict the decap of any circuit module in a given floorplan. Furthermore, a floorplan-aware budgeting approach is proposed to assign feasible decaps onto all the circuit modules to release all the IR-drop noises in the floorplan. The experimental results show that our proposed budgeting approach based on an accurate estimation obtains very promising results for MCNC benchmark circuits.

II. PROBLEM FORMULATION

Given a floorplan with a set of fixed circuit blocks, the floorplan area can be obtained as the bounding rectangle covering the floorplan and treated as a floorplan plane. It is assumed that each circuit block inside the floorplan has some power nodes on its block boundary to feed the necessary power into the circuit block. Basically, it is possible for its power node to determine the maximum current drawn by one circuit block by using the current estimation techniques[9]. Hence, any power node in a given floorplan can be modeled as a constant current source fed from the power node to ground. As shown in Fig. 1, there are 17 circuit blocks inside the floorplan, and each circuit block inside the floorplan has a power node on its block boundary.

For the design of a power network, the current electro-migration constraint is generally solved by the techniques of wiring area optimization. However, to meet the electro-migration constraint in a power network, the IR-drop noise
may be yielded after running wiring area optimization. Generally speaking, the possible IR-drop noise in a power network can be further solved by allocating decaps into the original floorplan. In the decap allocation, firstly, the size of the necessary decoupling capacitor must be estimated according to the voltage in the possible IR-drop noise. Based on the sizes of all the necessary decoupling capacitors, the decap areas of all the circuit blocks can be further computed. Finally, all the decap areas must be allocated and integrated into the original floorplan.

![Fig. 1 Power nodes and their equivalent current model](image1)

Given a noise-aware power network with a set of power nodes which have their constant current requirement inside an LB-compact floorplan, the positions of the power pads on the power network and the voltage IR-drop constraint, the floorplan-aware decap budgeting (FDB) problem is to estimate the decap budget of all the circuit modules in the given floorplan to satisfy the IR-drop constraint for all the power nodes.

### III. FLOORPLAN-AWARE DECAP ESTIMATION ON EQUIVALENT CIRCUIT MODEL

As any circuit module in a floorplan has an IR-drop noise, the IR-drop noise can be released by inserting feasible decap inside the circuit module or its neighboring circuit module.

#### 3.1 Equivalent Circuit Model for Power Network

Suppose there are M circuit modules in the floorplan and the switching current of module k is \( I_{r,k} \), \( k = 1,2,\ldots,M \). Let \( V_k \) be the voltage of module k without inserting any decap and let \( V_{r,k} \) be the minimum voltage to release the IR-drop noise. Hence, there is no IR-drop noise for module k if \( V_k \geq V_{r,k} \). As \( V_k < V_{r,k} \) for module k, feasible decap can be inserted inside module k or its neighboring circuit module. Let \( V_r \) be the voltage of the neighboring circuit module r for module k without inserting any decap. It is assumed that any power mesh has some power pads with a fixed power-supply voltage, \( V_{dd} \), and \( V_r \geq V_k \) for modules k and r.

![Fig. 2 Equivalent circuit model of a power network for module k](image2)

As shown in Fig. 2, as a given noise-aware power mesh provides the switching current of modules k and r with the voltages, \( V_k \) and \( V_r \), the power mesh can be modeled as an equivalent circuit with two relative resistances, \( R_k \) and \( R_r \). Clearly, the resistances, \( R_k \) and \( R_r \), can be obtained as \( \frac{V_{dd} - V_r}{I_{r,k}} \) and \( \frac{V_k - V_r}{I_{r,k}} \), respectively.

#### 3.2 Decap Charge/Discharge Style

Based on the proposed equivalent circuit model for modules, k and r, in a given floorplan, a feasible decap, \( C_{d,k} ^{r,k} \), can be inserted inside module r to release the IR-drop noise for module k if \( V_k < V_{r,k} \). As module k does not need any switching current, the equivalent circuit can be simplified as a RC charge circuit as shown in Fig. 3.

![Fig. 3 Equivalent decap charge model](image3)

In the RC charge circuit, the power-supply voltage, \( V_{dd} \), provides a time-dynamic current, \( I_r(t) \), to charge the decap, \( C_{d,k} ^{r,k} \), with a time-dynamic current, \( I_k(t) \), and the initial voltage, \( V_r(0) \), of the decap is 0. Hence

\[
I_r(t) + I_k(t) = 0, \quad V_r(0) = 0. \tag{1}
\]

By substituting the related voltage items for the time-dynamic current, \( I_k(t) \) and \( I_r(t) \), we can obtain the following equation as

\[
\frac{V_{dd} - V_r(t)}{R_k}C_{d,k} ^{r,k} \frac{dV_r(t)}{dt} = 0, \quad V_r(0) = 0 \tag{2}.
\]

Furthermore, we can obtain the following ordinary derivation equation as

\[
V_r(t) - R_kC_{d,k} ^{r,k} \frac{dV_r(t)}{dt} = V_{dd}, \quad V_r(0) = 0 \tag{3}.
\]

Finally, we can obtain the time-dynamic voltage, \( V_r(t) \), for module r as

\[
V_r(t) = V_{dd}(1 - e^{-\frac{t}{R_kC_{d,k} ^{r,k}}}). \tag{4}
\]

On the other hand, as module k needs the switching current, the equivalent circuit can be modelled as a RC discharge circuit as shown in Fig. 4.

![Fig. 4 Equivalent decap discharge style](image4)

In the RC discharge circuit, the power-supply voltage, \( V_{dd} \), provides a time-dynamic current, \( I_k(t) \), and the decap, \( C_{d,k} ^{r,k} \), discharges a time-dynamic current, \( I_k(t) \), to satisfy the current requirement, \( I_{r,k} \), for module k and the initial voltage, \( V_k(0) \), of the decap is \( V_{dd} \). Hence
By substituting the related voltage items for the time-dynamic current, $I(t)$ and $I(t)$, we can obtain the following equation as

$$I,v(t)+I,v(0)=I,v.$$  

(5)

Furthermore, we can obtain the following ordinary derivation equation as

$$I,v(t)-R_C \frac{dV}{dt}=I,v, \quad V,v(0)=V,v.$$  

(6)

Finally, we can obtain the timing-dynamic voltage, $V,v(t)$, for module r as

$$V,v(t)=(V,v-V,v) \cdot e^{\frac{-t}{V_C}} + V,v,$$  

(8)

and the timing-dynamic voltage, $V,d(t)$, for module k as

$$V,d(t)=V,v(t)-R_C I,v=V,v, e^{\frac{-t}{V_C}} + V,v.$$  

(9)

3.3 Decoupling Capacitance Estimation

According to the time-dynamic voltage, $V,v(t)$, for module k with the decap insertion inside module r, the IR-drop noise for module k can be released if $V,v(t) \geq V,v$ for a required period time $T$. Hence, we can obtain the following constraint to release the IR-drop noise for module k as

$$V,v(t) \geq V,v,  \quad (V,v-V,v) \cdot e^{\frac{-t}{V_C}} + V,v, \geq V,v.$$  

(10)

Since the resistance, $R_C$, is obtained as $V,v-V,v$ and $T$ is a positive constant, we can obtain the following constraint for the size of inserted decap inside module r to release the IR-drop noise for module k as

$$C_{d,k} \geq \frac{T \cdot V,v}{V,v-V,v} \cdot \left[ \ln \left( \frac{V,v-V,v}{V,v-V,v} \right) \right], \text{ if } V,v < V,v - V,v.$$  

(11)

Therefore, the decap inside module r to release the IR-drop noise for module k can be estimated as

$$C_{d,k} = \frac{T \cdot V,v}{V,v-V,v} \cdot \left[ \ln \left( \frac{V,v-V,v}{V,v-V,v} \right) \right], \text{ if } V,v \geq V,v + V,v.$$  

As the decap is inserted inside module k to release the IR-drop noise for module k, the value, $V,v$, can be replaced with the value, $V,v$, and the decap inside module k can be estimated as

$$C_{d,k} = \frac{T \cdot V,v}{V,v-V,v} \cdot \left[ \ln \left( \frac{V,v-V,v}{V,v-V,v} \right) \right].$$

IV. FLOOPLAN-AWARE DECAP BUDGETING

Basically, the decap inside a high-voltage circuit module can provide extra current to a low-voltage circuit module. Hence, the decap-insertion ordering for all IR-drop modules is arranged from the highest-voltage module to the lowest-voltage module. According to the constraint in (11) for the decap estimation of module r for the IR-drop noise in module k, the possible circuit modules to provide extra current to module k are constrained inside a decap supply window with the legal voltage range $(V,v - V,v,m)$ as shown in Fig. 5.

The decap budget for module r is converted to the required silicon area, $S_{d,k}$, to fabricate the required decap, $C_{d,k}$, to release the IR-drop noise of module k as follows:

$$S_{d,k} = \frac{C_{d,k}}{C_{w}}, \quad r,k=1,2,...M$$

, where $C_{w}$ is the unit area capacitance of a MOS capacitor. As the white-space area, $W,S$, is around module r, the effective decap area, $E,S_{d,k}$, of module r can be defined as

$$E,S_{d,k} = \left\{ \begin{array}{ll} S_{d,k} - W,S, & \text{if } S_{d,k} > W,S, \\
0, & \text{if } S_{d,k} \leq W,S. \end{array} \right.$$  

To release the IR-drop noise of module k, a circuit module r inside the decap supply window of module k with a minimum effective decap area, $E,S_{d,k}$, can be obtained for the floorplan-aware decap budget of module r. As the floorplan-aware decap budget is inserted into module r, the white-space area, $W,S$, around module r will be modified. Basically, as the IR-drop condition in any module with the higher voltage has been released, the IR-drop noise in the other modules with the lower voltage will be accurately estimated. Until the IR-drop noises of all the circuit modules in a given noise-aware floorplan are fully released, the floorplan-aware decap budgeting process will stop. Therefore, the floorplan-aware decap budgeting, FloorplanAwareDecapBudget(), will be described as follow.

FloorplanAwareDecapBudget(F, N, V,v,m)

Input: All the circuit modules with constant current requirement in a given floorplan, F;  
A noise-aware power network, N, and the minimum IR-drop voltage, V,v,m.

{  Sort all the circuit modules with an IR-drop noise into a decreasing order according to the module voltage;  \while (there exists any module with an IR-drop noise)  {  Find the IR-drop module with the highest voltage;  Construct an equivalent circuit and Estimate the decap to be inserted inside the circuit module with minimum effective decap area according to the minimum voltage, V,v,m;  Insert the estimated decap into the noise-aware power network, N, and Modify the white-space area around the processing circuit module;  }  }

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Recompute the module voltages of all the circuit modules in the floorplan, \( F \), according to the inserted decap in the power network;

Output the decap budget for all the circuit modules in the floorplan, \( F \);

V. EXPERIMENTAL RESULTS

For floorplan-aware decap estimation, a previous greedy estimation [7], a previous iterative estimation [8] and our proposed estimation have been tested for the floorplan results of five MCNC benchmark circuits, apte, xerox, hp, ami33 and ami49 implemented in a 0.25um technology under a noise-aware power mesh. The power supply, \( V_{dd} \), is 2.5 V and the minimum voltage, \( V_{min} \), is 2.25V, that is, the maximum tolerant noise is 0.25V. The required current, \( I_{req} \), of module \( k \), \( k = 1, 2, \ldots, M \), is \( D_k \cdot A_k \), where \( D_k \) is the worst case current density for 0.25um technology based on the technology parameters and \( A_k \) is the area of module \( k \).

For the floorplan-aware decap allocation, our proposed SA-based approach for the floorplan-aware decap placement on our proposed floorplan-aware budgeting has been implemented by using standard C++ language and run on a Pentium IV 2.8GHz machine. The floorplan results of five MCNC benchmark circuits, apte, xerox, hp, ami33 and ami49 are applied to allocate the inserted decaps of all the circuit modules in these floorplans.

It is assumed that our estimation only predicts feasible decap to release the noise inside the IR-drop module. In this experiment, the item, “Noise\(^{\text{diff}}\)”, stands for the maximum noise. In the iterative estimation [8], the item, “(n)” stands for the number of iterations for the decap budgeting. Table I shows the decap results for the previous greedy estimation [7], the previous iterative estimation [8] and our proposed model for all the benchmark circuits. Based on the purpose of releasing all the IR-drop noises on the tested circuits, the results show that our proposed model uses the fewer number of iterations to estimate feasible decaps for all the tested benchmark circuits. Clearly, our proposed budgeting method can use few decaps to satisfy the IR-drop constraint.

Table I Results for Floorplan-aware Decap Budgeting

<table>
<thead>
<tr>
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<th></th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Decap(nF)</td>
<td>Noise(^{\text{diff}})</td>
<td>Decap(nF)</td>
</tr>
<tr>
<td>apte</td>
<td>20.42</td>
<td>0.18</td>
<td>14.57(2)</td>
</tr>
<tr>
<td>xerox</td>
<td>10.13</td>
<td>0.16</td>
<td>5.24(3)</td>
</tr>
<tr>
<td>hp</td>
<td>5.92</td>
<td>0.17</td>
<td>3.22(3)</td>
</tr>
<tr>
<td>ami33</td>
<td>0.52</td>
<td>0.15</td>
<td>0.067(4)</td>
</tr>
<tr>
<td>ami49</td>
<td>19.28</td>
<td>0.17</td>
<td>8.36(4)</td>
</tr>
</tbody>
</table>

Table II shows the experimental results of the proposed SA-based allocation[10] on our floorplan-aware budgeting and the two-phase 1-D allocation[8] on an iterative decap budgeting for all the benchmark circuits. The experimental results show that the SA-based allocation based on our floorplan-aware budgeting obtains better decap allocation than the two-phase 1-D allocation[8] based on the iterative decap budgeting for the tested benchmark circuits. Clearly, the SA-based allocation based on our floorplan-aware budgeting only uses empty space in the original floorplan to allocate the necessary decaps for the reduction of the final floorplan area.

Table II Experimental Results for Floorplan-aware Decap Allocation

<table>
<thead>
<tr>
<th>Circuits</th>
<th>Floorplan Area (mm(^2))</th>
<th>Two-phase Allocation[8]</th>
<th>SA-based Allocation[10]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Area(mm(^2))</td>
<td>Time(s)</td>
<td>Area(mm(^2))</td>
</tr>
<tr>
<td>apte</td>
<td>46.924</td>
<td>50.706(+8.06%)</td>
<td>12</td>
</tr>
<tr>
<td>xerox</td>
<td>20.639</td>
<td>20.850(+1.02%)</td>
<td>18</td>
</tr>
<tr>
<td>hp</td>
<td>10.427</td>
<td>10.877(+4.32%)</td>
<td>16</td>
</tr>
<tr>
<td>ami33</td>
<td>1.254</td>
<td>1.254(+0.00%)</td>
<td>45</td>
</tr>
<tr>
<td>ami49</td>
<td>36.898</td>
<td>37.766(+2.35%)</td>
<td>57</td>
</tr>
</tbody>
</table>

VI. CONCLUSIONS

It is important for the chip cost to develop an efficient and accurate decap budgeting approach on a given floorplan. In this paper, an accurate estimation uses an exponential discharge style in the equivalent RC circuit to predict the decap size of any circuit module in a given floorplan and a floorplan-aware budgeting approach is proposed to assign feasible decaps onto all the circuit modules to release all the IR-drop noises in the floorplan.

REFERENCES