Hot-carrier reliability of 20V MOS transistors in 0.13 μm CMOS technology

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Abstract

This paper presents results of reliability investigation of 20V N-Drift MOS transistor in 0.13 μm CMOS technology. Due to high performances required for CMOS applications, adding high voltage devices becomes a big challenge to guarantee the reliability criteria. In this context, new reliability approaches are needed. Safe Operating Area are defined for switch, V_{ds} limited and V_{gs} limited applications in order to improve circuit designs. For V_{ds} limited applications, deep doping dose effects in drift area are investigated in correlation to lifetime evaluations based on device parameter shifts under hot carrier stressing. To further determine the amount and locations of hot carriers injections, accurate 2D technological and electrical simulations are performed and permit to select the best compromise between performance and reliability for N-Drift MOS transistor.

I. Introduction

High Voltages (HV) MOSFETs have been developed for variety of HV applications where supply voltages between 10V to 20V are required in analog ICs designed in CMOS technology, as for telecommunication applications [1-2]. HV transistors are integrated in a standard low-cost 0.13 μm CMOS process using some specific process steps [3]. Because of the high drain voltage used, these devices are more sensitive to hot carrier degradation than low voltage transistors and new degradation mechanisms appear due to the architecture of these devices [4-5-6-7]. As main process steps are dedicated to the improvement of low voltage CMOS performance and reliability, high voltage devices reliability optimization becomes a big challenge. In this context, a new reliability approach is needed.

Safe Operating Area (SOA) [8-9-10-11] are defined for switch, V_{ds} limited and V_{gs} limited applications (see Figure 1) according to circuit design requirements. For switch SOA, reliability tests are performed at 125°C on nominal length devices in off-state (V_{dsmax}=20V) and on-state (V_{dmax}=400mV). Concerning V_{ds} limited SOA, hot carrier injection (HCI) tests are performed also on nominal length devices but addressing all different cases I_{bmax}, V_{g}-V_{th} = 300mV and V_{gmax} at V_{dsmax}, measuring the full set of device parameters. For this SOA a minimum V_{dmax} of 10V was required by IC designers. Last SOA typically concerns small-signal analog applications where low V_{th} overdrive but very large V_{ds} signal swings are required. On the other hand, longer than nominal devices are preferred to improve matching and noise figures. Tests are performed to guarantee reliability criteria especially for V_{g}-V_{th} = 300mV case at 20V, and involve fewer electrical parameters (G_{m}, V_{th}) as devices work only in saturation regime. In this paper, the impact of drift area doping on N-Drift

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reliability is studied in order to extend $V_{ds\text{max}}$ as much as possible on $V_{ds}$ limited SOA. Our analysis, supported by TCAD (Technical Computer Aided Design) simulations, allows better understanding of HCI degradation mechanisms and permits to obtain the best trade-off between performance and reliability.

![Figure 1](image1.png)

**Fig. 1:** Safe Operating Area taking into account switch (a), $V_{ds}$ limited (b) and $V_{gs}$ limited (c) applications for the 20V N-Drift MOSFET. Channel length requirements and critical electrical parameters are shown for each SOA.

### II. Device Description

20V N-Drift MOS transistors are processed (see fig. 2) with 85Å gate-oxide thickness, gate-length and gate-width about respectively of 0.5 µm and 10 µm. The distance Olap is about 0.6 µm and the maximum operating gate voltage is 4.8V. These devices have a self-aligned gate on the source side and the drain side is carried out by a conventional CMOS scheme. In order to achieve a breakdown voltage of about 20V, a drift zone is implanted on the drain side with a deep implant of $3\times10^{12}$ at/cm².

The hot carrier stress is performed by applying a sufficiently high DC drain voltage in order to obtain enough electrical parameter degradation at wafer level and a gate voltage corresponding to peak substrate currents. During stress experiments at room temperature, device parameters are monitored at logarithmic stress intervals (five times per decade). Electrical parameters monitored are the transconductance ($G_m$), threshold voltage ($V_{th}$), linear drain current ($I_{d\text{lin}}$ @ $V_d=0.1V$ and $V_g=4.8V$), saturation drain current ($I_{ds\text{sat}}$ @ $V_g=4.8V$ and $V_d=4.8V\&10V$), and the linear on-resistance ($R_{on}$ @ $V_g=0.1V$ and $V_g=4.8V$). Hot carrier failure criterion is fixed at maximum 10% of electrical parameter shift for 10 years.

![Figure 2](image2.png)

**Fig. 2:** Cross section of 20V N-Drift MOSFET.

### III. Experimental results

Figures 3 and 4 show classical characteristics $I_d$ versus $V_{ds}$ and $I_b$ versus $V_{gs}$ for N-Drift MOS transistor with a deep drift implant of $3\times10^{12}$ at/cm². The usual maximum bulk current is observed at $V_g/2$ [12] revealing the impact ionization phenomenon. For higher gate voltage, substrate current increases again certainly due to the high current density and low graded drift doping [13]. After reliability tests using switch configuration no electrical shift were observed [14]. For $V_{ds}$ limited configuration after HCI stress at $I_{b\text{max}}$ with $V_{ds}$ about 14V to 19V (see Figure 5 and 6), a large linear drain current degradation is observed where 10% reduction is reached after $10^3$ s of stress time. Concerning channel parameters we observe that the $V_{th}$ and $G_m$ degradation are smaller than 1% indicating that HCI degradation is not located in the channel region. Taking into account these results in addition to $I_{ds\text{sat}}$ forward and reverse degradation, we suspect that N-Drift resistance degradation is...
responsible of electrical parameter shifts. Referring to $V_{ds}$ limited SOA, the device lifetime extrapolated at 10V obtained with various electrical parameters for $I_{b\max}$ case are inferior to 10% for 10 year-lifetime DC operation. Same results are obtained for $V_{g}V_{th}$ cases ($V_{g}$ corresponding practically to $I_{b\max}$) and smaller shifts are observed for $V_{g\max}$ case.

Fig. 3: $I_{d}$ versus $V_{ds}$ characteristics

Fig. 4: Measured $I_{d}$ versus $V_{gs}$ characteristics

We further show that $V_{gs}$ limited at $V_{g}V_{th}$=300mV is sufficient for a good circuit design, longer gate-lengths must be investigated to guarantee reliability criteria. In order to improve maximum drain voltage for $V_{ds}$ limited application and to confirm N-Drift resistance degradation, three different doses for N-Drift region have been further used with TCAD simulations. Accurate characterizations of the HCI locations and magnitudes are required as the device reliability is extremely sensitive to HCI mechanisms in both the N-drift and STI regions.

Fig. 5: $I_{d\text{lin}}$ relative degradation versus time

Fig. 6: $V_{th}$ relative degradation and delta $V_{th}$ versus time

Fig. 7: N-Drift structure after process simulation
IV. Simulation results

To understand the HCI mechanisms, 2D TCAD simulations with GENESISE ISE Tools have been used to study electric field, current density, electron and hole temperatures by varying bias conditions for three deep doping doses of the drift area. N-Drift devices were simulated using DIOS technological simulator which was enmeshed with MDRAW mesh tool before electrical simulations with DESSIS. On figure 7, we can see the N-Drift standard structure after process simulation.

Low Vg bias (Fig. 8.a)

At low Vg corresponding to \( \text{I}_{\text{bmax}} \) for high N-Drift dose about \( 3 \times 10^{12} \text{ at/cm}^2 \), a strong electron temperature at the P\(_{\text{well}}\) /N-Drift junction is observed which induces maximum hot carrier generation at that location. When dose decreases, electric field is extremely reduced and \( \text{I}_{\text{b}}/\text{I}_{\text{d}} \) ratio decreases (see Table 1). For \( \text{I}_{\text{bmax}} \) stress with N-Drift dose of \( 3 \times 10^{12} \text{ at/cm}^2 \), TCAD results permits to confirm N-Drift resistance degradation due to hot spot in N-Drift region.

High Vg bias (Fig 8.b)

Increasing Vg, maximum electric field is located towards the N-Drift/N\(^+\) region under the drain, hot carriers are now generated in this area. When the dose decreases, current density increases under the STI (Shallow Trench Isolation) and impact ionization phenomenon is clearly increased due to the Kirk effect [13]. When the amount of injected electrons from the N-Drift region is close to the donor density, holes are generated to restore the electrical neutrality. Fig. 9.a and Fig. 9.b present the space charge 2D mapping (see Eq. 1) for low (a) and high (b) Vg values. At high Vg, current flow becomes so strong that the space charge 2D mapping shows an inversion in the Drain region. Relating in a general way the charge density \( \rho \) and its relationship to the electric field E, one can state the following expressions:

\[
\rho = (N_d - N_a - n + p) \quad (1)
\]

\[
\frac{dE}{dx} = \frac{q}{\varepsilon} (N_{\text{drift}} - n) \quad (2)
\]

with q the elementary charge and \( \varepsilon \) the dielectric permittivity (\( \varepsilon = \varepsilon_0 \varepsilon_{\text{si}} \)). The Poisson law (Eq. 2) expresses the variation of electric field along x location as a function of the doping in the N-drift region (N\(_{\text{drift}}\)) and of the injected electrons (n). As much as electron injection increases at high Vg,
electrical field can reverse and holes are also generated in order to keep electrical neutrality; hole generation induces a drain current increase. On Fig.10, we can see the clear impact of a smaller doping dose on the saturated drain current: this is observed by the fact that the avalanche behavior starts at smaller drain voltages because of the Kirk phenomenon.

![Image](Fig. 9: Space charge 2D mapping (blue/green) (a) with \(V_{d}=20V\) at \(V_{g}=V(I_{b,\text{max}})\): At low \(V_{g}\), the light electron injection doesn’t modify the space charge in the Drift zone except under the N+/N-Drift junction where depletion exists. At the opposite, for \(V_{g,\text{max}}\) case at \(V_{d}=20V\) (b), the space charge shows an inversion of the type of semiconductor in the Drift region. Smaller is the dose, larger is the space charge. In this case, holes are generated in this area (Kirk effect) to keep electrical neutrality.

We point out that this dual behavior observed as a function of the larger gate voltage magnitude (\(V_{g,\text{max}}= 4.8V\)) for \(V_{d}= 20V\) prohibits smaller dose for the N-Drift area in order to increase the maximum drain voltage for \(V_{d}\), limited application (see Fig. 10). Table 1 summarizes N-Drift performances (\(R_{on}S\)), \(I_{d}/I_{g}\) ratio and \(I_{d}\) versus \(V_{d}\) behaviours for low \(V_{g}\) and \(V_{g,\text{max}}\). Split with a dose of \(2.10^{12}\) at/cm\(^2\) gives the best compromise between high performances and robust device reliability. Table 2 gives the corresponding extrapolated lifetime parameters for the N-Drift device processed with the same dose. It is shown that the device lifetime is guaranteed for ten years for all lifetime criteria.

![Image](Fig. 10: \(I_{d}\) versus \(V_{d}\) characteristics for the three doping doses.)
Table 1: Performances and reliability summary for 0.5µm gate length

<table>
<thead>
<tr>
<th>Drift dose</th>
<th>Ron*S [mOhm.mm²]</th>
<th>Ids(Vds) @ Vds = 20V [%]</th>
<th>maximum drain voltage for Vds limited (worst case)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1012</td>
<td>18.1</td>
<td>Excellent</td>
<td>strong avalanche (starting at 10V) 15V</td>
</tr>
<tr>
<td>2.1012</td>
<td>14.4</td>
<td>low distortion</td>
<td>slight avalanche (starting at 15V) 11.5V</td>
</tr>
<tr>
<td>3.1012</td>
<td>14</td>
<td>High distortion</td>
<td>No avalanche</td>
</tr>
</tbody>
</table>

Table 2: Extrapolated elementary device DC drift-time for 0.5µm N-DRIFT MOS @ V_d = 10V. (***) means degradations observed are inferior to 1%.

<table>
<thead>
<tr>
<th>Stress condition</th>
<th>τ @ 10% g_m</th>
<th>τ @ 10% V_th</th>
<th>τ @ 10% I_m</th>
<th>τ @ 10% R_m</th>
<th>τ @ 10% I_{dud}4.8V</th>
<th>τ @ 10% I_{dud}10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ibmax</td>
<td>**</td>
<td>**</td>
<td>&gt; 10 years</td>
<td>&gt; 10 years</td>
<td>&gt; 10 years</td>
<td>&gt; 10 years</td>
</tr>
</tbody>
</table>

V. Conclusion

In this paper, a new approach has been presented to ensure high voltage transistor reliability. Safe Operating Area are defined for switch, V_ds and V_gs limited applications. HCI tests were performed in each SOA case. The impacts of the deep doping doses in 20V N-Drift devices on the hot-carrier reliability have been determined for V_ds limited case. TCAD results have confirmed distinct location of the hot-carrier generation as a function of gate voltage where for I_bmax case hot carriers are generated at the P_{well}/N-Drift junction and for V_gmax case near the N-Drift/N^+ (drain) contact. For V_ds limited application, we have shown that a dose of 2.10^{12} at/cm² gives the best trade-off between high performances and device reliability.

References