Reduced Complexity, High Performance Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis

Lizhong Sun, Thierry Lepley*, Franck Nozahic**, Arnaud Bellissant**, Tad Kwasniewski and Barry Heim***
Department of Electronics, Carleton University, Ottawa, ON, Canada, K1S 5B6

Abstract

This paper presents the design consideration of high order digital $\Delta \Sigma$ modulators used as modulus controller for fractional-N frequency synthesizer. A third-order MASH structure (MASH 1-2) is designed and implemented which allows for the input to operate over 75% of the input adder capacity. The number of the output levels is reduced to two bits. The circuit was verified through simulation, ASIC implementation and exhibits high potential for a gigahertz range, low-power monolithic CMOS frequency synthesizer.

1. Introduction

Frequency synthesizers are widely used as local oscillator to provide accurately-defined frequencies and channel selection for wireless transceivers. Fractional-N indirect frequency synthesis based on a PLL (as shown in Fig. 1) is particularly well suited to wireless applications and integrated circuit implementations. The technique allows very narrow channel spacing relative to the output frequency, large bandwidth in the PLL relative to the channel spacing, and high output frequency relative to the processing technology used in the IC fabrication [1][2]. To realize fraction-N division function, the multi-modulus frequency divider (MMD) can be controlled by several techniques: pulse swallowing phase interpolation, Wheatley random jittering and Delta-Sigma ($\Delta \Sigma$) modulation [3]. The use of $\Delta \Sigma$ modulation concepts in modulus controllers results in a beneficial noise shaping of the phase noise (jitter) introduced by fractional-N division. Noise in the vicinity of the divided carrier frequency is small and noise at the higher offsets can be suppressed by the lowpass filter following the phase/frequency detector. The technique is able to achieve low phase noise, good spurious frequency suppression while providing fast settling time, desirable channel resolution and wide tuning bandwidth.

Section 2 of this paper presents the design consideration of high order $\Delta \Sigma$ modulators used as modulus controller for fractional-N frequency synthesizer. In section 3 a third-order MASH structure (MASH 1-2) is designed and implemented. Simulation and experimental results are presented in section 4.

2. High Order MASH Structure for Modulus Controller

The choice of appropriate high order $\Delta \Sigma$ structure requires the consideration of many factors including noise shaping, spurious content of the output spectrum, output levels, loop filter order and circuit complexity. The output noise spectral density of higher order structures monotonically increases at greater rates per unit frequency, resulting in greater SNR or bit resolution per given baseband bandwidth at lower frequencies. However, the price to be paid for this is that higher out of band noise levels requires corresponding higher order of loop filter being implemented in PLL. Typically the loop filter is set one order higher than the order of the modulator to produce the necessary suppression of quantization noise generated by the modulator. Furthermore, the high order $\Delta \Sigma$ modulators increase the complexity of circuits, thus chip size and power consumption increase.

High order $\Delta \Sigma$ modulators can be realized with interpolative and MASH architectures. A disadvantage of high order interpolative feedback structure is that they are subject to instability, although some stable structures have been found [4]. MASH architecture uses a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones [5]. The advantage of this approach is that higher-order noise filtering can be achieved using lower-order modulators. The overall cascaded system should remain stable since the lower-order modulators are more stable. However MASH $\Delta \Sigma$ modulator produce a multibit output which in turn must control a multi modulus divider. For example, a conventional MASH-3 modulator produces 3 bits.
output. To achieve a tuning range from \( n f_{\text{ref}} \) to \((n + 1)f_{\text{ref}}\), eight modules of MMD are required, thus increase the circuit complexity and power consumption.

The frequency resolution of channel selection is dependent upon the number of bits (\( L \)) of the control word (\( K \)) on the input of the modulator, and the rate of the reference frequency \( f_{\text{ref}} \), used by the PLL and the modulator. The hardware required to implement the different order of MASH modulators is estimated. The required number of gate arrays versus number of input bit (\( L \)) are shown in Fig. 2. Although MASH 2-2 and MASH 1-1-1-1 provide higher order of noise shaping than MASH 1-2 and MASH 1-1-1, they take up about twice the size and thus consume larger power. MASH 1-1-1 and MASH 1-2 exhibit the same order of quantization noise. However, as we demonstrate the MASH 1-2 can be designed to have only four levels output instead of eight for MASH 1-1-1. The lower level output of modulus controller reduces the complexity and power dissipation of the MMD. This reduction of power consumption is significant due to the high frequency operation of the frequency divider.

![Figure 2. Required hardware versus number of input bit L](image)

**3. Implementation of the MASH 1-2 Structure**

Fig. 3 shows the implemented MASH 1-2 structure. An equivalent to the first order \( \Delta \Sigma \) modulator is obtained using the Digital Phase Accumulator (DPA) where the \( L \) bits output is a measure of the quantization noise. A second-order Ritchie interpolative structure is used in the second stage. Compared to its higher order structure, the second order Ritchie interpolative structure [6] is much better suited for digital implementation since its feedback coefficients are relative to the power of two. The inversed 2's complement coding scheme is used in error cancellation process to obtain two bits output. Different from the analog implementation, the digital MASH architecture are capable of achieving complete cancellation of the quantization noise produced in the first stage of the modulator. The \( z \)-domain representation of such a modulator is shown in Fig.4.

![Figure 3. The MASH 1-2 modulus controller](image)

![Figure 4. z-domain representation of MASH 1-2 modulator](image)

**The DPA with Carry-In**

To act as pseudo-random number generators, all digital \( \Delta \Sigma \) modulator must be capable of producing a long duration limit cycle. The shorter the period, the higher the spur tone's amplitude. Under certain conditions, a \( \Delta \Sigma \) modulator may not produce a sequence long enough to be of a practical use. The problem can be caused by the presence, at the input to a \( \Delta \Sigma \) modulator, of a static signal \( K \). Assuming that the period of the bit stream is equal to \( P \) for a DPA, we have \( P = 2z/(GCD(K, 2^L)) \) where GCD denotes the greatest common divisor. It is found that the maximum length of the period can be observed only when \( K \) is odd. A simple way to achieve a longer period is to increase the data path by 1 bit and to set the LSB of \( K \) at '1' at the cost of the increased size and power consumption of the circuit. Another solution has also been proposed which uses the carry-in of the adder without increasing the data path width. A carry-in DPA has the carry-in input driven by an output of a D flip-flop, dividing the clock signal by two as shown in Fig.5. The DPA behaves as if there was one more bit in the data path. The
period increases by two which includes a case when \( K \) is even.

\[ K \]

Figure 5. The DPA with carry in.

Implementation of Second Order Ritchie Structure

As with any feedback type system, Ritchie structures have the potential to become unstable. This is mainly due to the unwanted overflows of the accumulators. If the saturation of accumulators can be avoided, the structure would operate with long sequence repetition cycles and spur tones in lower frequency range should be absent. We have adopted the 2’s complement fractional number coding scheme to code the value between \([-2^{M-2}, 2^{M-2}]\). In order to find the adequate internal bit length (M), the z-domain representation of the MASH 1-2 was simulated for all the possible values of input K. It was found that the outputs of all the integrators are within \([-4, 4]\) which results in M equal to L+3. From the coding used, we note that the simplest way to subtract 1 from the \( e_{q1} \) value, when \( Y_1=1 \), is to set its last three bits to 1 (-1 = \( -4 + 1 \)). Application of this coding scheme to both feedback loops allowed the development of feedback logic equations. Fig. 6 shows the implementations of the second order Ritchie structure.

4. Simulation and Experimental Results

Simulation results

The simulations were run from a VHDL description of the hardware implementation. The output sequence is windowed and a FFT is run on it to obtain the power spectrum of the output. We first simulated the modulus controller with static inputs of round binary numbers which give the worst case. Fig.7 shows the spectrum of the bit stream for a 14 bit static input of 5632. The simulation was run on \( 2^{18} \) samples. A slope of 60dB/dec of high pass noise shaping is achieved. For the extreme high and low values of the input K, the modulus controller noise shaping deteriorates. It is found that the highest input value that allows a normal behavior is 14336. The lowest value is 2048. Thus, the maximum range is 12288 and it is 75% of the total range (\( 2^{14} = 16384 \)).

Measurement results

The design was implemented on a Xilinx 3042 Field Programmable Gate Array (FPGA) with 14 bits input. The clock frequency of the circuit was limited to 500 kHz. The bit sequence at the output of the modulus controller was captured with a digital analyzer. A windowing and FFT have been run on those sequences as for the simulations. Fig.8 shows the measured spectrum of the output of the circuit for a static input equal to 5632. It confirms the simulation results in Fig.7.

Figure 6. The implementation of the second stage

Figure 7. Simulation spectrum of the modulator output bit for a static input

Figure 8. Measurement spectrum of the output of the circuit for a static input equal to 5632.
Acknowledgments

The authors gratefully acknowledge the financial support from Motorola Semiconductors and infrastructure support from Telecommunications Research Institute of Ontario, Canadian Microelectronics Corporation and National Science and Research Council of Canada.

References