

Design of a Fast Digital Double Relaxation Oscillation SQUID

M. Podt, A. J. Mieog, J. Flokstra, and H. Rogalla

Abstract—A fast digital Double Relaxation Oscillation SQUID (DROS) with a relaxation oscillation frequency of 100 MHz has been developed. The digital DROS incorporates a DROS and a superconducting up-down counter that supplies the feedback flux. The major advantage of a DROS is that the relaxation oscillations generate an on-chip clock signal and therefore, no external clock is required. In order to maximize the slew rate without compromising the sensitivity, the quantization unit of the feedback flux was adapted to the flux noise of the DROS. This resulted in a designed flux slew rate of $5 \cdot 10^6 \Phi_0/s$. We will discuss the design optimization, numerical simulations, the layout and some experimental results of the digital DROS.

Index Terms—Digital Integrated Circuits, Superconducting Devices, SQUIDS

I. INTRODUCTION

CONVENTIONALLY, the output of dc SQUIDS is linearized by using flux locked loop (FLL) electronics operating at room-temperature. However, because of the small flux-to-voltage transfer of standard resistively shunted dc SQUIDS, the output voltage noise is about one order of magnitude lower than the input voltage noise of a low-noise room temperature dc preamplifier, which would lead to amplifier limitation of the system sensitivity in a direct voltage readout mode. In order to solve this problem, ac flux modulation together with an impedance matching network is often used. On the other hand, the output of the SQUID itself can also be enhanced, as is done for the so-called second generation dc SQUIDS, e.g., SQUIDS with additional positive feedback (APF) [1], double relaxation oscillation SQUIDS (DROSs) [2], [3] and two-stage SQUID systems [4]. In this way, very sensitive SQUID systems have been developed. The slew rate of these systems is limited to about $10^6 \Phi_0/s$, which is mainly determined by the bandwidth of the room temperature FLL electronics and not by the bandwidth of the SQUID itself.

Currently, a lot of research is done on high-resolution, cryogenic particle detectors, such as X-ray detectors based on superconducting tunnel junctions. Although SQUIDS are promising candidates for the readout of these particle detectors, the slew rate and the sensitivity that are required, put severe demands on the FLL electronics. The main advantage of a digital SQUID, which incorporates the SQUID and the FLL electronics on one single chip, is that these sensors have the potential to be both very

sensitive and very fast. Therefore, digital SQUIDS are very promising devices for the readout of cryogenic particle detectors.

Most of the digital SQUID concepts, originally developed at Fujitsu [5], are based on latching Josephson logic. The key elements of this design are a comparator SQUID and a superconducting up-down counter [5], [6]. This comparator SQUID is driven by an external clock. Our concept of the digital SQUID, the Smart DROS, uses a DROS, which is based on relaxation oscillations that are generated in hysteretic dc SQUIDS by an R-L shunt [7]. Since these relaxation oscillations generate an on-chip clock signal, no external clock is required. For single DROSs, the frequency of these oscillations is of the order of $f_{RO} \approx 1$ GHz. Fig. 1 shows a schematic overview of the Smart DROS.

In a Smart DROS, the feedback flux is quantized, i.e., the smallest possible change in the feedback flux is determined by the quantization unit of the feedback flux $\delta\Phi_{fb}$. This is one of the most important parameters in the design of a Smart DROS. In an optimized system, the quantization unit of the feedback flux is equal to the flux noise of the DROS. If the quantization unit is much smaller than the flux noise, the system unnecessarily compensates its own noise and the maximum slew rate will be compromised. On the other hand, if the quantization unit is much larger, the sensitivity will be limited by quantization errors. Previously, we have shown that the Smart DROS should be able to achieve a flux slew rate of $10^8 \Phi_0/s$, together with a flux noise that is comparable to that of conventional dc SQUIDS [7]. In this paper we will present our development of a 100 MHz optimized Smart DROS, which is our first step towards a very fast digital SQUID. The relaxation oscillation frequency was limited to 100 MHz to relax the requirements on the readout electronics.

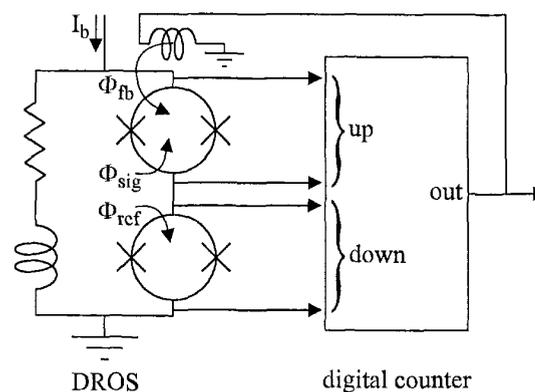


Fig. 1. Scheme of the Smart DROS. The digital counter is implemented in superconducting electronics, integrated on the same chip as the DROS.

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II. THEORY OF OPERATION

The key element of the FLL circuitry of the Smart DROS is a superconducting up-down counter [7]. This Josephson counter has the role of the integrator in a conventional FLL and consists of a superconducting storage loop with inductance L_{st} interrupted by two write gates. In the storage loop, flux quanta are stored and consequently, a circulating current I_{st} is flowing. The circulating current can be increased or decreased by adding respectively extracting flux quanta.

A DROS is connected to the Josephson counter which is used to transform the analog input signal of the Smart DROS (the signal flux Φ_{sig}) to the digital domain, by generating voltage pulses across the signal SQUID and the reference SQUID [2]. The signal SQUID is connected to the up-gate, i.e., each time a voltage pulse is generated by the signal SQUID, the circulating current is increased by an amount $\delta I_{st} = \Phi_0/L_{st}$. On the other hand, a voltage pulse across the reference SQUID causes the circulating current to decrease by the same amount. By leading the circulating current through the feedback coil of the DROS, the counter generates the feedback flux with a quantization unit $\delta\Phi_{fb} = M_{fb} \cdot \delta I_{st} = \Phi_0 \cdot M_{fb}/L_{st}$. Here, M_{fb} is the mutual inductance between the signal SQUID of the DROS and the feedback coil.

The readout can be performed by a second counter at room temperature that counts the number of pulses that are generated by the signal SQUID, N_{sig} , and by the reference SQUID, N_{ref} . The flux that is applied to the Smart DROS is simply given by $(N_{sig} - N_{ref}) \cdot \delta\Phi_{fb}$.

III. DESIGN OPTIMIZATION

A. Coupling Schemes

In order to achieve high slew rates, the quantization unit of the feedback flux should be made as large as possible. In an optimized Smart DROS, the quantization unit is equal to the broadband flux noise of the DROS, i.e., $\delta\Phi_{fb} = \sqrt{S_{\Phi}} \cdot \sqrt{f_{RO}}$. As has been discussed above, the quantization unit should not be larger, since this would cause quantization errors.

The coupling schemes we considered are shown in Fig. 2. In order to make coupling between the feedback coil L_{fb} and the SQUID inductance L_{sq} easier, a transformer can be used. By doing so, the number of windings on top the SQUID can be reduced, which means that smaller SQUIDs might be used. This results in a better noise performance. However, the disadvantage of using a

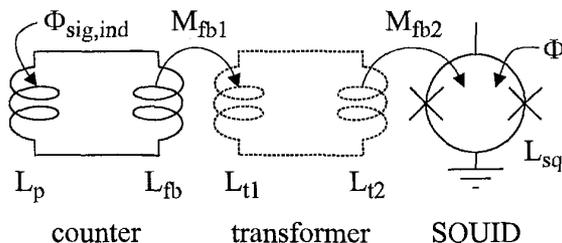


Fig. 2. Possible coupling schemes of the Smart DROS. The dotted transformer is optional and the DROS is represented by a single dc SQUID. The signal flux can be coupled either directly to the SQUID or indirectly via the transformer.

transformer is of course that signal is lost, such that the quantization unit of the feedback flux will be smaller. Therefore, the coupling scheme without transformer is to be preferred, as long as this is allowed within the practical limitations of the layout.

When no transformer is used, the quantization unit of the feedback flux, can be estimated by:

$$\delta\Phi_{fb} = k \cdot \sqrt{L_{sq}/L_p} \cdot \left[\sqrt{\alpha}/(\alpha+1) \right] \cdot \Phi_0, \quad (1)$$

where $\alpha = L_{fb}/L_p$, L_p is the inductance of the pickup coil of the counter and k is the coupling coefficient. It can be shown that optimum coupling is achieved for $\alpha = 1$, which means that the pickup coil and the feedback coil should have the same inductance.

The signal flux Φ_{sig} can either be coupled directly to the DROS or indirectly via the pickup coil of the counter. In case of direct coupling, the output range of the Josephson counter is limited by the critical current of the write gates, i.e., when the circulating current becomes too large, the Josephson counter will not function anymore. However, in case of indirect coupling, the circulating current in the counter is continuously nulled, so that the dynamic range is virtually infinite.

B. Numerical Simulations

The Smart DROS was implemented in the numerical simulation software JSIM [8] to investigate the dynamic behavior. Both the Josephson counter and the complete Smart DROS were simulated extensively [9]. The system is based on a DROS with an inductance of $L_{sq} = 250$ pH and a theoretical flux noise of $5 \mu\Phi_0/\sqrt{\text{Hz}}$. The time constant of the R-L shunt of the DROS was $L_{sq}/R_{sh} = 10$ ns, implying a relaxation oscillation frequency of about 100 MHz. The quantization unit of the feedback flux is about equal to the broadband flux noise of the DROS, i.e., $\delta\Phi_{fb} = 52$ m Φ_0 . Thus, the designed maximum flux slew rate is $5 \cdot 10^6 \Phi_0/\text{s}$.

Fig. 3 shows the result of a numerical simulation of the Smart DROS in operation, with the signal flux coupled directly to the signal SQUID of the DROS. At $t = 0$, the system is in equilibrium and the signal SQUID and the

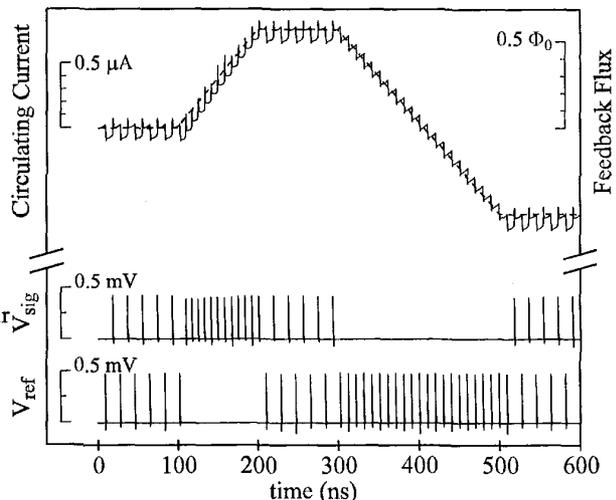


Fig. 3. Numerical simulation of the response of the Smart DROS to variations in the applied flux. The applied flux is represented by the dotted line. V_{ref} is the voltage across the reference junction and V_{sig} is the voltage across the signal SQUID of the DROS.

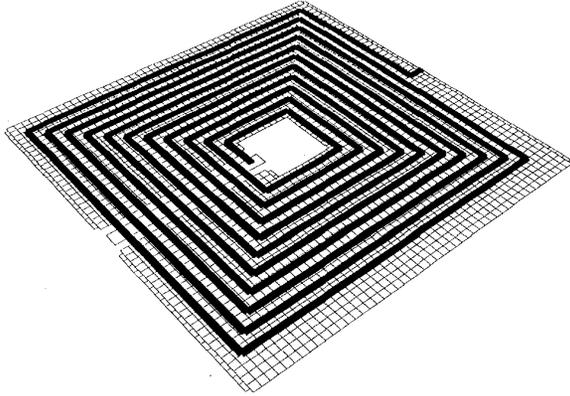


Fig. 4. Meshed gate SQUID used to numerically extract the SQUID inductance, the input coil inductance and the mutual inductance between them. The washer was implemented as a ground plane, the input coil consists of filaments on top of the washer.

reference SQUID oscillate in turn. At $t = 100$ ns, the signal flux is increased with a slew rate close to the maximum slew rate of the system. Consequently, only the signal SQUID generates voltage pulses and the feedback flux is increased until a new dynamic equilibrium is established. At $t = 300$ ns, the signal flux is decreased and only the reference SQUID participates in the relaxation oscillations until the equilibrium is restored again.

C. Inductance Extraction

For proper operation of the Smart DROS, it is important that the design values and the experimental values of the SQUID inductances and the coil inductances agree. For example, the voltage pulses that are coupled to the write gates should induce flux pulses with an amplitude of $\sim 1 \Phi_0$. This means that the mutual inductance M_{in} between the SQUID inductance of the write gate and the input coil on top of it has to be estimated rather accurately. Moreover, the quantization unit of the Smart DROS is optimized with respect to the flux noise of the DROS, which means that the ratio M_{fb}/L_{st} should be correct.

TABLE I
CALCULATED AND EXPERIMENTAL INDUCTANCES

SQUID	Parameter	Analytical	Numerical	Experiment 1
Gate	L_{sq} (pH)	110	105	~ 100
	M_{in} (pH)	907	853	820
DROS	L_{sq} (pH)	281	279	-
	L_{fb} (nH)	21.6	22.0	-
	M_{fb} (nH)	2.3	2.0	2.1

We have estimated the inductances both analytically [10] and numerically [11]. The two most important contributions to the SQUID inductance are the hole inductance L_h and the slit inductance L_l . Typically, the slit inductance is of the order of $0.4 \text{ pH}/\mu\text{m}$ [12]. The inductance of an N -turns coil completely covering the SQUID washer is estimated by:

$$L_{in} = N^2(L_h + L_l/3) + L_s, \quad (2)$$

where L_s is the stripline inductance of the coil. Similarly, the mutual inductance between the coil and the SQUID is:

$$M_{in} = N(L_h + L_l/2). \quad (3)$$

For numerical inductance extraction, the SQUID washer is implemented as a meshed ground plane, with a hole in the middle and a slit, as is shown in Fig. 4. The coil on top of the SQUID consists of filaments. The accuracy of the calculations is determined by the discretization level of the ground plane and the filaments and thus by the processor speed and the memory of the computer. As is shown in Table I, the numerically calculated values and the experimental values of the inductances correspond quite well.

IV. EXPERIMENTS

A. Chip Design

We have designed and fabricated Smart DROSs with parameters based on the numerical simulations and numerical inductance extractions discussed above. Fig. 5 shows a micrograph and the corresponding schematic overview of the complete system. The Nb/Al/AlO_x/Al/Nb

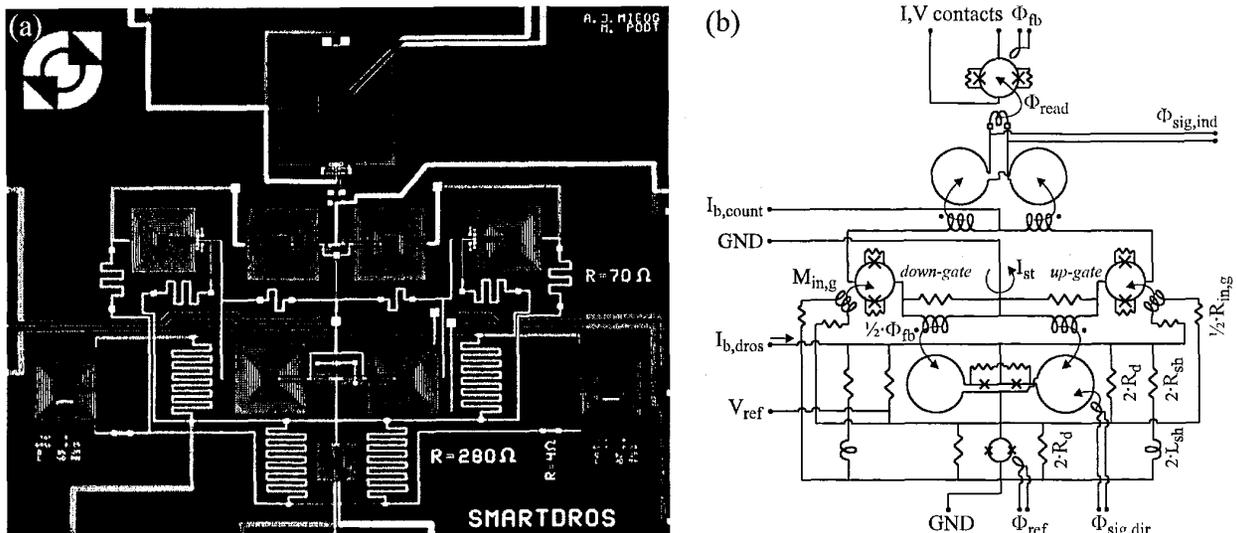


Fig. 5. (a) Micrograph and (b) scheme of the optimized 100 MHz Smart DROS based on a gradiometric DROS with reference SQUID. The readout SQUID on top of the SQUID, which can be connected and disconnected, can be used to measure the circulating current in the Josephson counter. The readout can also be performed by measuring the output pulses across the signal SQUID and the reference SQUID.

junctions of these devices are defined by reactive ion etching in SF₆ and have a minimum size of 4 μm × 4 μm.

The chip was designed such that in principle it can be read out by either a readout SQUID, measuring the circulating current in the Josephson counter, or a differential counter at room temperature, counting the voltage pulses. However, the slew rate of the Smart DROS can only be measured using a counter and not with a readout SQUID. Both the intermediate flux transformer between the readout SQUID and the Josephson counter and the signal SQUID of DROS have a gradiometric "figure-8" layout. This reduces parasitic coupling and eliminates flux variations in the DROS or in the readout SQUID caused by fluctuations in the bias current of the counter.

In order to investigate the dynamic range of the Smart DROS, the system was designed such that the readout SQUID can be connected or disconnected. When the readout SQUID is not connected, the signal flux can be applied either directly to the DROS or indirectly via the pickup coil of the counter, which is part of the intermediate flux transformer. Moreover, chips with an additional inductance in the storage loop of the counter were also made, such that the effect of the quantization unit could be studied.

B. Measurements

Fig. 6 shows the measured flux-to-voltage characteristic of a separate DROS, i.e., the Smart DROS without the FLL circuitry. The flux-to-voltage transfer is ~1.7 mV/Φ₀. The mutual inductance between the series-connected 9½-turns feedback coils and the signal SQUID of the DROS was $M_{fb} = 2.1$ nH, which is very close to the design value, see Table I. From the measured critical current modulation depth of the write gate, the SQUID inductance was determined to

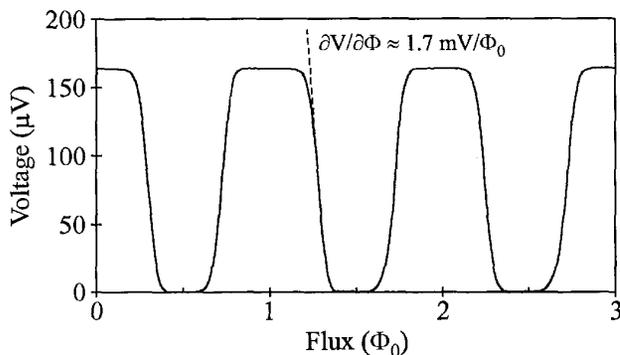


Fig. 6. Experimental flux-to-voltage characteristic of a separate DROS. The signal flux was applied via the single-turn input coil on top of one of the washers of the signal SQUID.

be $L_{sq} \approx 100$ pH and the mutual inductance between the SQUID and the input coil was measured to be $M_{in} = 820$ pH. Also these values meet the design values quite well.

Currently we are developing a digital readout mode, for which broadband amplifiers and differential counters are required. This is necessary to experimentally determine the slew rate and the bandwidth of the Smart DROS.

V. DISCUSSION AND CONCLUSIONS

We have described the optimization of a 100 MHz Smart DROS. Optimization means that the quantization unit of the feedback flux is adapted to the flux noise of the DROS. This results in high slew rates and a large bandwidth. Also an important issue in the optimization of the Smart DROS is the coupling scheme. Direct coupling limits the dynamic range of the system, whereas indirect coupling leads to a virtually infinite dynamic range.

Numerical investigation of the Smart DROS formed a key element of the design process. We have shown that by using the inductance extraction software FastHenry [11], the inductance can be estimated quite well.

The next step in the development of our Smart DROS system will be the design of a digital readout scheme. Currently we are developing broadband amplifiers and a CMOS differential counter, such that the high slew rate and the large bandwidth can experimentally be verified. In the future, the relaxation oscillation frequency can be increased to the GHz range, which allows slew rates up to 10^8 Φ₀/s [7].

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